ISSN: 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering
Vol. 1, Issue 1, July 2012

Comparative Study of Power, Delay and Noise of Logic Gates between CMOS and GaAs MESFET

Saradindu Panda[1], Sanjoy Bhadra[1], B.Maji[2], A.K.Mukhopadhyay[3]

[1]Dept. of Electronics and Communication Engineering, Narula Institute of Technology, Kolkata, India
[2]Dept. of Electronics and Communication Engineering, NIT, Durgapur, India.
[3]Director, BITM, Santiniketan, Birbhum.West Bengal, India
saradindupanda@gmail.com, amisanjaynarula@gmail.com, bmajiecenit@yahoo.com, askm55@gmail.com

Abstract:
This Gallium Arsenide MESFET based an absolutely new model of universal gates has been designed, analysed, reviewed & compared. Overall the newly designed model is fed by physical inputs which are highly researched and developed several times. This model is capable to remove all the difficulties of previously proposed and designed models. The necessity of implementing this type of structure is to encounter absence of dielectric in the CMOS structure [1]. As we remember structure of MOSFET; there Si was implanted beneath the gate and this oxide layer actually acts as the dielectric material alike to any capacitor. Actually there is no provision to implement such kind of dielectric during the fabrication process of the MESFET. Observing this analogical difference it is planned that if somehow any kind of dielectric material which is nearer to the oxide layer, implanted in the MOSFET during fabrication, is planted in the gate terminal without hampering the fabricated structure the device will analogically same as the MOSFET. This is actual motto to implement MESFET based design.

Keywords: GaAs, MESFET, CMOS, Power, Delay, Noise

I. INTRODUCTION

In the year of 1991 Mr. Mikael Anderson[2] proposed three different types of logic families to design the universal gates by MESFET. Successful design of NOT and AND gates were made by him.

MESFET was first invented and developed in mid of 1970s for necessity of manufacturing high speed communication devices, such that device can handle the signal frequency in GHz range and only for that reason the device will be designed and developed. This MESFET mainly used to make special device such as *GUNN DIODE*, *TUNNEL DIODE*, *IMPATT DIODE*[3] *etc.* Moreover this device has a great application on manufacturing communication instruments such as, sample and hold circuit, PAM and PCM modulator demodulator etc.

It has been observed that the main disadvantage of the CMOS based device was '***Unsupported GHz ranged FM or any kind of Microwave signal***' either the device comes to death or it becomes very slow response zone. So this type of device can't be used in satellite or high-speed communication devices. Moreover that the devices have low FAN – OUT capabilities and not a good noise immunity capabilities and speed is lower as compared to ECL based devices. Today the trend is high speed without hampering the power consumption to a great extent and should be a better noise immunity level. Focusing this new trend we have started our research on MESFET that we have observed that MESFET can fulfil all these need and this device can be used in the satellite communication also.

II. RELATED WORK

In the year of 1991 Mr. Mikael Anderson has proposed two basic different models for MESFET, (i) DEPLETION type and (ii) ENHANCEMENT types. Where the DEPLETION type MESFET has four different logics; (a) BFL, (b) SDFL,(c) CDFL, (D) SCFL and ENHANCEMENT type MESFET has three different types logics (a) DCFL, (b) SBFL and (c) E/D BFL. Each of the logic has suffered some problems one has speed high but power consumption high but other reduces power consumption but propagation delay was high and some contains more numbers of gates. Analyzing all possible realizing characteristics Mr. Mikael Anderson has come to the conclusion among all the logic families E – DCFL is the best optimized one as it contains comparatively less nos of gates and consumes less power and optimized propagation delay.

III. PROPOSED DESIGN PRINCIPLES

Now we are going to discuss about our proposed design. At first we should remember that all the designed circuits are designed using same kind of material → ***Enhancement type***

ISSN: 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering
Vol. 1, Issue 1, July 2012

GaAs based MESFET; power supply (Vdd) to all circuits are same and it is 4.5 V for all.

A. NOT Gate

The schematic of newly designed GaAs FET based inverter is shown in Fig. 1. The diagram is exactly same as the CMOS based diagram[1] but the only difference is that each and every gate terminal of the MESFET is mounted by a semiconductor based capacitor. In the design methodology 1 P and 1 N type MESFET in series and shorting the gate terminal the input data is supplied as the bit format. The Input and output waveform is shown in Fig. 2.

B. AND, NAND, OR, NOR, XOR GATE

The NAND gate is also designed using the same methodology with MESFET used in the CMOS based design [1] as shown in Fig. 3. The Input and output waveform is shown in Fig. 4. The NOR gate is designed as shown in Fig. 5. The Input and output waveform is shown in Fig. 6. If we use an Inverter at the output of the circuit then we will get the OR gate. The Input and output waveform is shown in Fig. 7. The XOR gate is designed as shown in Fig .8.

IV. RESULT ANALYSIS

Now we are going to compare the Power, Delay and Noise of our designed circuits using GaAs MESFET with the Conventional CMOS based devices. The Comparison is Shown in the following Table 1. The Comparative analysis of Power is shown in Fig 9, Delay in Fig.10 and Noise in Fig. 11.

The specification of semiconductor based capacitor are: Length (L): - 150 nm, Width (W): - 450 nm, Junction Bottom Capacitance: - 0.3nF/m,Junction Sidewall Capacitance: - 0.5nF/m, Narrowing due to side etching: - 50nm.

TABLE I
COMPARATIVE RESULT OF POWER , DELAY AND NOISE OF OUR DESIGNED CIRCUITS AND CONVENTIONAL CMOS DESIGN LOGIC GATES

Logic	*Device*	*Noise (All are in the pico range)*	*Power (Pico Watt)*	*Delay (pico seconds)*
CMOS	**NOT**	52.035	7.323	9.00
	AND	722.535	5.680	8.00
	OR	2839.062	5.851	1.00
	XOR	2411.073	5.877	16.00
MESFET	**NOT**	72.17	10.196	0.245
	AND	378.86	15.390	0.014
	OR	1181.98	15.010	0.003
	XOR	1617.97	10.036	5.001

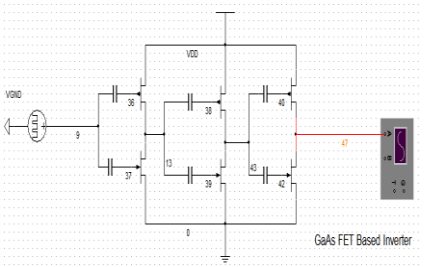

Fig 1. Schematic Diagram of GaAs FET based Inverter circuit

Fig 2 Input and Output Waveform for NOT Gate

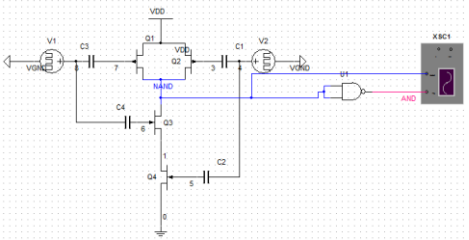

Fig 3. Schematic Diagram of GaAs FET based NAND circuitry.

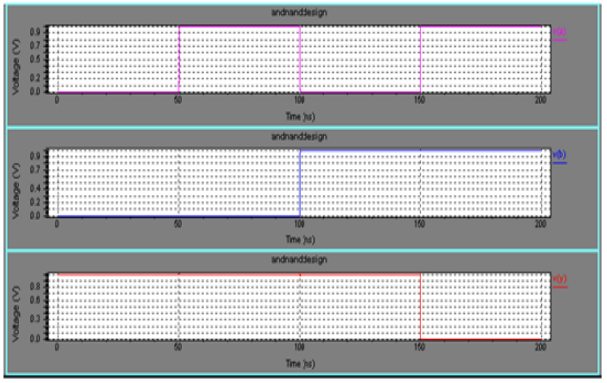

Fig 4. Input and Output Waveform for NAND Gate

ISSN: 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering
Vol. 1, Issue 1, July 2012

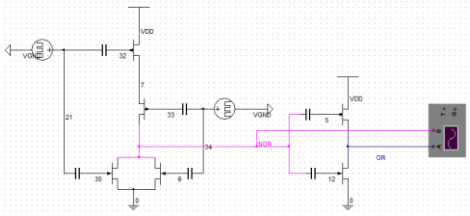

Fig 5. Schematic Diagram of GaAs FET based NOR circuitry

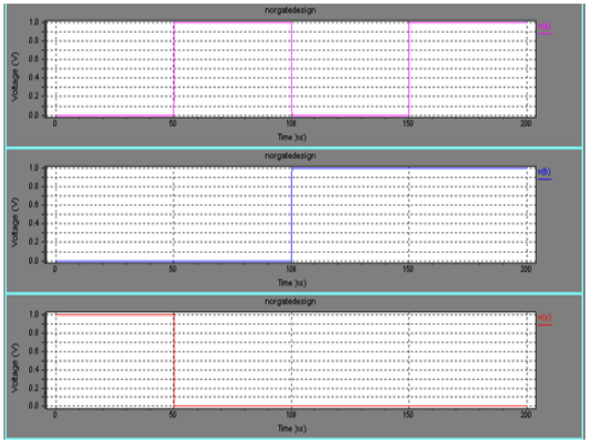

Fig 6. Input and Output Waveform for NOR Gate

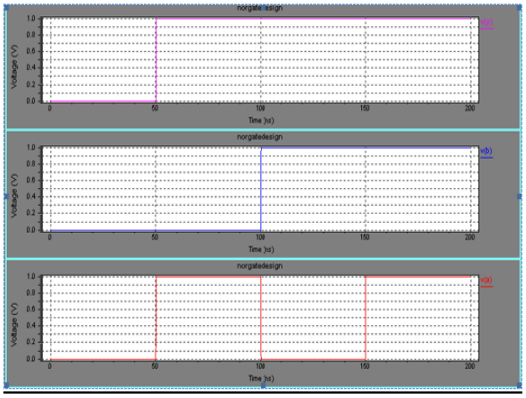

Fig 7. Input and Output Waveform for OR Gate

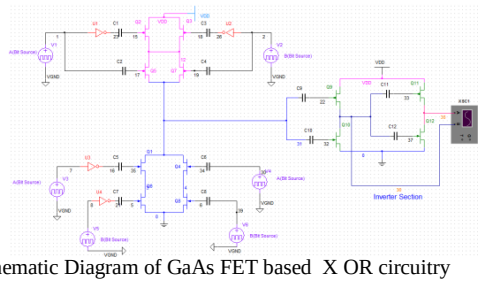

Fig 8. Schematic Diagram of GaAs FET based X OR circuitry

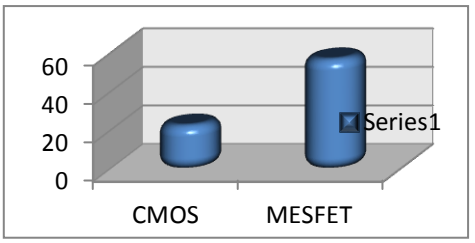

Fig 9. Average comparison of Power Consumption between CMOS and MESFET

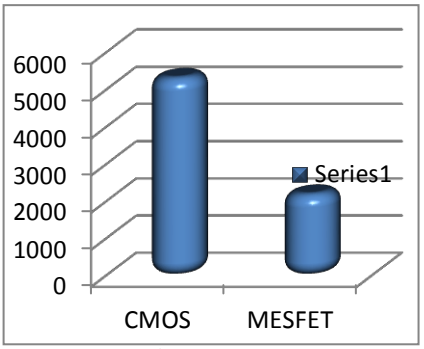

Fig 10. Average comparison of Delay between CMOS and MESFET

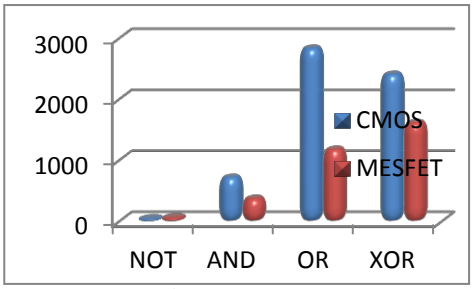

Fig 11. Average comparison of Noise between CMOS and MESFET

V. CONCLUSION

From the above analytical data we can conclude that the CMOS based device consumed low power; but MESFET based devices have better noise immunity than the CMOS based devices and it works too faster than CMOS based devices.

Though the high power consumption issue has not been encountered in this newly designed device it has several advantages which are listed below:

Advantages: -

- Better Fan – Out (As we see the NOT gate circuitry then we will see that it actually driving 2 other same NOT gate by its output.)
- Better Noise Immunity (MESFET based devices has better noise immunity than CMOS; follow chart)
- Operates at High frequency range (All the output of the circuitry given here are in the 200 MHz

frequency range but they are also tested in the GHz frequency range and working as same; so that we can use this for satellite communication).

- Can handle GHz to THz ranged FM signal & GHz ranged AC source.
- Negligible internal delay.
- Better output signal quality than CMOS based device.
- All initial delay for the bulky design is in the 0 level.

The designed devices also have some difficulties and those have been tried to minimize with the best effort such that the device can work for better performances.
The only and the main difficulty is:

- Large amount of power consumption; as we mentioned above that to operate a MESFET based designed circuit optimum supply voltage or VDD should be 4.5V.

Moreover that, it has low noise immunity level compared to CMOS based design.

ACKNOWLEDGMENT

The authors would like to thank Prof. (Dr.) M.R.Kanjilal and Faculty Members, Department of Electronics and Communication Engineering, Narula Institute of Technology, WBUT, for many insightful discussions.

REFERENCES

[1] Sung – Mo Kang; Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", Book.

[2] Mikael Andersson**,** "GaAs MESFET MODELING FOR DIGITAL INTEGRATED CIRCUIT SIMULATION".

[3] Samuel Y. Liao,"Microwave Devices and Circuits", Book, 3rd Edition.

[4] Dimitris Pavlidis, "HBT vs. PHEMT vs. MESFET: What's best and why?", Copyright © 1999 GaAs Mantech.

[5] Otto Berger, "GaAs MESFET, HEMT and HBT Competition with Advanced Si RF Technologies", Siemens Semiconductor Group, Copyright © 1999 GaAs Mantech

Biography

Saradindu Panda
He received M.Tech from Jadavpur University in 2007 in V Design and Microelectronics Technology. He is pursuing his P at NIT, Durgapur, West Bengal, India. Presently, he is invol in design and management of low-power and high sp integrated circuits with Solid State Devices in Nano Regime. is now senior faculty in ECE Department at Narula Instutute Technology, Agarpara, Kolkata, India. He has 7 years teach experience. He is author and Co-author of more than publications in different International and National Journals Conference Proceedings. His main research interest on to des low power , low noise VLSI Circuits and Noise modeling Nano Devices.

Sanjoy Bhadra
He is a final year B.Tech Student in Electronics and Communication Engineering, Narula Institute Of Technology under West Bengal University Of Technology.

Prof. (Dr.) Bansibadan Maji
He is now a senior Professor of ECE Department in NIT, Durgapur, West Bengal, India. He is now Head of The Department of ECE at NIT. His main research area on Microwave , Antenna, VLSI Design and Low power Device and Circuits. He is author and Co-author of more than 50 publications in different International and National Journals and Conference Proceedings.

Prof.(Dr.) Asis Kumar Mukhopadhyay
He received B.E. in Electronics and Communication Engineering from IE(I), Calcutta, M.Tech in Computer Engineering. from E & ECE department, Indian Institute of Technology, Kharagpur, and Ph.D(Engg) from Jadavpur University Kolkata, India. He has long experience in industry and teaching for more than three decades. Currently, he is the Director of Asansol Engineering College, Asansol, West Bengal, India. He was the Principal of Bengal College of Engineering and Technology for Women, Durgapur. Previously he served as the Dean (Academic) and Head of Department of Electronics and Communication Engineering, Dr. B. C. Roy Engineering College, Durgapur. He also worked at Narula Institute of Technology, Kolkata, College of Engineering & Management, Kolaghat, NERIST, Itanagar and Indian Institute of Technology, Kharagpur in various capacities. His current area of research includes Wireless and Mobile Networks and Overlay-based heterogeneous networks. He has 43 publications mostly in international journal and conference proceedings. He is a Life Fellow of the Institution of Engineers (I), Member, IEEE, Member, IEEE ComSoc, Global Member, ISOC; Sr. Life Member, CSI; Life Member, ISTE, IETE, SSI etc.