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A NOVEL ARCHITECTURE FOR HIGH SPEED 1-BIT FULL ADDER AT 45nm TECHNOLOGY

G. LAKSHMINARAYANA YADAV[1], P. SRAVANKUMAR REDDY[2]
[1] PG-Student, VLSI, [2]Assistant Professor, ECE Department, NEC, Nellore, Andrapradesh, INDIA
[1]lakshminarayana.468@gmail.com, [2]sra1reddy@gmail.com

ABSTRACT

Adder's area unit basic building block of Arithmetic VLSI circuits found in processors and microcontroller within Arithmetic and Logic units. Improvement of adder is so vital so as to extend the performance of those units wherever adders realize application. Full adders, till now, are designed wide selection of structures for improvement of varied parameters like power consumption, performance of speed and physical size. The paper here describes a comparative analysis of 10T and 28T full adder with the aim of accelerating power potency and reducing physical size at 45nm technology. The design carried out by using Tanner e EDA tool at 45nm technology.

Keywords: *1-bit Full Adder, CMOS, low power, tanner EDA tool*

1. INTRODUCTION

Today's there square measure a growing range of moveable applications requiring small-area low-power high-outturn electronic equipment. Therefore, circuits with low power utilization grow to be the foremost vital candidates for style of microprocessors and system mechanism. The battery technology doesn't advance at constant rate because the electronics technology and there's a imperfect amount of power on the market for the mobile systems. The goal of extending the battery lifetime of moveable natural philosophy is to cut back the energy consumed per mathematical process, however low power consumption doesn't primarily imply low energy. To execute associate mathematical process, a circuit will acquire through low power by continuance at terribly low frequency however it's going to take a really lasting to complete the operation.

Adder is a standout amongest the most fundamental segments of a CPU (Central processing unit), Arithmetic logic unit (ALU), and coasting point unit and location era like store or memory access unit. Then again, expanding interest for versatile supplies Such as phones, personal digital assistant (PDA), and Notebook PC, emerge the need of utilizing zone and Power proficient VLSI circuits. Conventional adder is one in all the chief essential components of a processor that decides its out turn, and for address era just if there should be an occurrence of reserve or operation the complete adder execution would have an impact on the system as a whole. a spread of full adders. Abuse static or dynamic logic gates are accounted within the literature. In this paper, have a tendency to propose a logical methodology to style 10-transistor full adders and 28t full adders. Our new adders even have the limit misfortune issue; in any case, the adders square measure supportive in bigger circuits like multipliers regardless of the edge misfortune disadvantage. a substitution full adder known as static energy recovery full adder utilizes exclusively 10 transistors that has the most modest sum scope of transistors and has reduces the power dissipation, for every Power decline is one in all the first issues in today's VLSI style techniques as a consequence of a few reasons one is that the long battery in operation life interest of movable gadgets and second is owing to expanding scope of transistors on one chip brings about high power dissipation.

The power consumption for CMOS circuits is described by the following equation:

$$P_{avg} = P_{dynamic} + P_{short\ circuit} + P_{leak}$$

$$Pavg = fclkCL\alpha iV^2dd + fclkI_{short}V_{dd} + I_{leak}V_{dd}$$

Clearly see that the power depends on different parameters as well as on supply voltage (Vdd). Lowering Vdd would significantly reduce the power consumption of the circuit. This basic concept would be utilized to improve the power performance of the adder in this paper.

2. REVIEW OF 1-BIT FULL ADDER DESIGN

A one-bit full adder is a device with three single bit binary inputs (A, B, Cin) and two single bit binary outputs (Sum, Co). Having both carry in and carry out capabilities, the full adder is highly scalable and found in many cascaded circuit implementations.

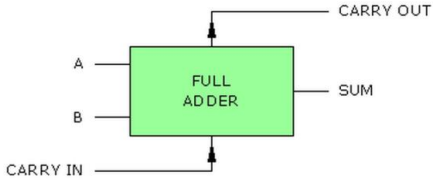

Fig-1:Symbol of 1-Bit Full Adder

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Fig1 shows the symbol of 1-Bit Full Adder. The basic logic functions of the full adder can be summarized in the truth table (right). From the truth table it can be seen that the full adder can be trivially constructed with two half adders. The full adder can also be decomposed into the following logical relationships:

$$S = \bar{A}\bar{B}C_{IN} + \bar{A}B\bar{C}_{IN} + A\bar{B}\bar{C}_{IN} + ABC_{IN}$$

$$S = A \oplus [B \oplus C_{IN}]$$

$$C_{OUT} = BC_{IN} + AC_{IN} + AB$$

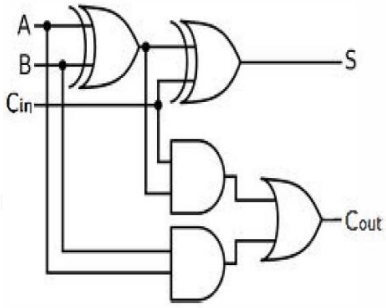

Fig-2:Logic diagram of 1bit full adder

CARRY IN	input B	input A	CARRY OUT	SUM digit
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Fig-3:Truth table of 1-Bit Fulladder

3. CONVENTIONAL CMOS FULL ADDER

The 1-bit conventional CMOS full adder cell is one The well known logic style used to implement the different functions. The CMOS structure consists of PMOS(pull up)and NMOS(pull down) to produce consider outputs. In this style all transistors are arranged completely separate branches.fig-4 shows the 28 transistors conventional full adder. Thus at this fundamental level it is very important to minimize latency and resolve any timing issues in order to avoid issues inevitably brought about by scaling.

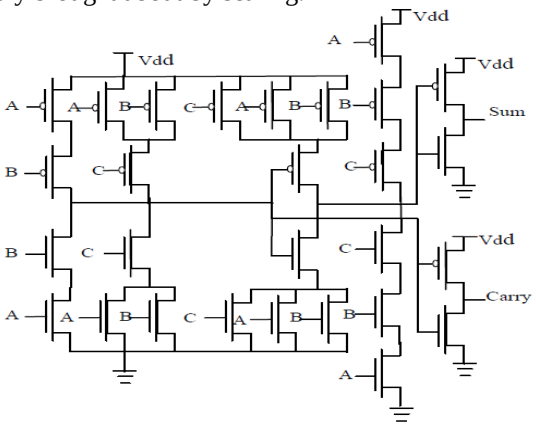

Fig-4: 28T Conventional Full adder

The above shown Conventional full adder is combination of PMOS pull up transistor and NMOS pull down transistor. It is well known for its robustness and scalability at low supply voltages. But its power consumption and transistor count are relatively high for low power arithmetic circuits. In this full adder, Interdependence between signals generation (SUM signal relies on the generation of COUT signal) causes the problem of delay imbalance

4. PROPOSED SYSTEM

10T Full Adder:

The circuit of 10t Adder is an one-bit full adder has 3- input (A, B, and carry in Cin) and 2-outcomes (sum S and carry out Co). The Adder cell can be designed by using five CMOS inverters. input A is straightforwardly joined with inverter first while input B is associated second and third inverter. Second inverter NMOS drain and third inverter PMOS drain are joined first inverter output while second inverter PMOS drain and third inverter NMOS drain are associated straightforwardly input A. Second inverter output is associated fourth inverter input and output Cin is given to fifth inverter.

The power supply VDD is directly connected to first inverter just. Al transistors have least length (LMIN = 45 nm as per utilized Technology), while their widths are commonly propose parameters. The estimation of Wp1 and Wp2 characterizes PMOS transistors width and Wn1 and Wn2 characterizes the NMOS driver transistors width use in first inverter CMOS Inverters. Based on CMOS 0.45 run process technology, the proposed full adder is demonstrated to have minimum power consumption utilization and less power delay product by Tanner simulation contrasting and other earlier literature, the qualities of the novel hybrid full adder demonstrates that the outline has the best power-delay item for carry out signal. Because of the minimum time delay of carry out,

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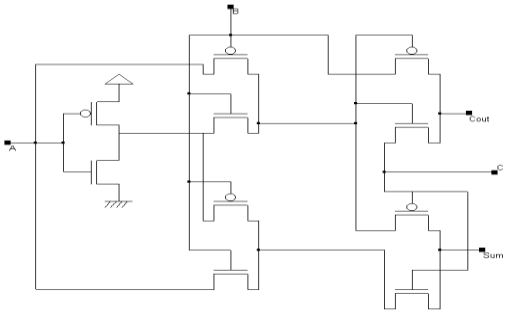

Fig-5:10T Full Adder

5. SIMULATION AND RESULTS

5.1 28Transistors full adder:

We can design the 28 transistors (conventional CMOS) full adder schematic by using S-editor in tanner EDA tool. The schematic diagram shown in fig-6.We has performed simulated results using T-spice in Tanner EDA tool. The supply voltages are 0.7v (45nm) and 1.8v (180nm).The data analysis of the input and output such as A, B, C, sum and carry shown in fig-7.

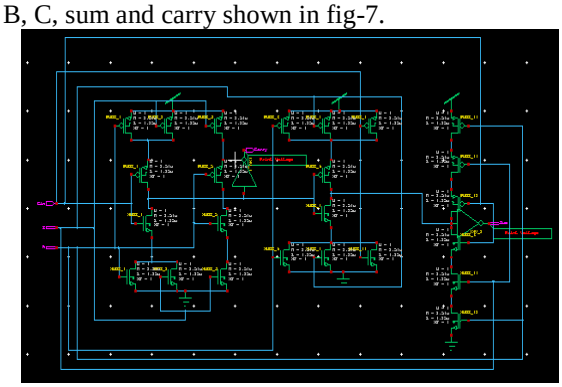

Fig-6: 28T Full Adder at 45nm technology

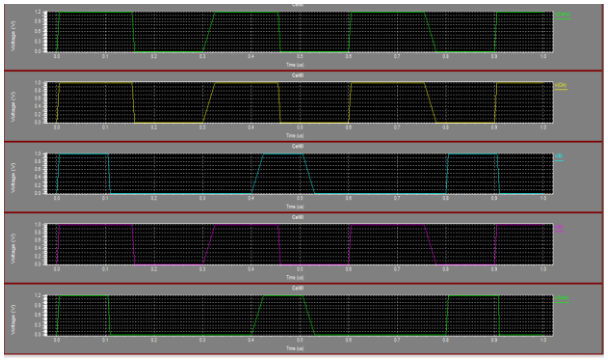

Fig-7: 28T Simulated output waveforms at 45nm technology

5.2 10Transistors full adder:

The 10 transistor 1-bit full adder schematic can be design by using S-edit in Tanner EDA tool. The schematic diagram of 45nm technology shown in fig-8 and the simulated response of output shown on fig-9. The simulation have done by using T-spice in Tanner EDA tool .the simulation performed at 0.7v (45nm) and 1.8v (180nm).

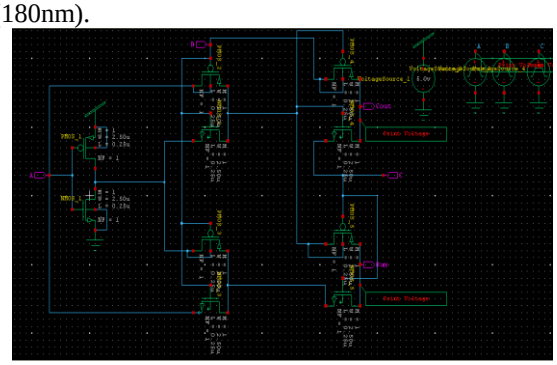

Fig-8: 10Tfulladder 45nm technology

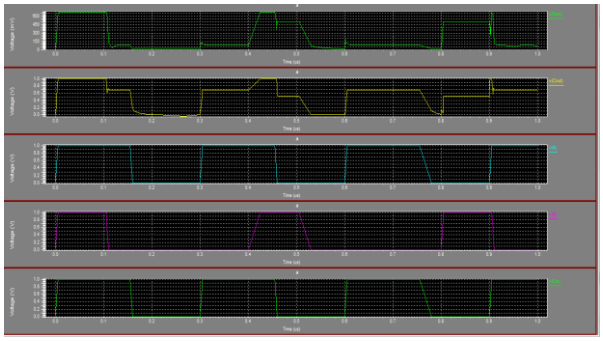

Fig-9: 10T Simulated output waveforms of transient response at 45nm technology

By observing the simulated results of the 28T and 10T the average power calculated by using following equation. Here the simulated waveforms of period 100ns and power supply 0.7v

$$P_{avg} = C_L V_{dd}^2 f_{clk}$$

Where P_{avg} is the average power, C_L is the load capacitance and f_{clk} is the clock frequency .

Simulation results also derive variations in delays. Rise time refers to the time required to change the specified low value to specified high value. Fall time refers to the time required to fall the pulse amplitude at specified value. The average gate delay of rising and falling transition is:

$$t_{avg} = \frac{t_r + t_f}{2}$$

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Power-delay product is defined as the product of leakage power and delay, the power delay product is mentioned as:
PDP = Leakage power × Delay
PDP means power –delay product
All the full adders were supplied with two different Technologies: 45nm and 180nm using different voltages such as 0.7v, 0.5 and 1.8v, 1.2v.

SIMULATION RESULT

COMPARISION TABLE

Technology	Transistors	Voltages (V)	Leakage power (watts)	Delay (ns)	Power delay product (joule)
180nm	28T	1.8	1.03e-4	4.07	4.19e-13
		1.2	7.44e-7	2.49	18.52e-16
	10T	1.8	1.30e-6	2.39	3.10e-15
		1.2	4.28e-7	2.08	8.90e-16
45nm	28T	0.7	5.80e-6	2.51	14.55e-15
		0.5	1.14e-6	2.4	2.73e-15
	10T	0.7	3.84e-8	2.43	9.33e-16
		0.5	4.01e-9	2.39	9.58e-18

Fig-10:- Comparison of Full adder With Different Nanometre Technology

CONCLUSION

In this paper we have carried out a comparison results among the different Nanometer technologies on full adder, including proposed 10t Full adder. The information obtained is useful in the early design phases of an adder circuit, since architectural optimization techniques are based on the knowledge of the full adder cell used. It will very useful to design 1-bit full adder at other CMOS nm Technology.

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