Interactions Between Precisely Placed Dopants and Interface Roughness in Silicon Nanowire Transistors: Full 3-D NEGF Simulation Study

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***Abstract*—In this work, we report a theoretical study based on quantum transport simulations that show the impact of the surface roughness on the performance of ultimately scaled gate-all-around silicon nanowire transistors (SNWT) with precisely positioned dopants designed for digital circuit applications. Due to strong inhomogeneity of the self-consistent electrostatic potential, a *full* 3-D *real-space* Non Equilibrium Green's Function (NEGF) formalism is used. The individual dopants and the profile of the channel surface roughness act as localized scatters and, hence, the impact on the electron transport is directly correlated to the combined effect of position of the single dopants and surface roughness shape. As a result, a large variation in the I_{OFF} and I_{ON} and modest variation of the subthreshold slope are observed in the I_D-V_G characteristics when comparing devices without surface roughness. The variations of the current-voltage characteristics are analyzed with reference to the behaviour of the transmission coefficients, electron potential and electron concentration along the length of the device. Our calculations provide guidance for a future development of the next generation components with sub-10 nm dimensions for the semiconductor industry.**

Keywords—silicon nanowire transistor (NWT), discrete dopants, surface rougness, 3-D noequilibrium Green function simulations (NEGF) component, single atom transistor, quantum transport

I. INTRODUCTION

The silicon technology can deliver sub-10 nm devices where 'every atom counts'. Manipulation of atoms with high precision on such a scale, in principle, can lead to technological innovations, such as transistors with extremely short gate length, quantum computing components and optoelectronic devices. One possible strategy to create this next generation of devices is to precisely place individual discrete dopants (such as phosphorous atoms) in nanoscale transistors.

Recent research, where a single phosphorous atom was embedded within an epitaxial silicon environment, opened the possibility of creating a single-atom transistors [1]. Although such an idea looks spectacularly attractive, the side gate architecture used in Ref 1 is not really fit for the purpose of digital applications. In order to be able to reliably switch on/off such nanometer scale transistors, the preferable transistor architecture needs to be based on the gate-all-around concept [2]. Indeed such all-gate-around silicon nanowire transistors

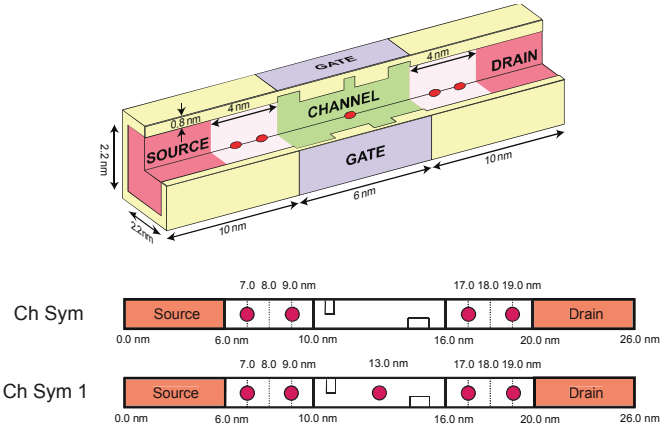

Fig. 1 The schematic view of a device discussed in this paper. All transistors have surface roughness and discrete dopants.

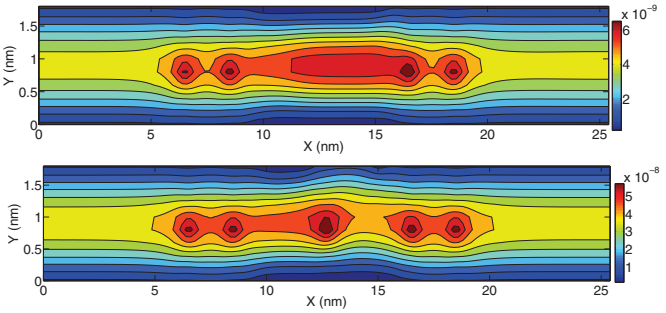

Fig. 2 J_X component of the current (A) of Ch Sym (top) and Ch Sym 1 (bottom). Both devices have the lowest I_{ON} at V_G=0.6 V.

(SNWT) have not only been experimentally demonstrated but have also been extensively studied revealing the impact of a single channel dopant on the device performance [3]. Previously we have demonstrated that dopant(s) in the channel of a nanowire transistor result in reduction of the transistor performance if compared to the undoped channel case [5]. We have also demonstrated that the performance of the SNWT can be improved by engineering the position of dopants in the source/drain access regions [4]. In this paper we study how such 'optimized' SNWT will be affected by interface roughness.

In order to answer the above question, we have carried out

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calculations using an n-type SNWT transistor with 6 nm channel length and a 2.2 x 2.2 nm^2 cross-section, which is illustrated in Fig. 1. Many researchers expect that transistors with such dimensions will mark the limit of CMOS scaling. The important features of such transistors are the unavoidable 'spacers' between the source/drain contacts and the gate, which have to be doped (white rectangular regions in Fig. 1). Based on the volume of the spacer (access) regions and the solid solubility of phosphorous in Si there are on average 2 dopants on each side of the gate for the applied SNWT dimensions. It has been demonstrated already that the randomness of the dopants in the access region can introduce significant variably in the characteristics of the SNWT [4]. Here, however, we will assume that future technology innovations will allow us to align the dopants in the most favourable (from the device performance point of view) position marked 'Ch Sym' in Fig. 1. This Ch Sym transistor with an undoped channel will be our reference point, which will allow us to compare performance of analogous transistors, such as Ch Sym 1 presented in Fig. 1. The device marked as 'Smooth' in our results section is introduced in order to provide comparison with our previously published works [5], and represents the SNWT with continuous doping in the soruce/drain contacts up to the gate edge.

This work begins with a brief description of the self-consistent NEGF/Poisson algorithm in section II. Section III (performance evaluation and variability) presents results of the simulations where we reveal the combined effect of channel surface roughness and discrete dopant position in the Ch Sym and Ch Sym 1 SNWT on the current-voltage characteristics. Moreover, the results are described in terms of transmission function profile, density of states, electron density and electron potential along the wire. The final section summarises the main findings of this work.

II. Transport Model and Simulation Methodology

Simulations are carried out using the quantum transport module of the GSS TCAD simulator GARAND [6]. Accurate modelling of such small transistors with channel lengths of sub-10 nm, particularly in the presence of discrete dopants and surface roughness, requires a full 3-D Non-Equilibrium Green's Function (NEGF) quantum transport treatment due to strong quantum confinement and tunneling [5]. In our work we neglect all sources of incoherent scattering, such as phonon interaction. Based on experimental evidence and previous research we believe that the inclusion of phonon scattering would have little impact on our results. Moreover, in the highly doped source and drain regions the scattering is dominated by impurity scattering and phonons play a minor role. The random rough interface between Si and SiO_2 is introduced using the approach described in Ref. [4]. Any roughness between the oxide and the gate material is ignored.

The Hamiltonian used in the discretisation of the NEGF equations is the effective-mass Hamiltonian that folds the full crystal interaction into the electron effective masses. The effective masses of the valleys are extracted from tight binding calculations that capture the dependence of the electron band structure on the nanowire cross-section. Due to the presence of the small cross-section of the SNWT, only four of the six valleys of the silicon conduction band were included. The two

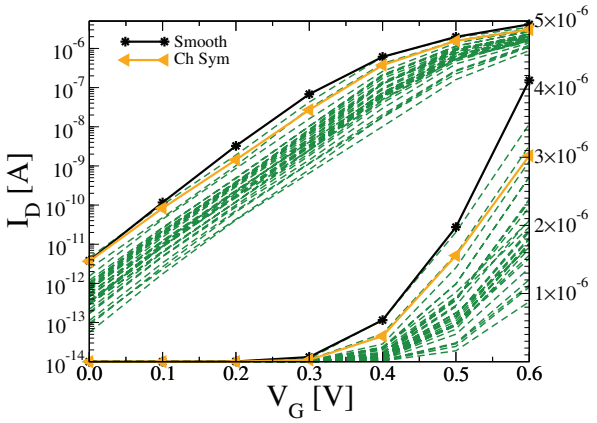

Fig. 3 I_D-V_G characteristics of 30 Ch Sym nanowire trasnsistors with various paterns of surface roughness. The smooth transistors and the device without channel surace rougness (Ch Sym) are shown for

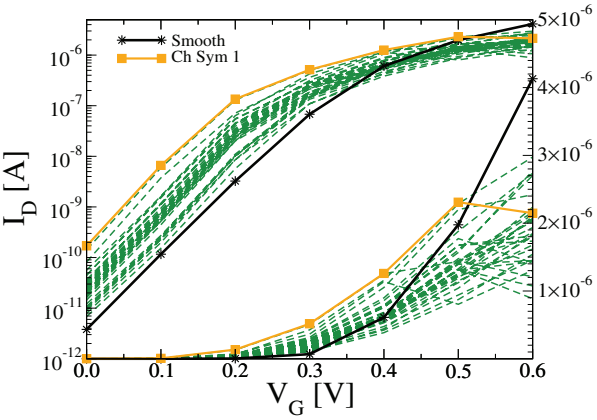

Fig. 4 I_D-V_G characteristics of 30 Ch Sym 1 nanowire trasnsistors with various paterns of surface roughness. The smooth transistors and the device without channel surace rougness (Ch Sym 1) are shown for comparison.

valleys that were neglected have transversal masses ($0.3m_e$) in the direction perpendicular to the wire axes resulting in a larger ground-state-energy shift. As a result, the electron population in these valleys is negligible if compared to the other four valleys for the simulated nanowire orientation, diameter, temperature and bias conditions. The correlation matrix, $G^<$, was calculated using a recursive algorithm. Boundary conditions of the Green's function equations at the contacts, which are given throughout the contact self-energies, were defined by using the algorithm described in reference [5]. The electron density is used to calculate, self-consistently, the electrostatic potential through the Poisson's equation. The obtained solutions of the NEGF and Poisson equations are iterated until density and current converge.

III. Performance Evaluation and Variability

All devices described in this paper have *surface roughness* and *precisely placed discrete dopants* in the source and the drain to avoid statistical variability. The I_D-V_G characteristics for 30 devices *without* and *with* a single channel dopant are presented in Fig. 3 and Fig. 4 correspondingly. The smooth transistors and nanowires without channel surface roughness

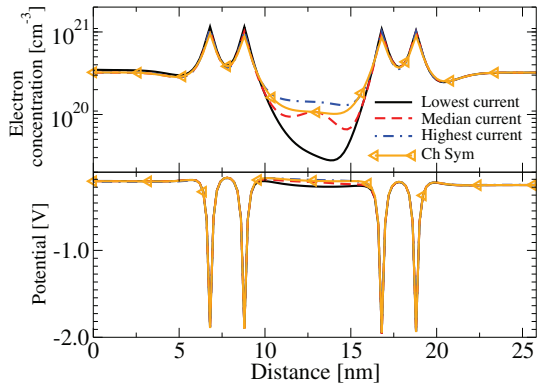

Fig. 5 Density and potential along the wire at V_G = 0.5 V for Ch Sym and three surface roughness devices with lowest, median and highest I_{ON}.

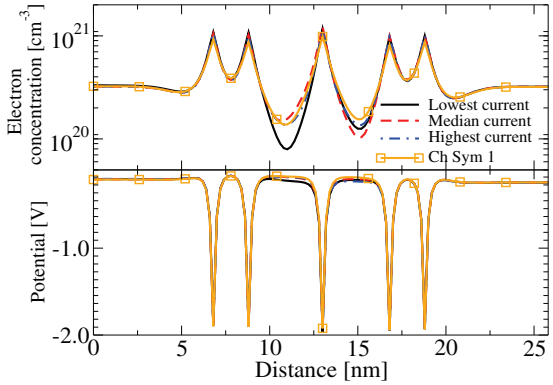

Fig. 6 Density and potential along the wire at V_G = 0.5 V for Ch Sym 1 and three surface roughness devices with lowest, median and highest I_{ON}

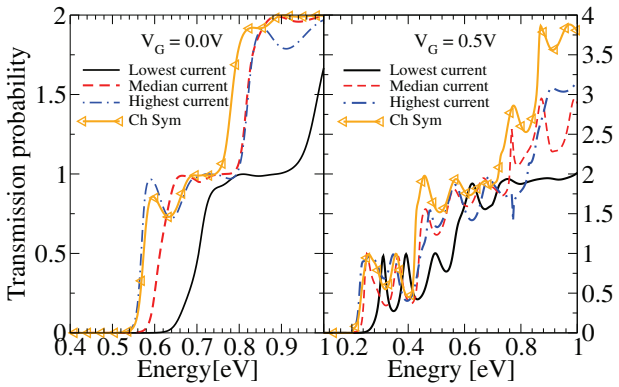

Fig. 7 Transmission probability at V_G = 0.0 V and V_G = 0.5 V for Ch Sym and three surface roughness devices with lowest, median and highest I_{ON}.

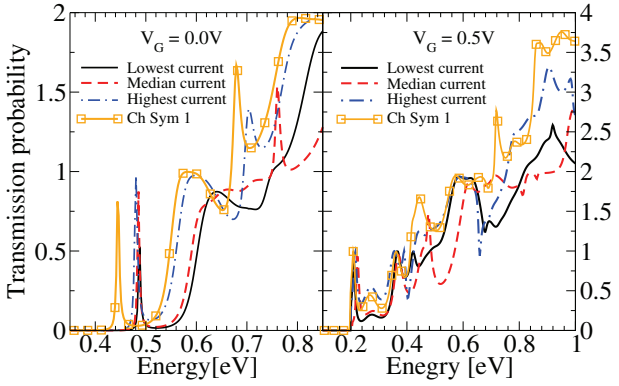

Fig. 8 Transmission probability at V_G = 0.0 V and V_G = 0.5 V for Ch Sym 1 and three surface roughness devices with lowest, median and highest I_{ON}.

(Ch Sym and Ch Sym 1) are shown for comparison. More information about devices with precisely placed discrete dopants and without channel surface roughness can be obtained from our recent publication [5].

The individual dopants and surface roughness act as localized scatters and, hence, the impact of electron transport is directly correlated to the position of single dopants and surface roughness pattern in the channel. Unfortunately, the unavoidable interface roughness (Fig. 1) can negate the effect of the precise doping placement. As a result, we observe a threshold voltage shift and I_{OFF}/I_{ON} variation in the Ch Sym and Ch Sym 1 devices due to scattering.

An analysis of Fig. 3 reveals important features in the I_D-V_G characteristics related to channel *surface roughness*. The results are similar to those analysed in our previously published paper [4]. They can be summarised by the following important observation. The I_{ON} and I_{OFF} is smaller for almost all microscopically different devices in comparison to the Smooth and Ch Sym transistors. Additionally, we observe a subthreshold shift of approximately 130 mV but no significant changes in the subthreshold slope, which indicates non-additivity in the combined scattering processes.

Fig. 4 shows important features in the I_D-V_G characteristics related to the combined effect of *surface roughness* and *single channel dopant.* Firstly, all devices with *surface roughness* have lower I_{OFF} in comparison to the Ch Sym 1 transistor. Hence, introduction of a variation of the channel thickness with the combined presence of a single dopant in the middle of the channel in principle could lead to decreasing of the leakage current. However, the Smooth device still has the lowest I_{OFF} relative to all single channel dopant transistors.

Secondly, the I_{ON} variation is significant and most devices with rough interface have lower 'drive' current in comparison to the Ch Sym 1. However, it is possible to have a rough device with higher I_{ON} than the Ch Sym 1 case but probability for this to happen is low. Only five from all thirty transistors have higher I_{ON} at V_G=0.6 V if compared to the Ch Sym 1.

Lastly, we observe large spread in threshold voltage, which, for the 30 devices simulated here, spans around 120 mV. For the case without channel dopant (Fig. 3), the threshold voltage span is almost the same – around 130 mV. Additionally, the combined effect of surface roughness and channel dopant shows changes in the subthreshold slope. Again, this effect is more pronounced in the transistors with channel dopant in comparison to the nanowires than have only channel surface roughness.

The variations of the I_D-V_G characteristics can be analysed with reference to the behaviour of the electron density along the wire, potential along the wire and transmission coefficients. Fig. 2 shows the current flow of the Ch Sym and Ch Sym 1

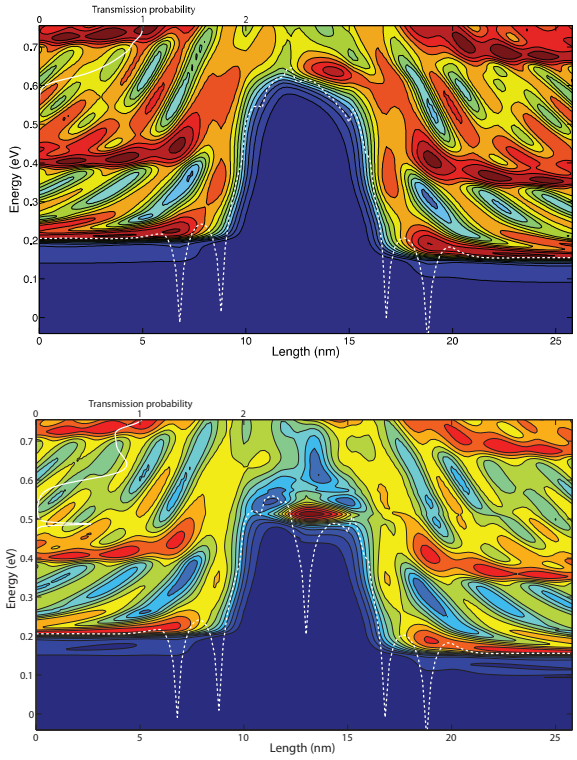

Fig. 9 Transmission probability (solid white line) and density of states along the wire for the Ch Sym (top) and Ch Sym 1 (bottom) case *with surface roughness* with the lowest I_{ON} for a gate voltage V_G = 0.0 V. The horizontal dashed white line is the electrostatic potential and it has been aligned to the first sub-band energy at the source.

transistors with the lowest I_{ON} at V_G=0.6 V. The J_X component of the current increases around the position of the discrete phosphorous atoms as if a funnel was created by the impurity potential and surface roughness. The current flow is directly correlated to the electron concentration and potential in the middle of the wire presented in Fig. 5 and Fig. 6. The electron concentration is perturbed by the channel surface roughness pattern and it is highest around the discrete dopants that have inverted sombrero shape of the potential.

Additionally, the variations of the current-voltage characteristics are analysed with reference to the behaviour of the transmission coefficients (Fig.7 and Fig. 8). At low gate bias of V_G = 0.0 V, introduction of *surface roughness* in a device with a single channel dopant is sufficient to raise the ground state of the transversal wave function, resulting in a step increase in transmission occurring at higher energies. For example, the first transmission peak for all SNWT transistors with *surface roughness* is shifted by around 0.05 eV from 0.45 eV for the Ch Sym 1 wire to 0.50 eV for all other devices (Fig. 8). This is reflected in the I_D-V_G characteristics where the current for all 'rough' devices is lower in comparison to the Ch Sym 1 transistor at 0.0 V gate voltage (Fig. 4).

A similar analysis is also performed at higher gate voltages (V_G = 0.5 V) – Fig. 8. At V_G=0.5V, the curves are more jagged and translated to lower energies relative to the same spectra at V_G=0.0V, due to increasing of scattering inside of the channel. The transmission coefficients indicate the presence of the Breit-Wigner- and Fano-type resonances. The width, position and the number of the resonant peaks and antiresonant dips depend on the profile of the surface roughness in combination with the discrete dopants in the SNWT. Those features are less pronounced at lower gate bias because of the dominant reflection of the carriers by the channel barrier potential.

Information supporting the latest statement is the distribution of the density of state (DOS) along the channel as presented in Fig. 9. The electrostatic potential is plotted with white dashed line. For both devices, Ch Sym and Ch Sym 1, the potential clearly shows the positions of the discrete dopants and the presence of channel surface roughness. The DOS is higher around the single dopant atoms and transmission function (plotted on the left-hand side of Fig. 9 with white solid line) has peaks corresponding to the channel dopant energy levels. Channel surface roughness could create quasi-bound states similar to those observed in the presence of discrete dopant.

IV. Conclusions

We have performed full 3D NEGF quantum transport simulations of the impact of precisely placed discrete phosphorous atoms and surface roughness on the operation of the all-gate-around silicon nanowire transistor (SNWT) in order to assess its potential application in digital circuits and systems.

All calculations presented in this work show the following common trends. Firstly, the I_{ON} that is critical for the circuit performance is worse for all transistors with discrete dopants and surface roughness considered in our study in comparison to the uniform doped devices. Secondly, we observe a subthreshold shift of approximately 130 mV and changes in the subthreshold slope for all single channel atom SNWT. Thirdly, the I_{OFF} for all single channel dopant devices with surface roughness is higher in comparison to the Smooth wire but lower relative to Ch Sym 1.

This paper shows the importance of quantum effects on the SNWT not only in terms of the threshold voltage shift and I_{ON} and I_{OFF} but also in terms of transport in the presence of surface roughness and ionized impurity scattering. Our results reveal a strong link and correlation between the undelaying microscopic structure of the SNWT and the devices performance, which plagues devices with small channel length.

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