Suppressed Carrier Clock for Reduction of Electromagnetic Radiated Emission from High-speed Digital System

Dong Gun Kam, Jonghoon Kim and Joungho Kim
KAIST (Korea Advanced Institute of Science and Technology)
Terahertz Interconnection and Package Lab., Div. of EE, Dept. of EECS,
373-1 Guseong, Yuseong, Daejeon 305-701, KOREA
kamdong@ieee.org; teralab@ee.kaist.ac.kr

Piljung Jun
Samsung Electronics co. LTD
System Development Group, Computer Division
416 Maetan-3, Paldal, Suwon, Kyungki, KOREA
pjjun@samsung.com

Abstract

In modern digital systems, most of electromagnetic radiated emission originates from high-speed digital clock signal. In order to reduce the electromagnetic radiated emission from the clock signal, spread spectrum clock had been used. It had been conventionally realized by modulating the period of a regular clock, using a phase locked loop (PLL) or a delay locked loop (DLL). However, neither of them can be implemented with simple circuit. To overcome this, suppressed carrier clock (SCC) has been recently proposed, which is implemented by intentionally skipping transitions of a regular clock.

In this paper, we analyze the effects of modulation profile on the suppression of electromagnetic radiated emission. Numerical simulation results show that saw-tooth modulation is an optimal method in terms of performance and feasibility. We also propose a simple circuit for modulation and demodulation of the SCC with the saw-tooth modulation profile. Finally, we implement the proposed circuit on an ALTERA chip, and it achieves 6 dB suppression of electromagnetic radiated emission.

Keywords

Suppressed Carrier Clock, Spread Spectrum Clock, Modulation Profile and EMI Reduction.

INTRODUCTION

In advanced microprocessors, most of electromagnetic radiated emission originates from high-speed digital clock signal because it is periodic with the highest frequency and its energy is concentrated on discrete frequency harmonics. Conventional electromagnetic interference (EMI) countermeasures include shielding, slew-rate limiting and filtering. However, as the clock frequency increases, these countermeasures become quite expensive to comply with enforced EMI regulation, such as FCC and CISPR. Therefore, the spread spectrum clock becomes more attractive.

A spread spectrum clock generator (SSCG) has been implemented by using either a phase locked loop (PLL) or a delay locked loop (DLL), where jitter is intentionally added to a regular clock for frequency modulation [1], [2]. This is similar to the spread spectrum technique widely used in communication systems, and effectively spreads the energy of discrete frequency harmonics over a wide range of frequencies. However, it is difficult to implement a PLL in the same die with high-speed digital logic. Thus, it should be implemented on a separated chip and assembled in a module. Even a DLL requires complex circuits and its core size typically exceeds 500um-by-500um for 0.35um CMOS process. Neither of them can be implemented with simple circuit.

To overcome this, suppressed carrier clock (SCC) has been recently proposed [3], [4]. It implements dual side-band suppressed carrier amplitude modulation, by intentionally skipping transitions of a regular clock. Since the basic concept of the SCC was introduced, there has been little analysis on how to implement and optimize it. In this paper, we analyze the SCC technique in detail by measurement and numerical simulation. First, we find that the saw-tooth modulation profile is an optimal method in terms of performance and feasibility. Second, we propose a simple circuit for modulation and demodulation of the SCC with the saw-tooth modulation profile. Finally, we implement the proposed circuits on an ALTERA chip, and it achieves 6 dB suppression of electromagnetic radiated emission.

SUPPRESSED CARRIER CLOCK (SCC)

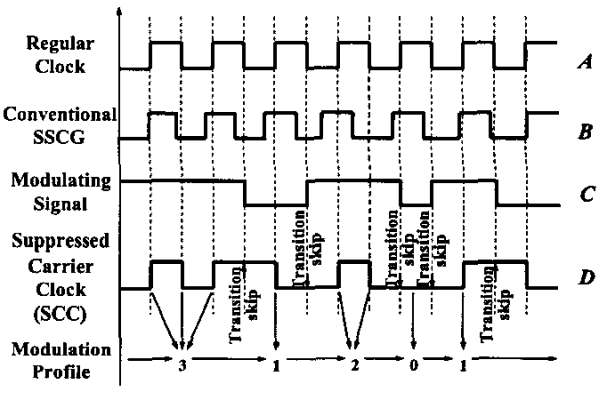

Figure 1. Conventional SSCG vs. proposed Suppressed Carrier Clock (SCC)

While conventional SSCGs are implemented by adding either period jitter or edge jitter to a regular clock, the SCC is realized by skipping transitions of the regular clock. Figure 1 illustrates the voltage waveforms of several kinds

of clocks in the time-domain. ***A*** is a regular clock and its period is fixed. ***B*** is a conventional spread spectrum clock implemented by the SSCG. It modulates the period of the regular clock (***A***) by injecting intentional jitter. ***D*** is the proposed SCC, which is the product of the regular clock (***A***) and the modulating signal (***C***). It should be noticed that the regular clock is alternately inverted, viz. transition-skipped at every rising edge and falling edge of the modulating signal. The modulation profile is defined as the sequence of the number of transitions between any two adjacent transition-skipped points.

The SCC modulation is similar to the amplitude modulation (AM) used for radio broadcasting. On the other hand, the carrier of the SCC modulation is not a sinusoidal wave but a square wave. The AM theory predicts that the power will appear in side bands around the fundamental clock frequency. That same theory also predicts that the side band shape will be determined by the spectral content of the modulating signal.

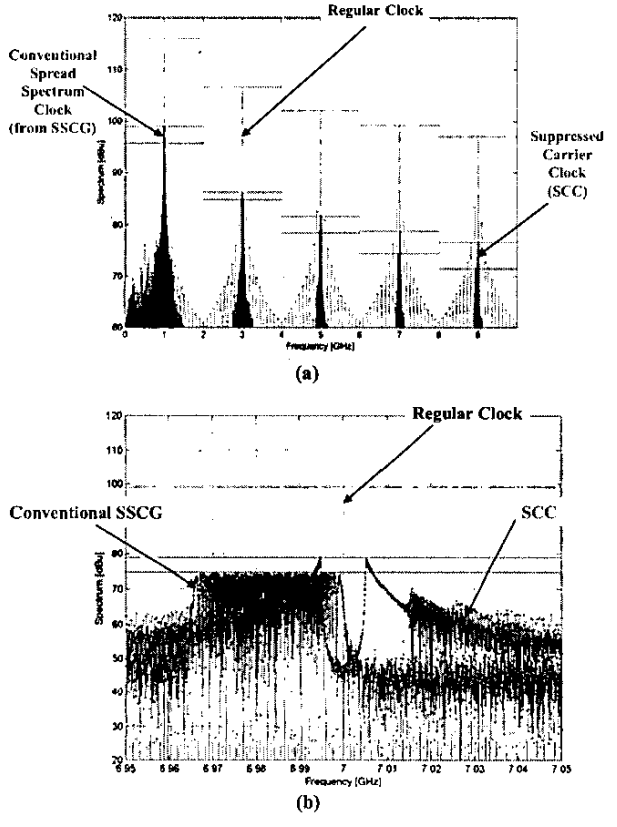

Figure 2. Conventional SSCG vs. proposed Suppressed Carrier Clock (SCC)

Figure 2-(a) shows the power spectrum of typical SCC, compared with a 1 GHz regular clock and a conventional spread spectrum clock generated by the SSCG. Figure 2-(b) is a power spectrum enlarged around the seventh harmonics. As expected from the AM theory, the SCC has no spectral content at the fundamental clock frequency and its harmonics. It has upper and lower side bands, which are similar in shape to the spectrum of the modulating signal. The SCC achieves more suppression of the power spectrum near the fundamental clock frequency than the conventional spread spectrum clock. However, it shows smaller decrease at higher frequencies due to considerable sub-peaks in the side band. As a result, the amount of suppression is relatively uniform up to the ninth harmonics when using the SCC.

MODULATION PROFILE

As mentioned earlier, the modulation profile is defined as the sequence of the number of transitions between any two adjacent transition-skipped points. The performance of the SCC is dependent on what kind of modulation profiles we use. Various modulation profiles are compared, including random pulse, sinusoidal, triangular, saw-tooth, and the SSCG modulation profile as shown in Figure 3. Numerical simulation results show that the saw-tooth modulation profile is an optimal method from the viewpoint of performance and feasibility.

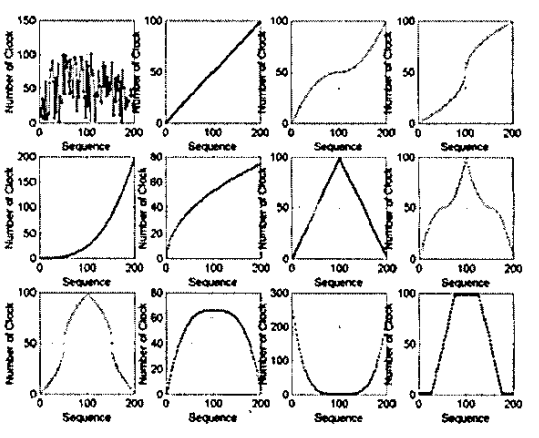

Figure 3. Various modulation profiles

Figure 4 shows the attenuation of the spectrum according to the various modulation profiles when a regular clock frequency, a modulation frequency and clock loss are 500 MHz, 50 kHz and 1 %, respectively. In other words, there are 10,000 clocks in one modulation period and every 50^{th} transition is skipped. It is also found that irregular skipped-transition point is more efficient to reduce spectrum. This is defined as the "offset" in the right figure. When we use {50, 50, 50 ...} as a modulation profile, viz. zero offset, the attenuation is about 9 dB. However, as we apply bigger offset like {1, 2, 3... 100}, the attenuation increases to 18 dB. This makes the saw-tooth modulation profile one of the most efficient modulation profiles.

Any non-linear modulation profiles having big offset can be as efficient as or more efficient than the saw-tooth modulation profile. However, it was found by numerical

simulation that there is little difference in attenuation of spectrum among them. Therefore, the saw-tooth modulation profile is an optimal method because it is easier to implement than any non-linear modulation profiles.

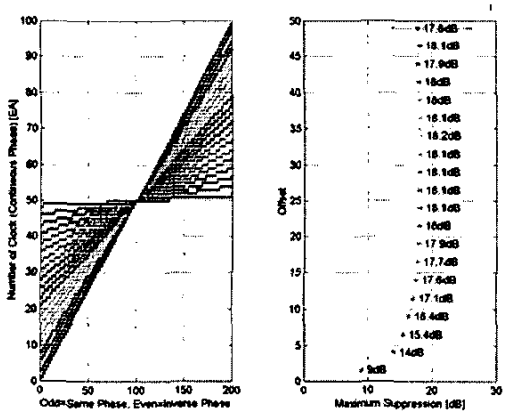

Figure 4. Attenuation of spectrum according to modulation profile

SCC MODULATOR AND DEMODULATOR

To realize the saw-tooth modulation profile, we propose a simple SCC modulator/demodulator. As shown in Figure 5, the modulator is composed of a multiplexer, an inverter and a modulation controller. A glitch is an error condition where a digital gate will transition momentarily from one logic state to the other and back again. Glitches in digital clocks are likely to cause system failure and this must be prevented. Figure 6 shows a multiplexer design that is better than a stand-alone XOR gate.

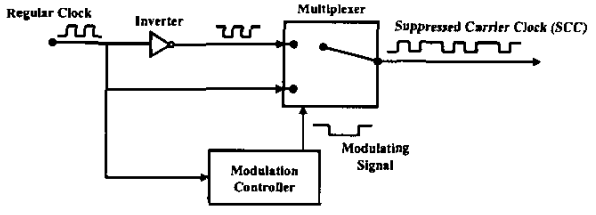

Figure 5. SCC Modulator

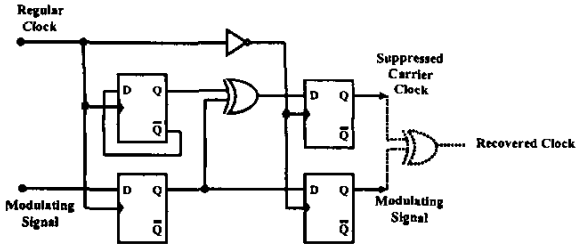

Figure 6. Glitch-free multiplexer

The modulation controller determines the modulation profile. In order to generate the saw-tooth modulation profile, it should be composed of a multiplexer, an adder, a comparator, a divider and a resister as shown in Figure 7. If initial values for the multiplexer, the adder and the comparator are 1, 2 and 11, respectively, the register's value becomes 1, 3, 5, 7, 9, and 11 in sequence. Any increasing arithmetic series can be implemented with this configuration. The divider can be used for making the series of repeated numbers like 1, 1, 3, 3, 5, 5 ... The down-counter reads the register's value and count from it to 0. Whenever the down-counter's value becomes 0, the glitch-free multiplexer switches the path. In this way, the SCC can be implemented. Furthermore, the modulation controller can be simply implemented with an up-counter as shown in Figure 8. Figure 9 shows the proposed SCC demodulator, by which the original regular clock can be recovered even without knowing the modulating signal.

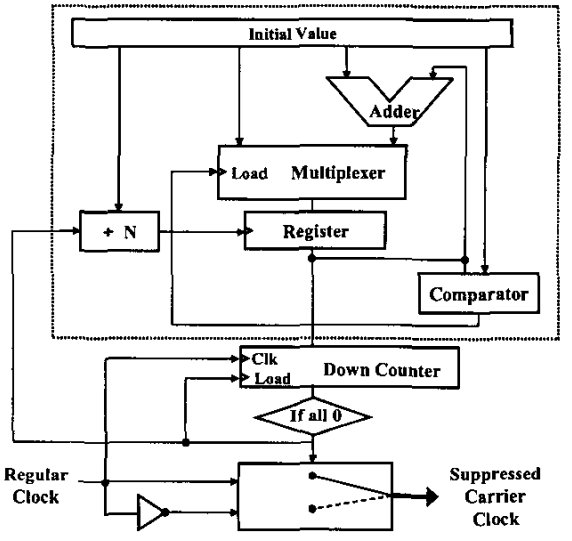

Figure 7. Saw-tooth modulation profile generator I

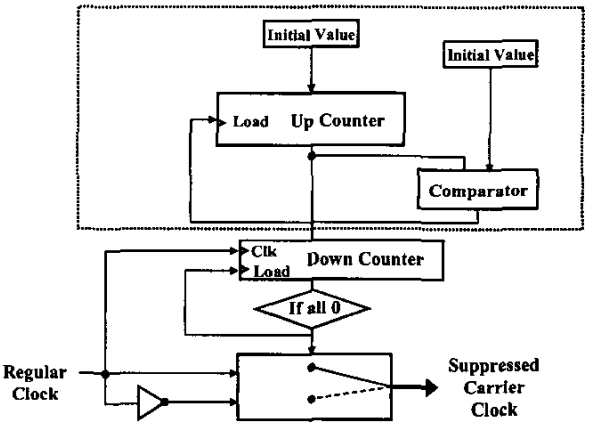

Figure 8. Saw-tooth modulation profile generator II

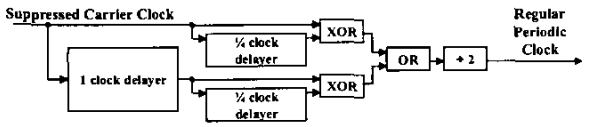

Figure 9. SCC demodulator

ON-CHIP IMPLEMENTATION AND MEASUREMENT

Finally, we successfully verified the proposed circuits by measurement. As shown in Figure 10, we realized the SCC with the saw-tooth modulation profile by using an ALTERA chip (EPM3128). The modulated clock was connected to a digital oscilloscope and a spectrum analyzer. It was successfully demonstrated that the saw-tooth modulation profile was generated and the peak power spectral density was considerably reduced as shown in Figure 11.

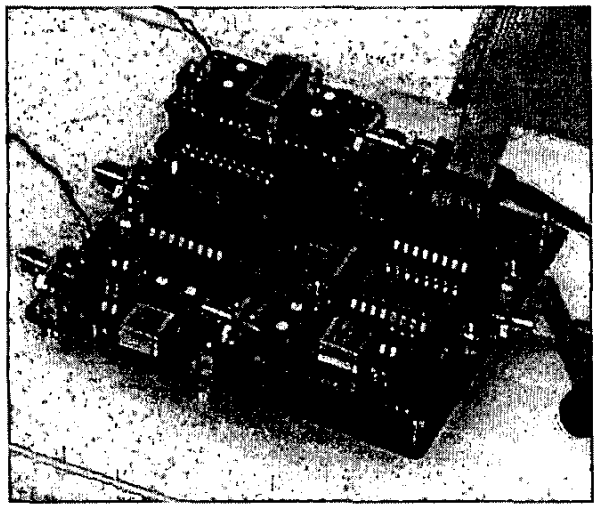

Figure 10. On-chip implementation of the proposed SCC

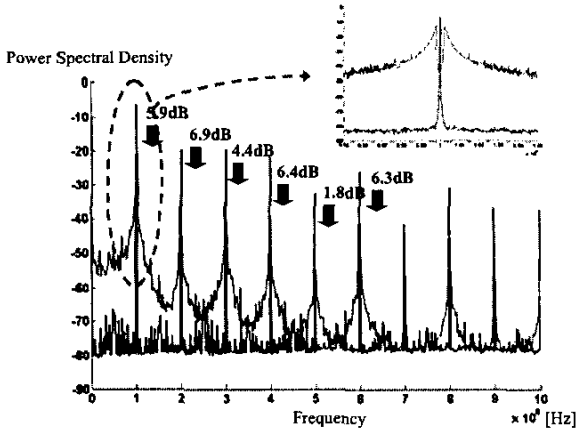

Figure 11. Measured power spectral density by using the proposed SCC

CONCLUSIONS

In order to reduce electromagnetic interference (EMI), the Suppressed Carrier Clock (SCC) was implemented by skipping transitions of a regular clock signal intentionally. We found that a saw-tooth modulation profile is optimal in terms of performance and feasibility. We proposed a simple SCC modulator and demodulator according to the saw-tooth modulation profile. Finally, we implemented the proposed circuits on a chip, and found that it achieves a 6 dB suppression of peak power spectral density.

REFERENCES

[1] K. Hardin, J. Fessler, and D. Bush, "Spread spectrum clock generation for the reduction of radiated emissions," IEEE International Symposium on Electromagnetic Compatibility, 1994, pp. 227 -231.

[2] Y. Moon, D. Jeong, and G. Kim, "Clock dithering for electromagnetic compliance using spread spectrum phase modulation", IEEE International Solid-State Circuits Conference, 1999, pp. 186-187.

[3] I. Greiss, "Digital modulated clock circuit for reducing EMI spectral density," United States Patent, No. 5,731,728, 1998.

[4] D. Arnett, "Suppressed carrier digital clocks," IEEE International Symposium on Electromagnetic Compatibility, 1999, pp. 816-821.

[5] J. Kim, P. Jun, J. Byun, and J. Kim, "Design guidelines of spread spectrum clock for suppression of radiation and interference from high-speed interconnection line," IEEE Workshop on Signal Propagation on Interconnects, 2002, pp. 189-192.