Modeling and Controller Design of Non Ideal Z-Source Converter

M. A. Ismeil[1,3], A. Kouzou[2,3], Ralph Kennel[3], A. A. Ibrahim[1], M. Orabi[1] and M. E. Ahmed[1]

[1]Electrical Department, Faculty of Engineering, South Valley University, 81542 Aswan, Egypt.

[2]Electrical Department, Djelfa University, Ain Chih BP 3117, Djelfa, Algeria

[3]Department of Electrical Drive Systems and Power Electronics, Technical University of Munich,80333 Munich, Germany

Phone/Fax number:+49 89 289 28336, e-mail: **mohamed.ali@tum.de**;**ralph.kennel@tum.de**

Abstract. This paper deals with the study of the non-ideal Z-Source inverter where the inductors and capacitors resistance are taken into account, while the main aim of the Z-source inverter for performing voltage buck and boost capabilities using a unique impedance network between the power source and converter circuit is guarded. In this paper an average model for the Z-Source inverter using state space averaging is proposed. Then, the behaviors of the studied system is analyzed based on the stability of the presented model, this analyze leads to the design of the suitable controller to be used to ensure the stability of the presented model. Finally the average model analyze is verified by simulation results.

Key words

State space averaging, small signal model, Z-source.

1. Introduction

Actually there is a very significant interest in grid connected systems of renewable energy sources, especially PV sources, these system are basically power electronics converters, where the main target in these applications research is to minimize the cost and to improve their efficiency. Contrary to the classical structures, the use of one stage instead of two stages and removing the transformer from AC side if it is used will decrease drastically the cost of PV system interface for grid connection [1]. Three-phase voltage-source pulse width modulation (PWM) inverters have been widely used for DC/AC power conversion because they can produce a variable voltage and variable frequency power. In the same time a lot of control strategies have been used to fulfill the aforementioned requirements and to improve the quality of the output voltage of the three phase inverter, On the other hand these inverters need dead time to avoid the arm-short and snubber circuits to suppress the switching spikes [2].

In 2002, the topology of the Z-source inverter was proposed as an alternative solution to overcome the limitations of traditional inverter such as the boosting mode and the problems of short circuit [3]. The idea of this topology is based on building an impedance network (Z network) which is used to replace the traditional DC link as shown in Fig. 1. Therefore; an additional zero state will appear following to the leg shoot- through of one phase, two phases or three phases, this case is not allowed in the control strategy of the traditional inverter. On the other side, this alternative topology gives more flexibility and allows boosting the voltage across the DC-Link bus. In addition, the reliability of the inverter is greatly improved because the uncontrolled shoot through caused by electromagnetic interference (EMI) noises which can destroy the inverter circuitry will be no longer faced. Thus, this solution provides a low-cost, reliable, and highly efficient single-stage structure for buck and boost power conversion [4]. Indeed, a lot of papers present the modeling and the controller design of Z-source with ignoring the parasitic elements [5-10]**.**
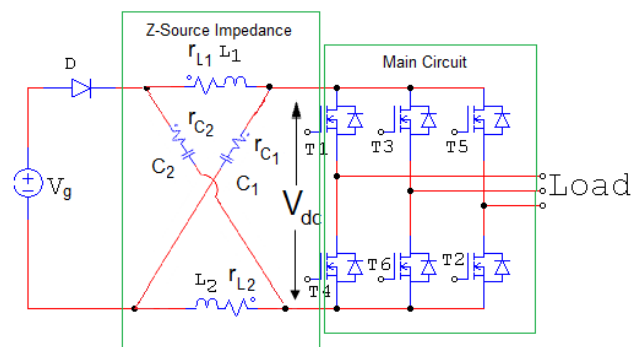

Fig. 1 Z-Source Inverter

2. State Space Averaging

As shown in Fig. 2 Z- Source has an X shape LC impedance network between the DC source and the inverter. Where r_{L1}, r_{L2} are parasitic resistances of inductors, and r_{C1}, r_{C2} are parasitic resistance of capacitors. The input diode is added to prevent reverse flow of current.

This structure of Z source inverter can be operating in shoot- through or non-shoot- through state [3, 11]. Where, its output voltage can be boosted or bucked.
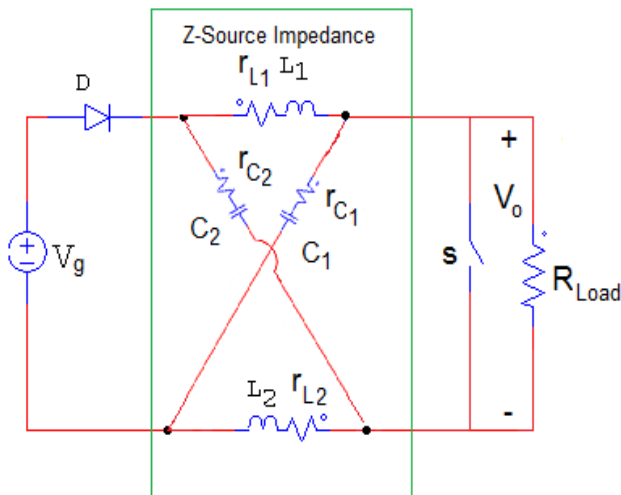

Fig. 2 DC equivalent circuit of Z source inverter

A. Shoot- Through Mode

The first state occurs when two switches in one leg are turned; this case is not allowed in the inverter classical controls strategies, so the switch S is turned on as shown in Fig. 3, the following assumptions are taken into account for all modes:

$$L_1 = L_2 = L$$
$$C_1 = C_2 = C$$
$$r_{L1} = r_{L2} = r_L$$
$$r_{C1} = r_{C2} = r_C$$

The shoot-through state equations can then be written in matrix form as follows:

$$\begin{bmatrix} L\dfrac{di_{L1}}{dt} \\ L\dfrac{di_{L2}}{dt} \\ C\dfrac{dv_{C1}}{dt} \\ C\dfrac{dv_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} -(r_C + r_L) & 0 & 1 & 0 \\ 0 & -(r_C + r_L) & 0 & 1 \\ 0 & -1 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} \quad (1)$$

Where: i_{L1} and i_{L2} are inductor currents for L_1 and L_2, v_{C1} and v_{C2} are capacitor voltage for C_1 and C_2 respectively.
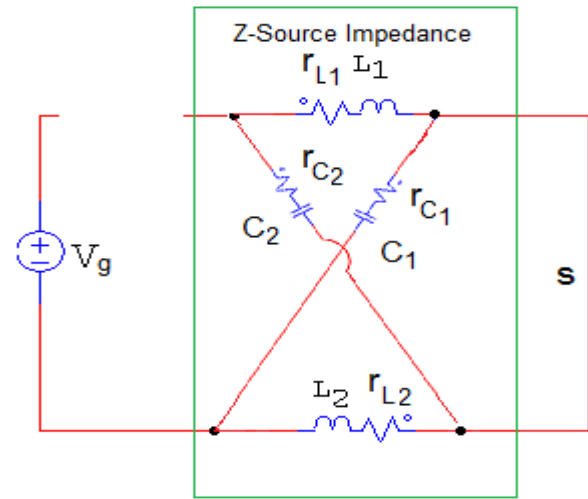

Fig. 3 Z source shoot-through state

B. Non shoot- Through Mode

In this state the inverter bridge becomes an equivalent resistive load when it is in one of the six active states or in one of the two traditional zero state (i.e. an open circuit). Therefore, we can get a uniform equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in one of the eight non shoot-through switching states. During this state the switch S is turned OFF as shown in Fig. 4. The input diode is forward biased, allowing the Z-source inverter to assume the conventional VSI active or null states.
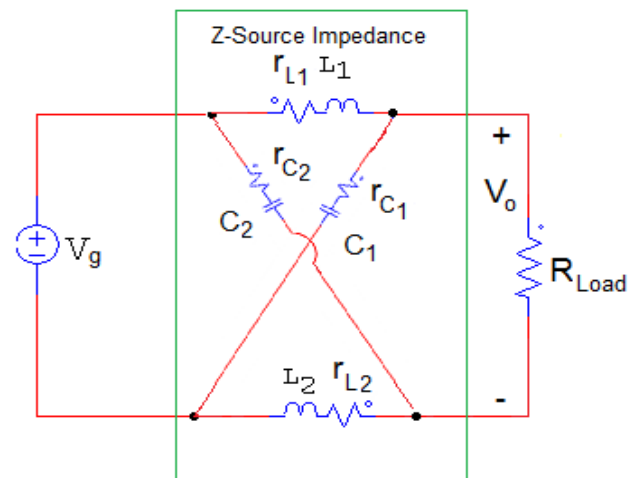

Fig. 4 Z source non shoot-through state

In this mode the relation between the input voltage, capacitor voltage and the inductance voltage can be presented by the following state equation:

$$\begin{bmatrix} L\dfrac{di_{L1}}{dt} \\ L\dfrac{di_{L2}}{dt} \\ C\dfrac{dv_{C1}}{dt} \\ C\dfrac{dv_{C2}}{dt} \end{bmatrix} = A_1 \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} V_g + \dfrac{V_o(r_C)}{R_{Load}} \\ V_g + \dfrac{V_o(r_C)}{R_{Load}} \\ -\dfrac{V_o}{R_{Load}} \\ -\dfrac{V_o}{R_{Load}} \end{bmatrix} \qquad (2)$$

Where:

$$A_1 = \begin{bmatrix} -(r_C + r_L) & 0 & 0 & -1 \\ 0 & -(r_C + r_L) & -1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}$$

An average model for non ideal Z source Inverter can be written as:

$$\begin{bmatrix} L\dfrac{di_{L1}}{dt} \\ L\dfrac{di_{L2}}{dt} \\ C\dfrac{dv_{C1}}{dt} \\ C\dfrac{dv_{C2}}{dt} \end{bmatrix} = A_2 \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} V_g + \dfrac{V_o(r_C)}{R_{Load}} \\ V_g + \dfrac{V_o(r_C)}{R_{Load}} \\ -\dfrac{V_o}{R_{Load}} \\ -\dfrac{V_o}{R_{Load}} \end{bmatrix} \qquad (3)$$

Where:

$$A_2 = \begin{bmatrix} -(r_C + r_L) & 0 & D & -D' \\ 0 & -(r_C + r_L) & -D' & D \\ -D & D' & 0 & 0 \\ D' & -D & 0 & 0 \end{bmatrix}$$

where T_o and $D = \dfrac{T_o}{T}$ represent the switch ON time and the corresponding duty ratio, while T_{off} and $D' = \dfrac{T_{off}}{T}$ represent the switch OFF time corresponding duty ratio. By insertion small signalin previous equation (3) can be rewritten as follows:

$$\begin{bmatrix} L\dfrac{d(I_{L1} + \hat{i}_{L1})}{dt} \\ L\dfrac{d(I_{L2} + \hat{i}_{L2})}{dt} \\ C\dfrac{d(V_{C1} + \hat{v}_{C1})}{dt} \\ C\dfrac{d(V_{C2} + \hat{v}_{C2})}{dt} \end{bmatrix} = A_2^{small} \begin{bmatrix} I_{L1} + \hat{i}_{L1} \\ I_{L2} + \hat{i}_{L2} \\ V_{C1} + \hat{v}_{C1} \\ V_{C2} + \hat{v}_{C2} \end{bmatrix} + B_2^{small} \quad (4)$$

Where:

$$A_2^{small} = \begin{bmatrix} -(r_C + r_L) & 0 & (D+\hat{d}) & -(1-(D+\hat{d})) \\ 0 & -(r_C + r_L) & -D' & D \\ -(D+\hat{d}) & (1-(D+\hat{d})) & 0 & 0 \\ (1-(D+\hat{d})) & -(D+\hat{d}) & 0 & 0 \end{bmatrix}$$

$$B_2^{small} = \begin{bmatrix} (1-(D+\hat{d}))\left((V_g + \hat{v}_g) + \dfrac{(V_o + \hat{v}_o)(r_C)}{R_{Load}}\right) \\ (1-(D+\hat{d}))\left((V_g + \hat{v}_g) + \dfrac{(V_o + \hat{v}_o)(r_C)}{R_{Load}}\right) \\ -(1-(D+\hat{d}))\dfrac{(V_o + \hat{v}_o)}{R_{Load}} \\ -(1-(D+\hat{d}))\dfrac{(V_o + \hat{v}_o)}{R_{Load}} \end{bmatrix}$$

Where $\hat{i}_L, \hat{v}_C, \hat{v}_g, \hat{v}_o, \hat{d}$ is the AC small signal value for inductor current, capacitor voltage , input voltage, output voltage of Z source impedance and duty ratio respectively.
$I_{L1}, I_{L2}, V_{C1}, V_{C2}, D$ and V_g are DC steady state values across inductor L_1, L_2, voltage across capacitor C_1, C_2, duty ratio, and input voltage respectively.

when no perturbations are applied, the small signals will be omited, hence the DC steady state equations at the operation point can be expressed as:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = A_2^{DC} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \end{bmatrix} + \begin{bmatrix} \dfrac{D'(r_C)}{R_{Load}} \\ \dfrac{D'(r_C)}{R_{Load}} \\ -\dfrac{D'}{R_{Load}} \\ -\dfrac{D'}{R_{Load}} \end{bmatrix} V_o + \begin{bmatrix} D' \\ D' \\ 0 \\ 0 \end{bmatrix} V_g \qquad (5)$$

Where:

$$A_2^{DC} = \begin{bmatrix} -(r_C + r_L) & 0 & D & -D' \\ 0 & -(r_C + r_L) & -D' & D \\ -D & D' & 0 & 0 \\ D' & -D & 0 & 0 \end{bmatrix}$$

By considering the small change,the small signal AC state equation become as follows:

$$\begin{bmatrix} L\dfrac{d\hat{i}_{L1}}{dt} \\ L\dfrac{d\hat{i}_{L2}}{dt} \\ C\dfrac{d\hat{v}_{C1}}{dt} \\ C\dfrac{d\hat{v}_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} -(r_C + r_L) & 0 & D & -D' \\ 0 & -(r_C + r_L) & -D' & D \\ -D & D' & 0 & 0 \\ D' & -D & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix}$$

$$+\begin{bmatrix} \dfrac{D'(r_c)}{R_{Load}} \\ \dfrac{D'(r_c)}{R_{Load}} \\ -\dfrac{D'}{R_{Load}} \\ -\dfrac{D'}{R_{Load}} \end{bmatrix}\hat{v}_o + \begin{bmatrix} D' \\ D' \\ 0 \\ 0 \end{bmatrix}\hat{v}_g + \begin{bmatrix} V_{C1}+V_{C2}-V_g-\dfrac{V_o r_C}{R_{Load}} \\ V_{C1}+V_{C2}-V_g-\dfrac{V_o r_C}{R_{Load}} \\ -I_{L1}-I_{L2}+\dfrac{V_o}{R_{Load}} \\ -I_{L1}-I_{L2}+\dfrac{V_o}{R_{Load}} \end{bmatrix}(\hat{d}) \quad (6)$$

The application of the Laplace transformation on (6), the small-signal expression for the inductor voltage expression of the inductance L_1 is deduced:

$$sL\hat{i}_{L1}(s)=-(r_L+r_C)\hat{i}_{L1}(s)+D\hat{v}_{C1}(s)-D'\hat{v}_{C2}(s)+D'\hat{v}_g(s)$$

$$-\left(V_{C1}+V_{C2}-V_g-\frac{V_o r_C}{R_{Load}}\right)\hat{d}(s)+\left(\frac{D'r_C}{R_{Load}}\right)\hat{v}_o(s)$$
$$(7)$$

On the other side, the small-signal expression of the inductor voltage across the inductor L_2 is expressed as follows:

$$sL\hat{i}_{L2}(s)=-(r_L+r_C)\hat{i}_{L2}(s)-D'\hat{v}_{C1}(s)+D\hat{v}_{C2}(s)+D'\hat{v}_g(s)$$
$$-\left(V_{C1}+V_{C2}-V_g-\frac{V_o r_C}{R_{Load}}\right)\hat{d}(s)+\left(\frac{D'r_C}{R_{Load}}\right)\hat{v}_o(s) \quad (8)$$

According (8) the small signal expression of the current across the capacitor C_1 can be expressed as follows:

$$Cs\hat{v}_{C1}(s)=-D\hat{i}_{L1}(s)+D'\hat{i}_{L2}(s)-\left(\frac{D'}{R_{Load}}\right)\hat{v}_o(s)$$

$$+\left(-I_{L1}-I_{L2}+\frac{V_o}{R_{Load}}\right)\hat{d}(s) \quad (9)$$

Whereas, the small signal expression of the current across capacitor C_2 can be expressed as follows:

$$Cs\hat{v}_{C2}(s)=D'\hat{i}_{L1}(s)-D\hat{i}_{L2}(s)-\left(\frac{D'}{R_{Load}}\right)\hat{v}_o(s)$$

$$+\left(-I_{L1}-I_{L2}+\frac{V_o}{R_{Load}}\right)\hat{d}(s) \quad (10)$$

Due to the similarty between the components of the Z impedence , the following simplification can be applied without any effect or modification of the ideal behaviours of the Z-source:

$$\hat{v}_{C1}(s)=\hat{v}_{C2}(s)=\hat{v}_C(s)$$
$$I_{L1}=I_{L2}=I_L, V_{C1}=V_{C2}=V_C$$

Using (7),(8),(9) and (10) the following expression is deduced:

$$\left(Cs+\frac{(D-D')^2}{(Ls+r_C+r_L)}\right)\hat{v}_C(s)=K_2\hat{d}(s)+\left(\frac{D'(1-2D)}{Ls+r_C+r_L}\right)\hat{v}_g(s)$$

$$-\left(\frac{D'r_C}{R_{Load}}+\left(\frac{D'r_C}{(Ls+r_C+r_L)R_{Load}}\right)(1-2D)\right)\hat{v}_o(s) \quad (11)$$

Where:

$$K_2=\left(-2I_L+\frac{V_o}{R_{Load}}\right)+\frac{\left(V_C-V_g-\dfrac{V_o r_C}{R_{Load}}\right)^2}{(Ls+r_C+r_L)}(1-2D)$$

Finally, the transfer functions expressions of the capacitor voltage to the input voltage and the shoot through duty ratio is deduced and can be presented as follows.

$$G_{vcg}=\left.\frac{\hat{v}_c(s)}{\hat{v}_g(s)}\right|_{\hat{v}_o(s)=\hat{d}(s)=0}=\left(\frac{D'(1-2D)}{Cs(Ls+r_C+r_L)+(D-D')^2}\right)$$
$$(12)$$

$$G_{vcd}=\left.\frac{\hat{v}_c(s)}{\hat{d}_g(s)}\right|_{\hat{v}_o(s)=\hat{v}_g(s)=0}$$

$$=\left(\frac{(Ls+r_C+r_L)\left(\dfrac{V_o}{R_{Load}}-2I_L\right)+\left(2V_C-V_g-\dfrac{V_o r_C}{R_{Load}}\right)(1-2D)}{Cs(Ls+r_C+r_L)+(D-D')^2}\right)$$
$$(13)$$

When there is no distrubance in the capacitor voltage and the duty ratio, the transfer functions expressions of the output voltage to the input voltage and the shoot through duty ratio can be presented respectively as follows:

$$G_{vog}=\left.\frac{\hat{v}_o(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=\hat{v}_C(s)=0}$$

$$=\frac{\left(\dfrac{D'(1-2D)}{Ls+r_C+r_L}\right)}{\left(\dfrac{D'r_C}{R_{Load}}+\left(\dfrac{D'r_C}{(Ls+r_C+r_L)R_{Load}}\right)(1-2D)\right)} \quad (14)$$

$$G_{vod}=\left.\frac{\hat{v}_c(s)}{\hat{d}_g(s)}\right|_{\hat{v}_C(s)=\hat{v}_g(s)=0}$$

$$=\left(\frac{(Ls+r_C+r_L)\left(\dfrac{V_o}{R_{Load}}-2I_L\right)+\left(2V_C-V_g-\dfrac{V_o r_C}{R_{Load}}\right)(1-2D)}{\left(\dfrac{D'r_C(Ls+r_C+r_L)}{R_{Load}}+\dfrac{D'r_C(1-2D)}{R_{Load}}\right)}\right)$$
$$(15)$$

It possible to clarify the presence of RHP zero at boosting mode when $2I_L < \dfrac{V_o}{R_{Load}}$, where the first term in the numerator of (13) and (15) becomes negative.

TABLE 1 Z- Source Inverter Parameter

Parameter	Value
V_g	150V
I_{Load}	10A
C	1mF
L	5mH
r_C	0.03Ω
r_L	0.5Ω
D	0.3

From DC equation (5)

$$-DI_{L1} + D'I_{L2} - \left(\frac{D'}{R_{Load}}\right)V_o = 0 \qquad (16)$$

$$-D'I_{L1} + DI_{L2} - \left(\frac{D'}{R_{Load}}\right)V_o = 0 \qquad (17)$$

From *DC* equation (5)

$$0 = -(r_L + r_C)I_{L1} + DV_{C1} - D'V_{C2} + D'V_g + \left(\frac{D'r_C}{R_{Load}}\right)V_o \qquad (18)$$

$$0 = -(r_L + r_C)I_{L2} - D'V_{C1} + DV_{C2} + D'V_g + \left(\frac{D'r_C}{R_{Load}}\right)V_o \qquad (19)$$

From (16) and (17) the inductors currents can be calculate: equal

$$I_{L1} = I_{L2} = 17.5A$$

From (18) and (19) the capacitors voltages can be calaculated:

$$V_{C1} = V_{C2} = 239.8375V$$

The system is unstable because of the RHP Zero. the design of a feedback with an adequate phase margin becomes more difficult when RHP zeros appear in the transfer function. For example, for a fixed shoot D=0.3, the bode diagram of duty ratio to-capacitor-voltage transfer function with parametric sweep of C is shown in Fig. 5, It is obvious that the system has a large DC gain (57.4db), in the same time crossover frequency changes with the change of the capacitor value, while the system remains unstable.
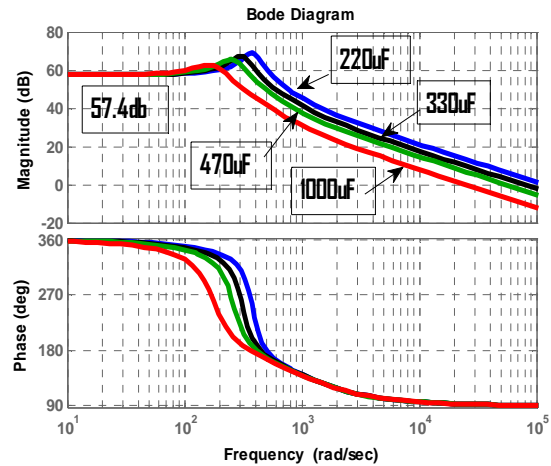

Fig. 5 Bode Plot of Transfer Function G_{vcd}, Z Source with Different Capacitances

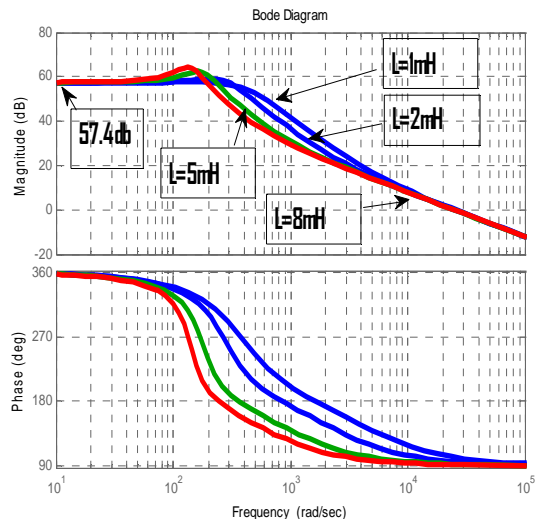The poles position changes following to the inductor value as shown in Fig. 6.

Fig. 6 Bode Plot of Transfer Function G_{vcd}, Z Source with Different Inductance
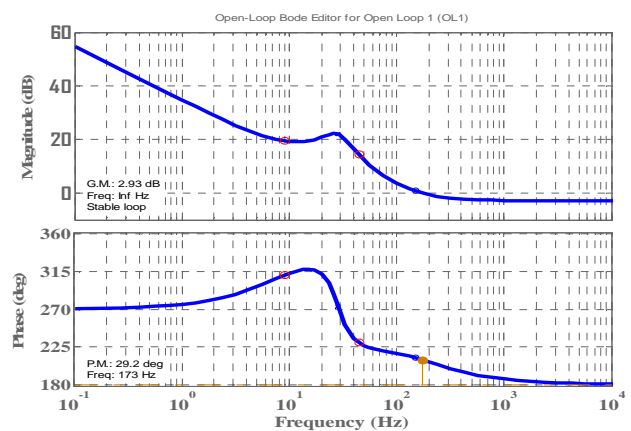

Fig. 6. Bode plot of transfer function after adding compensation

The parameters listed in Table 1 allow the appearance of two poles at 165 rad/sec and a zero at 948 rad/sec. It is clear that if a PID controller is used, it has to be designed so that two zeros can be added near the two pole, where the integrator has to achieve the increase of the DC gain
The crossover frequency is 173 Hz and the phase margin is 29.2deg.

3. Conclusion

In this paper, a complete study based on small signal analysis of the Z- source inverter with classical structure is presented, where the inductors and the capacitors resistances of Z-source network are taken into account. This study is based on a mathematical model which is developed and analyzed, on the other side this study is focusing mainly on the effect of the non-ideal parameters on the behaviors of the Z-source network, especially on the stability of the system, to achieve this an investigation using the bode diagram plot is performed. Finally, based on this study the synthesis and the design of the appropriate controller which will be used to ensure the stability of the system can be achived.

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