DIGITAL LOCK-IN TECHNIQUES FOR ADAPTIVE POWER-LINE INTERFERENCE EXTRACTION

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This paper presents a simple digital approach for adaptive power-line (PL) (or other periodical) interference extraction. By means of two digital square (or sine) wave mixers the real and imaginary part of the interference are found and thus the interference waveform is synthesized and subtracted. The described technique can be implemented in open-loop architecture where the interference is synthesized as a complex sinusoid or in closed-loop architecture for automated phase and gain control. The same approach can be used for removal of fundamental frequency of the PL interference as well as its higher harmonics. It is suitable for real-time operation with popular low-cost microcontrollers.

Keywords: power line interference, mixer, balanced demodulator, synchronous detector, phase-sensitive switch, lock-in amplifier

1. INTRODUCTION

Power-line (PL) interference (hum) is a common problem in almost all biosignal acquisition applications. Because the body serves as a capacitively coupled antenna, a part of the picked PL interference currents traverse the electrodes and produce a common mode voltage over an amplifier common mode input impedance. Even when special signal recording techniques are applied (shielding, driven right leg, body potential driving etc.), some AC noise remains as a consequence of electrode impedance imbalance and/or due to finite value of the amplifier CMRR [1]. A further reduction of the interference should be implemented by either post-digital or post-analog filters.

A first option for interference removal is to include analog or digital notch post-filters in the signal path. Unfortunately these filters distort the desired signal as well as remove the interference [2]. To minimize signal loss the high-Q switched capacitor filters tracked to the PL frequency by additional PLL circuit could be implemented [3].

Other option is to use low-pass averaging digital filters with firs zero at the PL frequency [4]. Because of introduced additional signal bandwidth limitation these filters significantly attenuate important frequency components.

Next approach, based mainly on a property of the ECG signal to have linear regions, is a subtraction procedure [5, 6]. With great advantage to reject all harmonics of the PL frequency, the procedure is suitable mainly for ECG and is inapplicable over biosignals without linear segments.

Other modern approach for interference minimization is by adaptive noise cancellation [7]. Adaptive filters remove the interference using reference input. They minimize the total output power and thus minimize the output noise power. Since the signal in the output remains constant, minimizing total output power minimizes the interference. Frequently these filters use LMS (Least-Mean-Squares) algorithm and cannot follow fast changes in the interference amplitude or phase.

Finally global filters reduce the PL interference in a frequency domain (FFT) and are not suitable for real-time implementation [8].

Although in presence of many different approaches, the problem of interference removal still exists and the researchers continue to find a simple and ultimate solution resulting to 'high fidelity' and 'clean' records.

This paper presents a simple digital lock-in technique for PL (or other periodical) interference extraction. By means of square-wave (or sine-wave) digital mixers the real and imaginary (amplitude and phase) part of the interference are found and thus the interference waveform is synthesized and subtracted. The same approach can be used for removal of fundamental frequency of the PL interference as well as its higher harmonics.

2. LOCK-IN CONCEPT

Lock-in techniques are used from many years especially for frequency conversion (frequency shifting) in telecommunications and in analog or digital lock-in amplifiers [9, 10]. They are widely used also in auto-zeroed (chopper) amplifiers for reduction of low-frequency noise (1/f) and offset as well as in any low-level signal conditioning sensor applications such as Hall-effect sensors, infrared (PIR) sensors etc.

In a nutshell, by lock-in approach an amplitude and phase of a low-level (nano or micro voltage range) sinusoidal signal can be measured.

The mixer (multiplier, balanced demodulator, synchronous detector, phase-sensitive detector) is the main building block in any lock-in system [11]. Each mixer simply is a linear multiplier which output is a product of two signals – one is the signal of interest and the other is a reference.

In dependence on the reference signal waveform, two types of mixers are used: sine wave mixers and square wave (switching type) mixers. The great advantages of switching type mixers are their simplicity and easy way to make linear multipliers over a very wide range of input signals. The drawback is that square wave, used as a reference, contains odd harmonics of the fundamental frequency and after mixing these harmonics produce large number of sum and difference frequencies which are detected [12].

If the higher harmonics are ignored, and the reference (f_R) and input (f_I) frequencies are equal, the mixer output contains a phase-sensitive DC voltage and a component which is twice the reference frequency ($2f_R$). The $2f_R$ component should be strongly attenuated by a low-pass post-filter (LPF) with appropriate settling time [13]. Although the sine wave mixing is more accurate, in practice the square wave is preferable due to its simple realization.

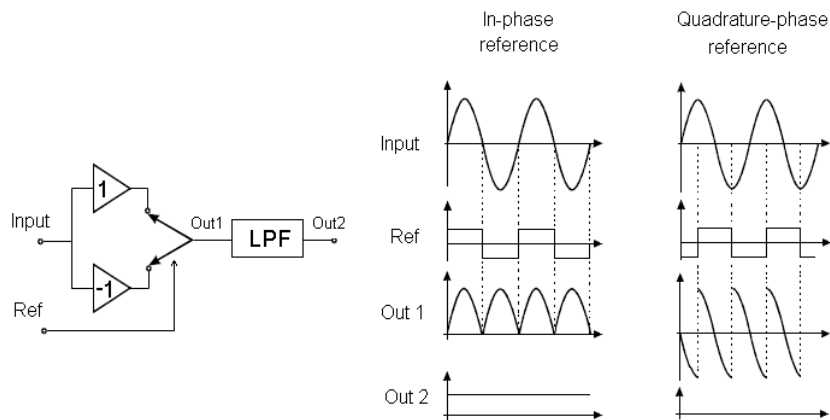The basic operation of square wave mixer (phase-sensitive switch) is shown in fig.1.

Fig. 1 Basic operation of square wave mixer

Assuming that the phase difference between f_R and f_I is zero then the in-phase mixer output is a full-wave rectified sinusoid. After low-pass filtering the average value of this waveform is $2V_m/\pi$, where V_m is the amplitude of the rectified sine wave. In the same time for quadrature output, the mean value is zero.

Generally, if the input signal has phase difference θ then the average value at the in-phase output is:

$$V_{Re} = V_m \frac{2}{\pi} \cos\theta$$

and the average value at the quadrature-phase output is:

$$V_{Im} = -V_m \frac{2}{\pi} \sin\theta$$

For these two equations the V_m and θ can be found:

$$V_{Im} = \frac{\pi}{2}\sqrt{V_{Re}^2 + V_{Im}^2} \text{ and } \theta = \tan^{-1}\left(-\frac{V_{Im}}{V_{Re}}\right)$$

So the needed interference parameters as a pure sine wave are found and the interference could be synthesized and subtracted.

2.1 Open-loop architecture for interference extraction

Let's express the PL interference (V_I) as a simple sine wave:

$V_I = V_m \sin(\omega t + \theta)$, using a basic trigonometric identity:

$\sin(\omega t + \theta) = \sin(\omega t)\cos\theta + \cos(\omega t)\sin\theta$, the equation for V_I can be rewritten as:

$V_I = V_m \sin(\omega t + \theta) = \frac{\pi}{2}V_{Re}\sin(\omega t) - \frac{\pi}{2}V_{Im}\cos(\omega t)$

The consequence is that the interference V_I could be synthesized by sum of sine and cosine waves, as shown in fig. 2. The advantage of this architecture is that it is an open-loop, simple and unconditionally stable system. But it is perfect only if the PL frequency and interference have no difference.
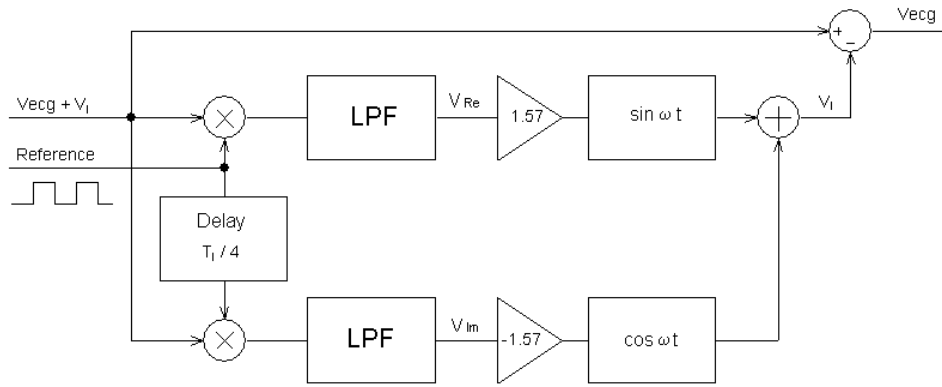
Fig. 2 Open-loop architecture for interference extraction

However the PL frequency could vary up to ±0.2Hz and will produce a difference frequency at the mixer output (beat) which degrades the interference extraction in dependence on the LPF settling time. This influence could be avoided if the sampling rate and the internally generated references are synchronized to the PL frequency. A simple solution for tracking is by band-pass filtering of the input signal and counting and averaging the PL periods. The other modern approach could be by Digital Phase Locked Loop (DPLL) architecture (see fig. 3) [14].

2.2 Closed-loop architecture for interference extraction

The closed-loop principle is based on two mixers connected in two control loops: one for automated phase control and other for automated gain control, as shown in fig. 3.

The first mixer operates with quadrature reference and serves as a phase-detector in DPLL system. The main task of this loop is to track the sampling rate and the in-phase and quadrature-phase references to the PL frequency. As can be seen from fig. 3, after filtering the mixer output is fed to the DCO (Digitally Controlled Oscillator) input. The DCO is a software controlled oscillator (timer) and has similar functionally like VCO (Voltage Controlled Oscillator) in conventional PLL design.
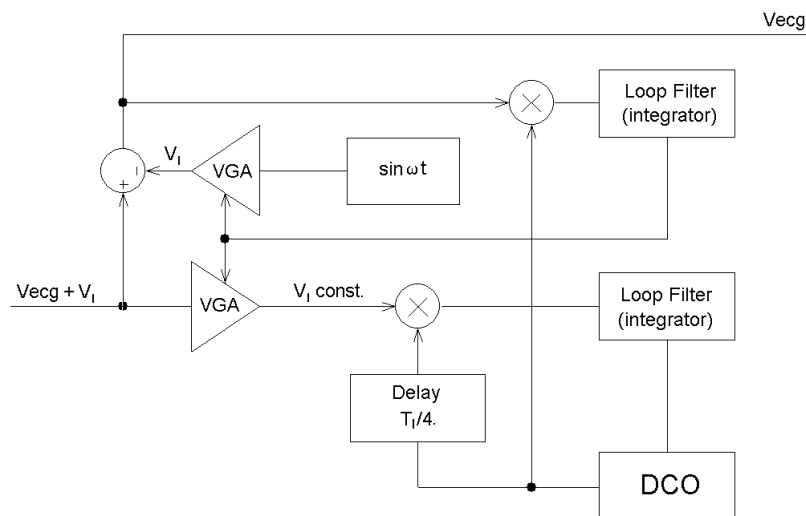

Fig. 3 Closed-loop architecture for interference extraction

At steady-state the average value at the mixer output is zero thus the DCO output is in-phase with the PL interference. Because the DCO serves as a second integrator connected in the control loop, the loop filter should be carefully designed and optimized to make a stable operation with appropriate settling time [14].

The second mixer is connected in automated gain control loop. It controls two digital VGAs (Variable Gain Amplifiers). The first one stabilizes the PL interference amplitude fed to the DPLL. The second VGA scales the amplitude of a generated (e.g. by a look-up table) sine wave. At steady-state the average value at the mixer output is zero thus the PL interference is perfectly subtracted.

3. RESULTS

The open-loop architecture from fig. 2 was tested by MATLAB simulations. A real ECG signal, sampled at 2kHz is used. The implemented low-pass filters (LPF) are two-pass moving average with first averaging time 20ms (one PL period) and second averaging time 200ms (10 PL periods). The group delay of such filter is 110ms.

Fig. 4 shows a simulation result without PL interference. The first trace is the original ECG signal. The second shows the same signal after a lock-in procedure. The third trace is the error i.e. the difference between trace 1 and 2. 1 LSB corresponds to 1μV. It is clear that the lock-in procedure introduces a spurious noise (hum) lower than 5μV. Note that the amplitude of the introduced spurious noise depends on the used LPF characteristic. Generally speaking reducing the bandwidth *n* times will reduce the remaining spurious
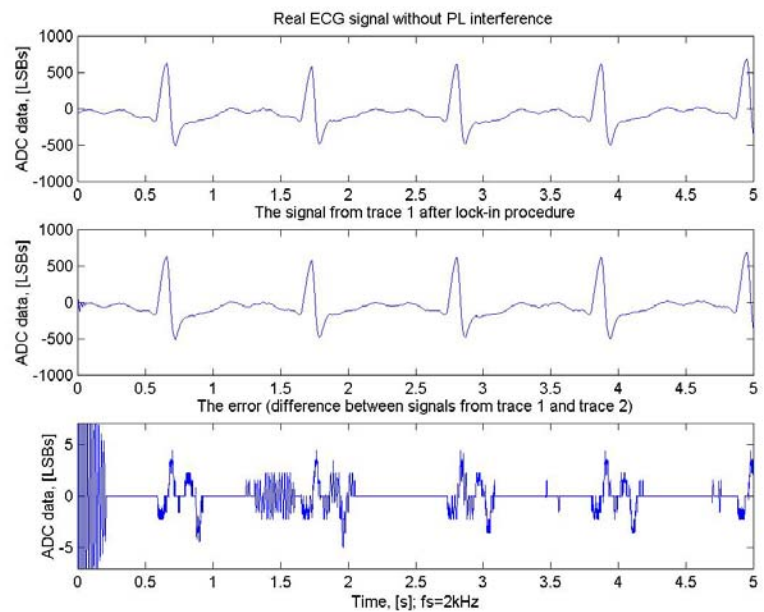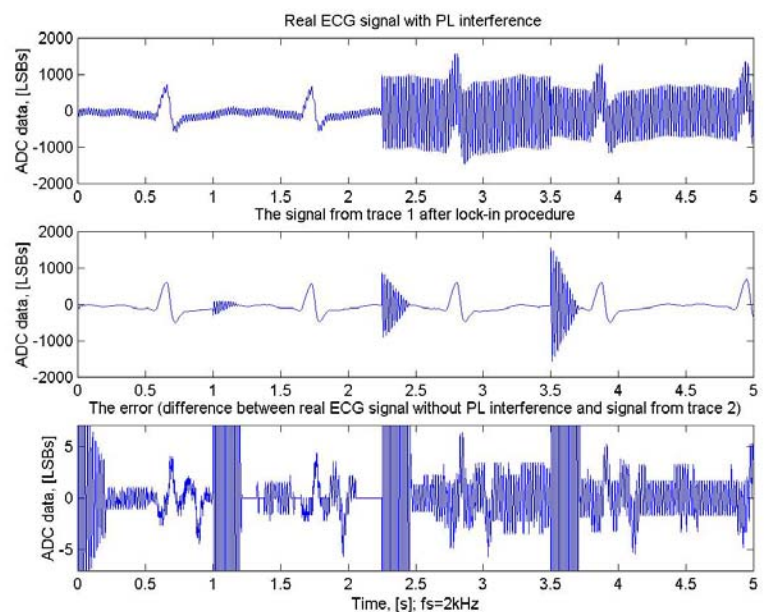

Fig. 4 Spurious noise after lock-in procedure

Fig. 5 Interference removal by lock-in procedure

noise $\sqrt{n}$ times.

Fig. 5 shows the behavior of the lock-in procedure with changes in the PL interference. At the beginning the amplitude of the PL interference is 100μV. At 1s simulation time the interference phase is changed to 135º. At 2.25s the interference amplitude is increased to 1000μV, and after 3.5s the amplitude is decreased to 700μV in combination with a phase change from 135º to 0º.

It can be seen that the lock-in reaction time is 110ms and depends on the group delay of the used LPF. When the LPF is settled the remaining error is around 5μV regardless the interference amplitude.

4. CONCLUSION

The presented digital lock-in techniques provide a powerful and ultimate solution for rejecting the PL interference in all biosignal acquisition applications.

The main advantages of the presented approach should be pointed out:

- simple solution for removal of fundamental frequency of the PL interference as well as its higher harmonics
- could be organized in open-loop or closed-loop architecture
- suitable for real-time operation with popular low-cost microcontrollers.

5. REFERENCES

[1] Huhta C, Webster J *60-Hz interference in electrocardiography*. IEEE Trans. Biomed. Eng. 20, pp. 91-101, 1973

[2] Warlar R, Eswaran C *Integer coefficient bandpass filter for the simultaneous removal of base line wander, 50 and 100Hz interference from the ECG*. Med Biol Eng Comp 29, pp. 333-336, 1991

[3] Yoo S et al. *Simple self-tuned notch filter in a bio-potential amplifier*. Med Biol Eng Comp 35, pp. 151-154, 1997

[4] Levkov Ch. *Fast integer coefficient FIR filters to remove the AC interference and the high-frequency noise components in biological signals*. Med Biol Eng Comp 27, pp. 330-332, 1989

[5] Christov I, Dotsinsky I *New approach to the digital elimination of 50 Hz interference from the electrocardiogram*. Med Biol Eng Comp 26, pp. 431-434, 1988

[6] Levkov Ch et al. *Removal of power-line interference from the ECG: a review of the subtraction procedure*. Biomedical Engineering Online 4 pp. 50, 2005

[7] Widrow B et al *Adaptive noise canceling: Principles and applications*. Proceedings of the IEEE 63, pp.,1692-1716, 1975

[8] Barr R, Fendjallah M *Frequency domain digital filtering techniques for selective noise elimination in biomedical signal processing*. IEEE Comp. in Card., 2 pp. 813-814, 1990

[9] PerkinElmer Inc. *The analog lock-in amplifier*, Technical note TN1002, 2000

[10] PerkinElmer Inc *The digital lock-in amplifier*, Technical note TN1003, 2000

[11] Princeton Applied Research Corp. *Explore the lock-in amplifier*, 1983

[12] Princeton Applied Research Corp. *A lock-in amplifier primer*, 1975

[13] Scofield J *A frequency domain description of a lock-in amplifier*, American journal of physics 62 pp. 129-133, 1994

[14] Li W, Meiners J *Introduction to PLL system modeling*, Texas Instruments Inc. Application journal SLYT015, 2000