An Analog Checker With Input-Relative Tolerance for Duplicate Signals

Haralampos-G. D. Stratigopoulos & Yiorgos Makris
Electrical Engineering Department
Yale University
New Haven, CT 06520-8285

Abstract

We discuss the design of a novel analog checker that monitors two duplicate signals and provides a digital error indication when their absolute difference is unacceptably large. The key feature of the proposed checker is that it establishes a test criterion that is dynamically adapted to the magnitude of its input signals. We demonstrate that, when this checker is utilized in concurrent error detection, the probability of both false negatives and false positives is diminished. In contrast, checkers implementing a static test criterion may only be tuned to achieve efficiently one of the aforementioned objectives. Likewise, when the proposed checker is employed for off-line test purposes, it results simultaneously in both high yield and high fault coverage.

1. Introduction

The numerous analog interfaces incorporated in modern systems have stimulated an increasing level of interest in analog test. The problem is particularly difficult mainly due to the continuous nature of analog signals and the necessity for accurate measurement of their values. Limitations of traditional functional test methods led to the development of Design for Test (DFT) techniques that aim to reduce the complexity of stimuli application and response evaluation and, by extension, to lessen the dependency on automatic test equipment.

Current DFT techniques fall into one of the following categories: *reconfiguration for test* and *code-based test* [1]. The former consists of methods to reconfigure the circuit under test into an easily testable form or to establish access to internal nodes in order to reduce the test generation effort and improve fault detection. The latter utilizes analog checkers to determine whether an inherent or generated code is corrupted due to the presence of a fault. The use of analog checkers to set a test criterion has the important advantage that it alleviates the difficulty encountered in measuring the values of on-chip signals through external means.

Typically, a checker is employed to compare two signals. Comparators are extensively used in analog design [2], with their most important application occurring in analog-to-digital conversion. The sign of their output voltage indicates which of the input signals is larger. For test purposes, however, one is rather interested in the *correlation* of two encoded signals. As an example, consider two signals that are expected to be identical in the absence of faults. Since deviations from nominal values attributable to process variations are certain to exist, checkers should take into account a tolerance window within which two signals are deemed equal instead of performing an exact comparison.

Recently, several analog DFT approaches that utilize checkers have been proposed. In [3], the output of a programmable biquad that can mimic any biquad in a filter is compared successively to the output of every filter stage when both receive the same input stimulus. The use of continuous checksums for circuits with a state-variable representation is proposed in [4], where two duplicate signals are generated from internal nodes in two different ways and are compared to detect circuit malfunctions. A pseudo-duplication method is presented in [5], where a checker is used to compare two signals whose nominal values are identical during fault-free operation. The design of self-exercising analog checkers has been studied separately in [6].

In all cases described above, the checker examines whether the inequality $|V_1 - V_2| < V_\delta$ holds, where V_1, V_2 are the input voltages and V_δ is a threshold voltage that accounts for process variations. V_δ is defined statically for a specific input value V_o. While this is acceptable for signal values within a narrow band, $V \in [V_o - \Delta V_o, V_o + \Delta V_o]$, $\Delta V_o > 0$, it is too constraining when $V > V_o + \Delta V_o$ or too lenient when $V < V_o - \Delta V_o$. For example, assume that the threshold is set to 10mV. In this case, for a pair of signals of nominal magnitude 100mV, a 12mV deviation in one of them, i.e. a 12% signal discrepancy, is indicated as an error. Similarly, for signals of magnitude 500mV, the same 12mV deviation will also be flagged as an error, despite the fact that it constitutes only a 2.4% difference from the nominal value. On the other hand, for a signal of magnitude 50mV, an 8mV deviation, which corresponds to a 16% difference from the nominal value, will not be flagged as an error since this deviation is less than the statically defined error threshold of 10mV. Consequently, high fault coverage and high yield cannot be achieved simultaneously, unless the input voltage range is restricted within the set $[V_o - \Delta V_o, V_o + \Delta V_o]$. Furthermore, when the checker is employed in a concurrent error detection scheme, the use of a predefined static threshold will result in inadvertent false positives and false negatives. Hence, in order to enhance the quality and accuracy of test, checkers with a dynamically adjustable error threshold are necessary.

This problem was first reported in [7], wherein a sample-and-compare circuit implementing a threshold relative to the magnitude of the input signal was proposed. In order to make

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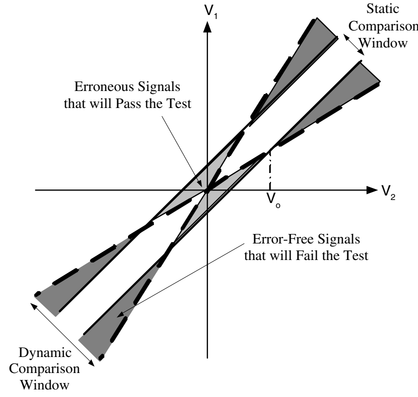

Figure 1. Code space of duplicate signals considering static and dynamic tolerance.

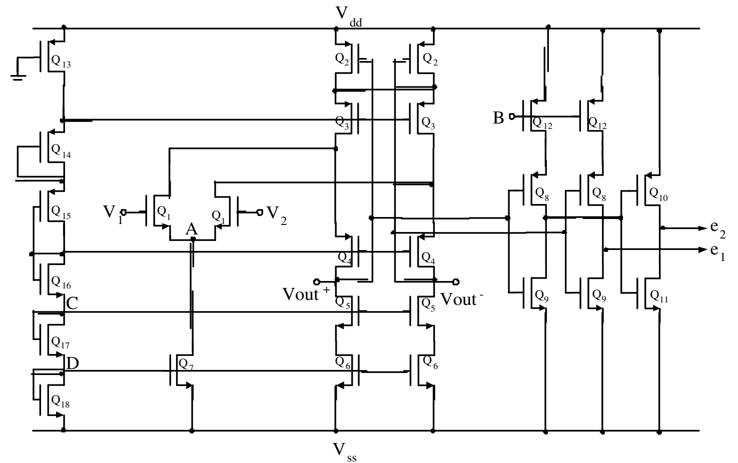

Figure 2. Schematic of the proposed analog checker with dynamic error threshold.

the operation of this checker as synchronous with the circuit under test as possible, the sampling frequency of the former has to be significantly higher than the actual operational frequency of the latter. The slew-rate of the op-amps in the checker, however, limits the sampling frequency that can be achieved since the checker output has to settle before a new sample is obtained. Increasing the sampling frequency requires that high-performance amplifiers be used, which may increase prohibitively the area overhead. Moreover, charge imbalance in the transistor channels and the capacitor plates due to switching operations may cause erroneous evaluation of small signals.

The aforementioned limitations are resolved in a novel design described herein. The area overhead is significantly reduced. Furthermore, the lack of switching activity in the proposed circuit enables continuous signal monitoring, thus revoking the limitations that sampling imposes on the operational frequency of the circuit under test and on the magnitude of the signal being evaluated.

The remaining of the paper is organized as follows. In section 2, we define the relative threshold. In section 3, we present the actual design of the proposed checker. In section 4, we illustrate the operation of the checker and its advantages over checkers utilizing a statically defined threshold through representative simulations. The properties of the proposed checker are discussed in section 5.

2. Threshold Definition

The checker monitors two nodes, which ideally, during correct operation, attain the same voltage value. Since the checker allows a margin to account for mismatches or other non-idealities, it examines whether the following inequality holds:

$$|V_1 - V_2| < V_\delta = \varepsilon_r \frac{|V_1 + V_2|}{2} \tag{1}$$

The threshold is defined as a percentage of the absolute average value of the input signals. If the above inequality is not satisfied, the checker indicates the unacceptable signal discrepancy. The threshold assignment in (1) is equivalent to the one given in [7].

The advantage of this approach over a statically defined error threshold is demonstrated in Fig. 1, where the space of two signals is represented by the entire plane. The area within the parallel dark lines corresponds to signals that are considered equal when a static threshold is utilized. In contrast, when a dynamic threshold is utilized, equivalent signals are contained within the dashed lines. Assuming that a percentile deviation is a fairer criterion, shaded regions indicate false assessments when a static error threshold is utilized: signal pairs that are included into the shaded regions will erroneously fail the test if $|V| > V_o$ or will erroneously pass the test if $|V| < V_o$. In off-line test, error-free signals failing the test correspond to yield loss, while erroneous signals passing the test inevitably result in an increased test set or in fault coverage reduction. Similarly, in concurrent error detection, error-free signals failing the test correspond to false negatives, while erroneous signals passing the test correspond to false positives.

It is evident that in most circumstances, where the possible input voltage band is not very small, a relative tolerance is more appropriate for assessing the signal pair, whereas a static threshold model would lead to an unacceptable probability of circuit misclassification.

3. Circuit Design

The schematic of the proposed checker is shown in Fig. 2. The design is based on a fully differential folded-cascode amplifier used in an open-loop configuration (transistors Q_1-Q_7) [2]. Transistors Q_{13}-Q_{18} form a bias chain, which establishes consistent bias currents in the branches of the amplifier. The size of Q_{16} is chosen to set the dc voltage in the

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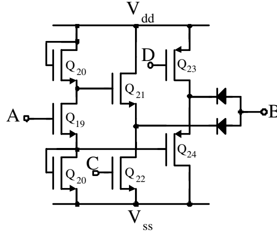

Figure 3. Full-wave rectifier.

output nodes to the desired value V_{out}^{dc}. Small-signal analysis of the circuit yields:

$$V_{out}^{+} \approx +A_{v1}(V_1 - V_2)$$
$$V_{out}^{-} \approx -A_{v1}(V_1 - V_2) \tag{2}$$

where

$$A_{v1} = \frac{2g_{m_1}}{(g_{d_1} + g_{d_3})g_{d_4}/g_{m_4} - g_{d_6}g_{d_5}/g_{m_5}}$$

and g_{m_i}, g_{d_i} are the transconductance and the incremental drain conductance of transistor Q_i, respectively. Each of the outputs of the amplifier is connected to an inverter (transistors Q_8-Q_9), which is biased to $V_t > V_{out}^{dc}$. We define the distance α as:

$$\alpha = V_t - V_{out}^{dc} \tag{3}$$

Thus, an absolute voltage change of magnitude larger than α in the outputs V_{out}^{+} and V_{out}^{-} will cause one of the two inverters to change state. The distance α is chosen to set the desired test criterion. If

$$|V_1 - V_2| > \alpha A_{v1}^{-1} \tag{4}$$

then the circuit indicates that the discrepancy of the input signals exceeds the tolerance window. In this case, the outputs receive the values $e_1e_2 = 00$ or $e_1e_2 = 11$ depending on the sign of the difference between the input signals. One inverter is triggered by positive changes and the other by negative changes. If the input signal deviation is acceptable, the checker indicates fault-free operation by setting $e_1e_2 = 10$.

The error threshold $V_\delta = \alpha A_{v1}^{-1}$ can be made relative to the input signals if the distance α is regulated by their magnitude. This is accomplished by adding a load transistor Q_{12} at each output inverter, as shown in Fig. 2. The voltage in node B regulates the current that flows through the inverters, and therefore the bias voltage V_t, when both transistors are in saturation. It can be shown that:

$$V_B \approx V_\alpha - \sqrt{\frac{(W/L)_{Q_9}}{(W/L)_{Q_{12}}}}\alpha \tag{5}$$

where

$$V_\alpha = V_{dd} + V_{T_p} + \sqrt{\frac{(W/L)_{Q_9}}{(W/L)_{Q_{12}}}}\left(V_{ss} + V_{T_p} - V_{out}^{dc}\right)$$

Selecting appropriate sizes for the transistors Q_9 and Q_{12} so that $V_\alpha = 0$ and using (1), equation (5) becomes:

$$V_B \approx -A_{v2}\frac{|V_1 + V_2|}{2} \tag{6}$$

where

$$A_{v2} = \sqrt{\frac{(W/L)_{Q_9}}{(W/L)_{Q_{12}}}}A_{v1}\varepsilon_r$$

We proved that the threshold assignment in inequality (1) is achieved if the voltage V_B varies in accordance to (6). A circuit that produces this voltage at the gates of transistors Q_{12} is illustrated in Fig. 3. It is a simple full-wave rectifier with some gain. The voltage in node A is $V_A = (V_1 + V_2)/2$. V_A and is replicated at the gates of Q_{21} and Q_{24} with opposite polarities. Transistors Q_{21}-Q_{24} form two *dc*-level shifters which bring the *dc* value of these two signals to analog ground. The diodes carry out the rectification. The output voltage is given by:

$$V_B \approx -\frac{g_{m_{19}}}{g_{m_{19}} + g_{m_{20}}}\frac{|V_1 + V_2|}{2} \tag{7}$$

Therefore we have to choose the geometry of Q_{19}, Q_{20} such that:

$$\frac{g_{m_{19}}}{g_{m_{19}} + g_{m_{20}}} = A_{v2} \tag{8}$$

Note that there is enough freedom in the design to satisfy the conditions set above.

Since there are no high-impedance nodes internal to the fully differential amplifier, its output terminals settle very quickly. The response at high input frequencies is limited by the switching characteristics of the inverters. The checker is designed to be asymmetrical in the sense that the transition of an input pair to an erroneous state is detected quickly, while the transition into the error-free state is slower [6]. This is achieved by choosing the ratio $(W/L)_{Q_9}$ to be large in order to speed up the falling time of the inverters. The geometry of Q_8 and Q_{12} is chosen properly so as to set the desired value of the quiescent error threshold, while maintaining a ratio $(W/L)_{Q_8}$ as large as possible in order to reduce the rise delay of the inverters as well.

At high-input frequencies, the speed at which the threshold adjusts to the inputs' magnitude degraded due to the high impedance nodes in the full-wave rectifier. Specifically, the rectifier recovers at a smaller rate than dV_A/dt resulting in a significant distortion during the zero crossing of V_A. If a high-frequency test vector is required for off-line test or if

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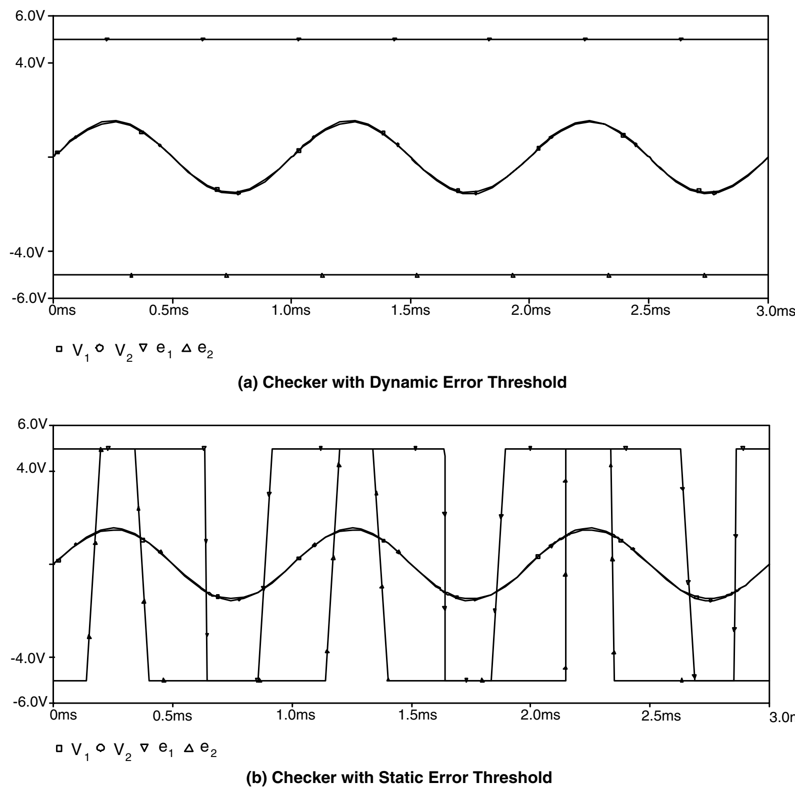

(a) Checker with Dynamic Error Threshold

(b) Checker with Static Error Threshold

Figure 4. Simulation of a sinusoidal pair with amplitudes $|V_1|_{max} = 1.5V$ and $|V_2|_{max} = 1.56V$.

a concurrently tested circuit operates in high-frequencies, a wide bandwidth full-wave rectifier [8] can be used to assure correct threshold assignment.

4. Simulation Results

In the following simulations, we set the error threshold to $\varepsilon_r = 0.05$ and we experiment with signals of frequency 1 kHz.

Assume that the inputs of the checker are two sinusoidal signals of amplitude 1.5V and 1.56V respectively. Let us also assume that the threshold of a similar checker without variable threshold capability is set to 50mV. Since the discrepancy of the two signals is less than 5% of their average value, the proposed checker indicates correct operation $-e_1e_2 = 10-$, as shown in Fig. 4(a). However, the checker with the statically defined error threshold indicates (incorrectly) this nominal deviation of less than 5% as an error $-e_1e_2 = 11$ and $e_1e_2 = 00$[1]$-$, as shown in Fig. 4(b). In this case, the circuit would be discarded as faulty during off-line test, resulting in yield loss. Likewise, false negative indications would occur during concurrent error detection.

Let now the inputs of the checker be two sinusoidal signals of amplitude 0.5V and 0.54V respectively. In this case, the proposed checker will correctly identify the unacceptably large signal difference, as shown in the simulation of Fig. 5(a). In contrast, as shown in Fig. 5(b), the checker with the statically defined error threshold of 50mV will not detect the discrepancy, despite the fact that it is larger than 5% of the average value of the two signals. This example indicates how faulty circuits may evade detection during off-line test when a static test criterion is used. Similarly, frequent false positive signal assessments would occur during concurrent error detection.

Similar results were obtained through numerous simulations of signals of various shapes and magnitudes. The error detection threshold remains close to 5% of the average value for all of these signals. We stress that ε_r can be set to any value by choosing the appropriate transistor sizes.

5. Comments on the Properties of the Checker

As compared to the previous solution [7], the proposed circuit results in lower area overhead since it avoids using costly capacitors, resistors, and op-amps. Moreover, it monitors signals continuously and has the ability to assess any voltage pair, thus being independent of the circuit under test. In contrast, the switching operations in [7] will cause charge injection, which inevitably, after repetitive comparisons will result in misguided decisions unless an autozeroing technique is employed. Even in this case, charge injection may be a serious limitation when low-voltage signals are processed.

[1] We remind that when the difference $V_1 - V_2$ exhibits a positive change exceeding the error threshold, the checker outputs obtain the values $e_1e_2 = 11$. Similarly, the outputs obtain the values $e_1e_2 = 00$ when a negative change exceeding the error threshold occurs.

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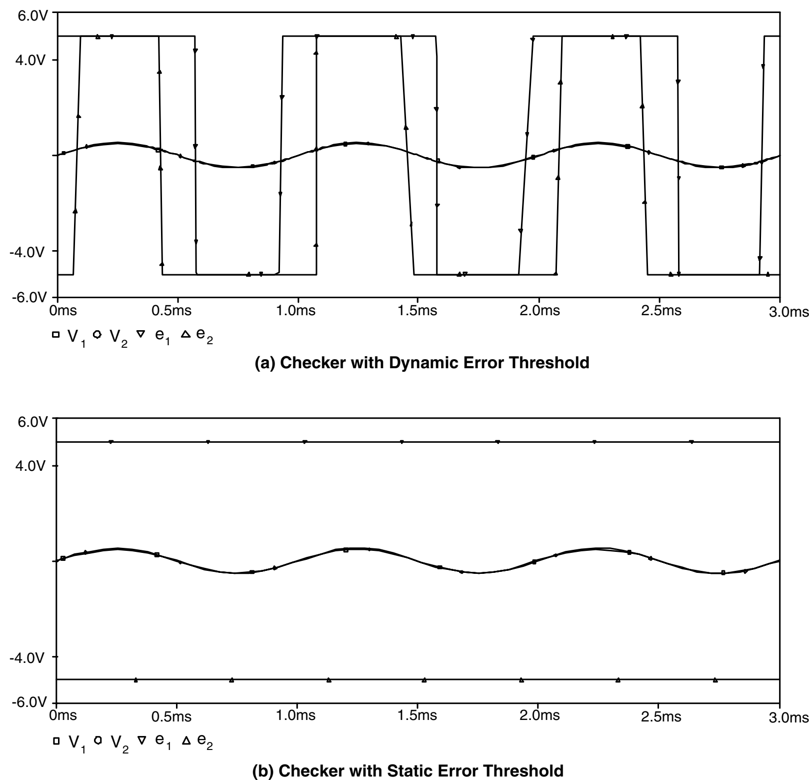

Figure 5. Simulation of a sinusoidal pair with amplitudes $|V_1|_{max} = 0.5V$ and $|V_2|_{max} = 0.54V$.

The error detection scheme implemented by the proposed checker does not assume a specific fault model. It is rather defined at an abstract level in terms of the correlation of its input stimuli. In order to achieve a reliable error detection scheme for the circuit under test, the checker must necessarily be code-disjoint [9]; i.e. input values are mapped to the output code space if and only if they belong to the input code space. Therefore, the checker must indicate its own faults that violate the code-disjoint property. For this purpose, the method presented in [7] is followed, wherein potential faults in the checker are targeted in a short separate test phase.

6. Conclusion

Efficient analog circuit test through code-based DFT methods necessitates checkers wherein the comparison window is defined as a percentile deviation from the nominal value of the evaluated signals. Towards this end, we presented a low-cost checker that dynamically adjusts the error threshold to the magnitude of its input signals. As discussed theoretically and as demonstrated through simulation, when utilized in off-line test the proposed design results simultaneously in high fault coverage and low yield loss. Furthermore, during concurrent test, it resolves the problem of false positive and false negative signal assessments and operates continuously and in parallel with the circuit under test. In short, the effectiveness of existing analog test solutions can be significantly enhanced by the accuracy of the proposed checker.

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