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Miniature Fuel Cell with Monolithically Fabricated Si Electrodes - Optimization with Square Shape Through-chip Porous Layer –

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Abstract: Our Si based thin fuel cells have a through-chip porous Pt layer. The through-chip porous area has long narrow shape and the through-chip porous layer sometimes cracked during experimental handling. Therefore, the fuel channel shape was changed to square shape. Si substrate around the through-chip porous area works as rims and the mechanical strength seemed to be improved. Using the square openings, peak output of 108mW/cm^2 was obtained. However, the square opening is not suitable for our stacking structure. Then shallow channels, which connect each through-chip porous Pt layer, were fabricated by plasma etching with double masking layers.

Key words: miniaturized fuel cell, porous Si, plating, plasma etching, MEMS

1. INTRODUCTION

Portable electronic devices have driven research about small electric power sources. At this point, Li ion batteries are widely used in the portable devices. However, the portable devices will need higher electric energy storage abilities for higher functionalities and recent accidents, such as explosion of the batteries, may suggest that we are facing difficulties in further improvement of the Li ion batteries. Then, fuel cells have attracted large attention as ultimate portable power sources. Prototypes have been demonstrated by many research groups [1-2] and some of them are really sophisticated and seem to be fit for practical use. But, no miniature fuel cells are available in a usual consumer market yet. There may be problems in production cost and mass productivities. Further miniaturization will be still needed.

MEMS (Micro Electromechanical Systems) fabrication technology is an important tool to reduce the fuel cell structure to micrometer scales and is advantageous for mass production. Therefore, a lot of studies for fuel cell miniaturization using MEMS techniques were made during these several years [3-12]. In most of those studies, conventional catalyst layers, in which carbon black with catalyst metal particles is splayed, were used. However, MEMS fabrication techniques treat basically monolithic structures and treating powders such as carbon black is not preferable. In order to adapt the construction process to more MEMS fabrication procedures, various approaches have been tried though the performance of the prototypes were generally poor [9-11]. Then, much attention have been paid for forming catalyst layers which need large surface area. Recently, Honda proposed a novel fine silicon based fuel cell using carbon nanotubes as a catalyst support and relatively high power output was reported [12].

Recently, we discovered that a porous Pt layer can be obtained by just immersing high porosity porous Si into a Pt plating bath containing HF [13]. Using the porous Pt as a catalyst layer, we built novel fuel cell electrodes [14]. On the electrodes, fuel channels were etched after forming the porous Pt catalyst layer and the catalyst layer was expected to work as a stopping layer of plasma etching. Then, through-chip porous Pt layer were successfully fabricated and monolithic fuel

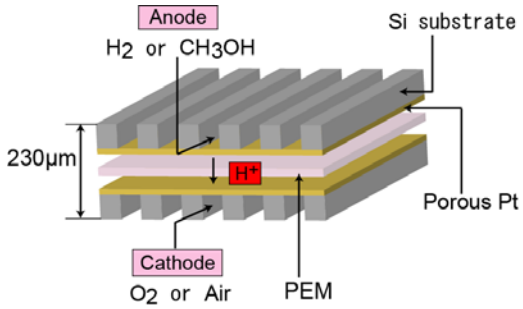

Fig.1 Schematic view of the Si based fuel cell

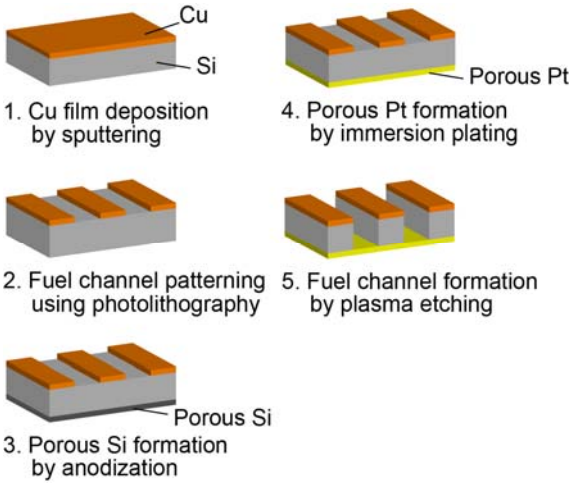

Fig.2 Fabrication process of the monolithic electrode

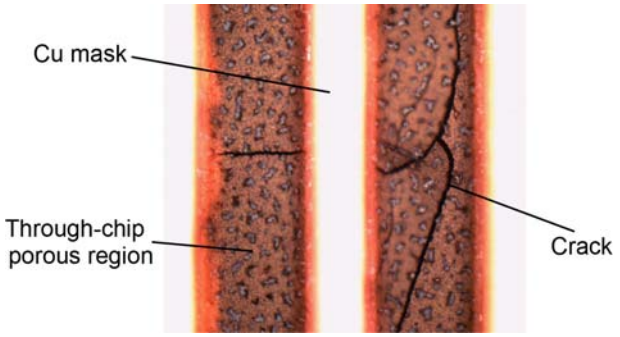

Fig.3 Top view of the electrode after fuel channel fablication

cell electrodes were demonstrated. Prototype cell showed a relatively high output of 82mW/cm^2 among MEMS based miniature fuel cells as presented in the last PowerMEMS2007. But the performance was poor for practical use and further improvement was needed.

At this point, the electrodes are 100µm thick and they are fragile. Especially, our preliminary prototypes has millimeter scale through-chip porous layer where cracks were often caused. In this study, new fuel channel structure is proposed for improvement of the cell performance.

2. NEW FUEL CHANNEL STRUCTURE

2.1 Fuel cell design

The fuel cell design we proposed is shown in figure 1. The electrode plate has quite simple structure, in which catalyst layer and fuel channels are monolithically fabricated on a Si wafer. A highly doped Si wafer, that has low resistivity, works as a current path. PEM (Polymer Electrolyte Membrane) is hotpressed with two Si electrodes using Nafion solution as an adhesive. Thickness of the Si wafer is about 100µm and the total thickness of a cell can be less than 230µm. Figure 2 shows the fabrication procedure. After removing oxide by HF, copper thin film is deposited on the Si wafer by sputtering. Using usual photolithographic patterning with photoresist and wet etching, fuel channel mask is made on the copper film for plasma etching. Porous Si layer is formed on the opposite side of the Si wafer by anodization in an electrolyte containing HF. The porous Si layer is subsequently submerged in a Pt plating bath and porous Pt layer is obtained. Detailed description about porous Pt layer formation can be seen in ref. [12]. Fuel channels are opened by applying plasma etching on the backside of the porous Pt layer with the copper film mask. Conventional parallel plate reactive etching system is used, and SF_6 and O_2 gases are used for the etching. In this plasma etching process, porous Pt layer is supposed to work as a stopping layer of the etching, because the etching rate is low at the

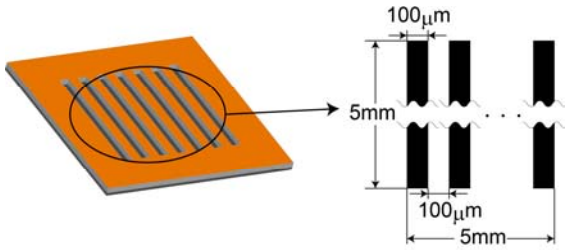

Fig.4 Conventional slender through-chip porous region.

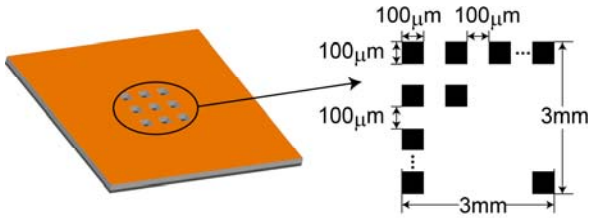

Fig.5 Square shape through-chip region.

porous metal layer, and through-chip porous Pt layer can be relatively easily fabricated.

2.2 Square shape opening for fuel supply

In the past experiments, cracks were sometimes observed on the bottom of the fuel channels, where through-chip porous Pt layer appeared, as shown in figure 3. Porous Pt layer is supposed to be the most fragile part on the electrode plate. Figure 4 shows the conventional fuel channel shape. The dimension of the fuel channels were 5mm in length and 100µm in width. Therefore, it is expected that such large through-chip porous layer can be easily damaged by small shocks during experimental handling or plasma etching. In order to reduce the crack generation, a rim on the through-chip porous layer is supposed to be useful. Then, opening shape of the through-chip porous layer was modified from narrow rectangle to 100µm x 100µm square shape as shown in figure 5. At this point, yield factor of the cell fabrication is poor. Generally it is difficult to make large reaction area without damage and dimension of the reaction area was shrunk from 5mm x 5mm to 3mm x 3mm. By this modification, though the area of the through-chip porous Pt area was reduced, Si substrate around the through-chip porous area is supposed to work as rims and the mechanical strength of the electrode plate may be improved.

Using the above new design, fuel cells were built with trial and error. There are no quantitative data, but the yield rate seems improved and various conditions, such as thinner through-chip porous layer, which could not be built in past experiments, could be tested. Figure 6 shows an example result. Conditions used in the catalyst layer formation are shown in table 1. TSF-

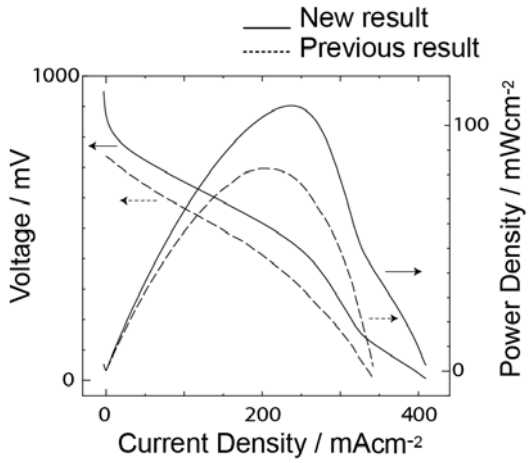

Fig.6 Polarization curve of the prototype cell

1301 PEM sheet (Toagosei, Japan) was used. Because this PEM sheet has small swelling deformation, damage of the porous Pt layer is not serious in our experiments. 1.25% Nafion solution was dropped on the Si electrode plates and hotpress was applied for 30 min at 373K. Power generation was tested in a temperature controllable chamber at 318K. 6 sccm of dry hydrogen and 6 sccm of oxygen were fed to the cell respectively. The peak output of 108mW/cm^2 was obtained, which is 30% increase from the previous result reported in PowerMEMS 2007. Further optimization and observation is still ongoing.

2.3 Fuel channel design for cell stacking

In the conventional fuel cell system, stacking of the cells is usually used and higher power density is realized. The advantage of our fuel cell design is the small thickness. In order to take advantage of the thin structure, smart stacking technique has to be developed. In the MEMS processes, anodic bonding or direct bonding are often used. The anodic bonding needs high temperature around 700K. However, stack bonding process is required to be done at low temperature because the catalyst layer is delicate to the heat. While in the direct bonding process, very clean surface are required but the surface of the electrodes is contaminated during the fabrication process. Solder bonding is expected to be applied to rough surface and

Table 1 Condition for prototype fuel cell

Property of Si substrate	
Crystal Orientation	(100)
Type	N
Resistivity [Ωcm]	0.001-3
Anodization condition	
Composition of solution	Water : HF(46%) : Ethanol = 5 : 3 : 2 (wt)
Current density [mA/cm^2]	60→0
Time	1380
Immesion plating condition	
Composition of plating bath	1.0MH_2SO_4 + 20mMH_2PtCl_6 + 400mMHF
Plating time [min]	25, 30

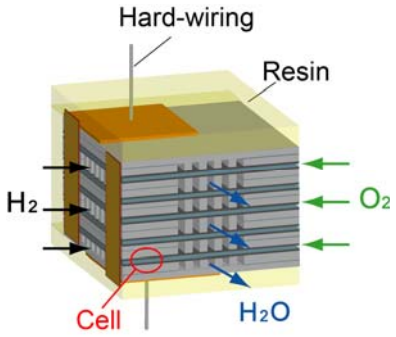

Fig.7 Cell stacking structure

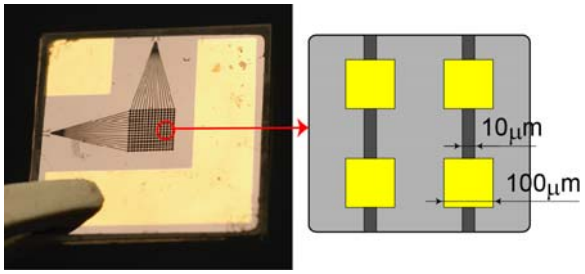

Fig.8 Shallow fuel channels

the bonding is available with relatively low temperature process by choosing appropriate metals. Solder layer is also expected as a current path for extracting produced current to outer circuits. At this point, we are attempting to construct stacking structure as shown in figure 7. In this structure, two electrode plates are bonded and parallel electric connection of each cell will be made with outer wirings. Fuel channels are formed to the edge of the plates. Therefore, fuel is fed from the side of the cell stacks and separation of fuels is expected to be easy.

However, the fuel supply opening employed in the previous section 2.2 does not have connection with each other. In order to realize the stacking structure, each opening has to be connected. Then, we decided to make shallow channels between each opening as shown in figure 8. Fabrication strategy is shown in figure 9. Thick photoresist is put on the copper film mask and photolithographic patterning is applied. On the fuel supply opening area, where through-chip porous layer is formed, there is no copper film nor photoresist. While on the shallow channel area, there is no copper film, but the photoresist remains. With this double mask structure, deep Si etching is expected on the fuel supply opening area, while on the connection channel area, Si etching starts after the thick photoresist is etched away and shallow trench is expected.

Figure 10 shows a SEM image after the plasma etching and the copper film removal by wet etching. Though the dimension of etched feature is broadened due to the poor plasma etching anisotropy, it is clearly

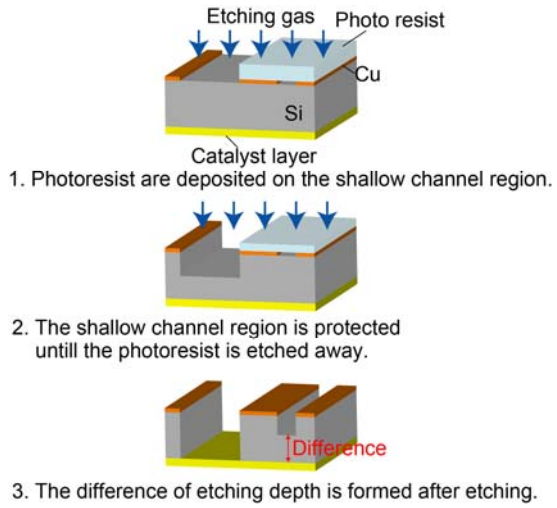

Fig.9 Schematic of the shallow channel formation

found that the depths of fuel supply opening and connection channels are different and the strategy works fine. Each opening is certainly connected by the shallow channels. In this case, approximately 20μm thick photoresist was prepared.

With recent Deep RIE machines, thin photoresist layer can be used as a mask for deep Si etching and thick photoresist is too resistive to be etched away. Even in that case, photoresist can be removed by applying just oxygen plasma and the etching start timing for shallow trenches can be controlled. Recent direct laser pattern generators have a gray scale function. Using this gray scale function, photoresist thickness can be controlled and channel depth might be flexibly designed. In this study, twice photolithographic patterning was needed, but by using recent techniques, such as the gray scale patterning, only once photolithographic patterning may be enough for making shallow connection channels.

4. CONCLUSION

In order to improve the performance of our miniature fuel cells with Si electrodes, long narrow fuel channels were modified to square shape fuel supply openings with shallow connection channels. With the square shape openings, Si substrate around the through-chip porous area is supposed to work as rims and mechanical strength of the through chip porous layer may be improved. This improvement broadens the use of various porous layers, such as much thinner porous layer or higher porosity layer. At this point, peak output of 108mW/cm^2, which is 30% larger than the one reported at the previous PowerMEMS 2007, was observed with the square openings. Yield ratio of the cell fabrication also seems to be improved by the square openings and further optimization will be performed.

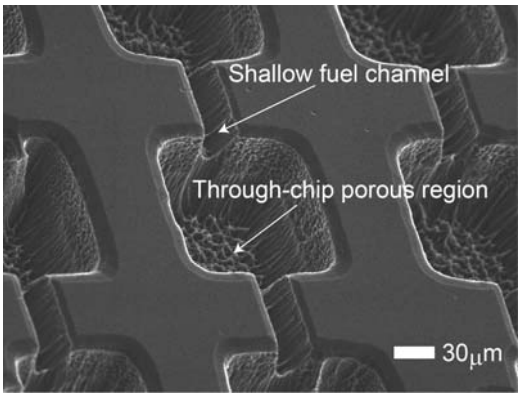

Fig.10 SEM view after plasma etching

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