Low Frequency Noise Considerations for CMOS Analog Circuit Design

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Abstract: This paper gives an overview on 1/f-noise issues relevant for today's CMOS analog circuit design. The device-to-circuit relation of noise and the relevant operating conditions are reviewed. Modeling of the biasing dependence of 1/f-noise amplitude including large signal and statistical effects are discussed. The noise corner frequency[1] is shown to increase with CMOS technology scaling, and statistical effects are shown to even scale worse compared to the 1/f-noise. Moreover circuit design measures against noise are investigated. Finally, reliability issues concerning 1/f-noise in analog circuits are reviewed.

Keywords: 1/f-noise, flicker noise, low noise circuit design, CMOS low noise

PACS: 85.40.Qx

INTRODUCTION

At low frequencies the noise of CMOS integrated circuits is dominated by 1/f-noise or even by the noise of individual traps (see Figure 1a). This noise increasingly threads design of low noise analog, mixed-signal and radio frequency circuits in increasingly larger frequency bandwidths. The noise corner frequency[1] is roughly 10 MHz for 90nm technology and will further increase in future CMOS generations (see Figure 1b). Careful design for low noise is mandatory in many cases. In this paper we review the 1/f-noise properties of CMOS devices at circuit-relevant operating conditions, their modeling, and discuss strategies to minimize noise in circuits.

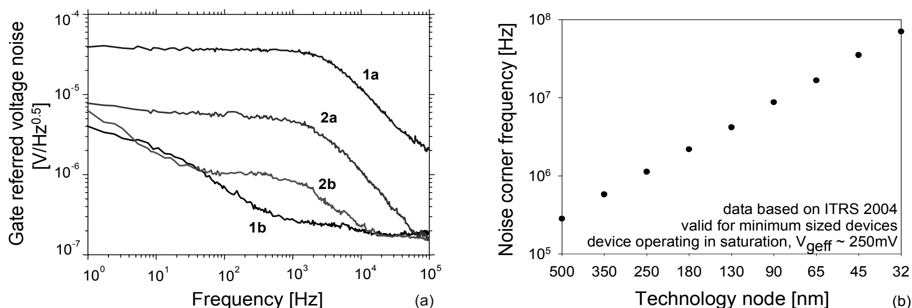

FIGURE 1(a): Gate referred voltage noise of two different W=0.16µm/L=0.13µm n-MOS transistors: first device biased at V_g-V_t =0.5V, with V_d=0.15V (1a) and V_d=1.0V (1b), second device, biased at V_d=1.0V, with V_g-V_t =0.5V (2a) and V_g-V_t =0.2V (2b). **(b)**: Noise corner frequency of minimum sized CMOS devices versus technology node calculated from ITRS 2004 data [1].

[1] Intercept point where amplitudes of 1/f-noise and thermal noise are equal.

1/F-NOISE IN CIRCUITS

To optimize the noise properties of CMOS analog circuits, noise propagation within the circuit and the device noise behavior in the circuit at the respective operating point needs to be considered. This is detailed for two examples and two classes of circuits.

The circuit in Figure 2a) shows a differential stage as it is frequently used for amplification of small signals or for buffering of signals. This circuit is an example for a small signal type circuit with almost constant biasing conditions. All devices are operated in saturation with gate voltages a few hundred millivolts above threshold (typically 100–500mV). Circuit noise calculation is performed considering that each noise voltage propagates like an uncorrelated signal in a small signal equivalent circuit.

The circuit in Figure 2b) shows a voltage controlled oscillator as it is frequently used for tunable frequency references. This circuit is an example for another class of circuits where the operating points of the devices undergo almost every value between maximum and minimum supply voltage for both gate and drain. As a consequence operating point dependent signal transfer functions including non-linear effects (e.g. frequency-mixing) have to be taken into account. A simple estimation of the noise from extrapolation of one operating point is insufficient. Especially here, circuit simulation tools are very useful. Since large-signal circuits often show periodic behavior they can either be described by a transient simulation over one period or by Fourier transformation techniques. As a rule of thumb, the most critical operating points for noise propagation are the points of equal current flow on both branches, when the output voltages (and therefore both drain and source voltages) are roughly half the supply voltage.

From a circuit-designers point of view, noise optimization is done by circuit sizing and choosing appropriate circuit architecture. Circuit simulation together with simple but sufficiently accurate noise models helps to reach an optimum solution in a reasonable amount of time. Moreover, a good understanding of the device physics behind 1/f-noise helps to identify possible bottlenecks for scaling the circuit architectures to new CMOS process generations.

1/F-NOISE COMPACT MODELING

1/f-noise of MOSFETs originates from trapping and de-trapping of charged carriers at the interface and oxide traps in the MOS structure [2] (Figure 3a). By variation of the number and mobility of free carriers in the MOS channel, the traps directly influence the low frequency noise behavior. Single traps produce a Lorentzian shaped spec-

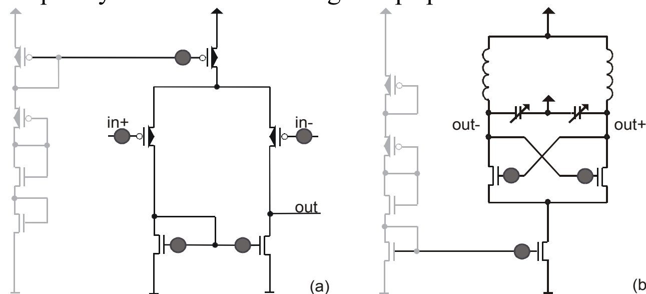

FIGURE 2(a): The picture shows a differential stage as example of a typical CMOS linear analog circuit for small signal gain. **(b)**: Voltage controlled oscillator as example for a noise sensitive circuit with large signal output. The devices depicted in light gray color represent simple biasing branches.

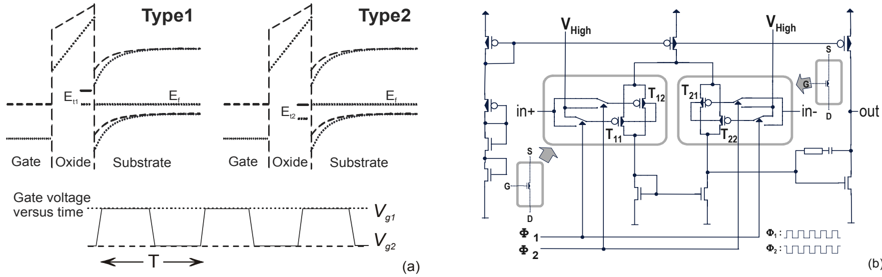

FIGURE 3(a): Energetic situation of two noise relevant traps at two different gate voltages as shown in the lower left. **(b):** Test circuit used for measuring the 1/f-noise reduction of switched MOSFETs [10].

trum, an ensemble of traps produces a noise spectrum roughly inversely proportional to the frequency [2,3,4] (Figure 4a). For small signal circuits using devices operated in saturation it is useful to describe the 1/f-noise S_{Vg} as referred to their gate voltage V_g:

$$S_{Vg}(V_g, f) = S(V_g) \cdot \frac{N_{t,f}}{W \cdot L} \cdot \frac{1}{f} \tag{1}$$

In this representation the Coulomb-equivalent charge of these trapped oxide charges well describes the noise behavior almost independent of the biasing [5]. $N_{t,f}$ is the trap density close to the Fermi level which is mostly relevant for noise, and W and L are the device width and length. The biasing relation is described by the function $S(V_g)$. It depends on the relative influence of number and mobility fluctuations on the noise amplitude [3,6], but the general influence on the noise amplitude over the range of relevant gate voltages is relatively weak for modern technologies.

1/f-noise amplitude is reduced under certain non-equilibrium biasing conditions [7,8,9]. The physics behind the noise reduction is understood when considering two types of traps and two voltages alternately applied to the gate of a device (see Figure 3a) [9]. The densities of those two types differ with respect to their energetic position and the corresponding alternating Fermi-level or gate voltage. If the period of oscillation between the two gate voltages is faster than the average capture and emission time of the trap levels, the traps cannot follow the fast oscillation. They often remain in the

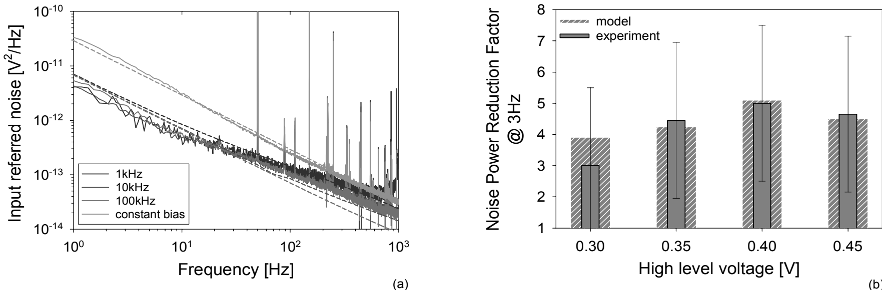

FIGURE 4(a): Experimental (solid lines) and calculated (dashed lines) gate referred voltage noise versus frequency of a W/L=12µm/0.6µm p-MOSFET with a rectangular gate-source voltage (V_{g1}=-500±30mV, V_{g2}=300±30mV, see Figure 3a) at switching frequencies indicated in the graph. Drain voltage is 800±100mV. **(b)**: Measured (thin bars) and calculated (thick bars) noise reduction versus higher gate-source voltage (V_{g2} = V_{high} in Figure 3b) for a W/L=12µm/1µm p-MOSFET at a lower gate-source voltage V_{g2} of -500±30mV, a switching frequency of 1kHz, and a drain-source voltage of 800±100mV.

energetic position where one of the two gate voltages drives them into a defined steady state where they do not contribute to the noise. This 'memory' reduces their trapping and de-trapping activity and their contribution to the noise at the other gate voltage where they normally are active is reduced as well. However, it also enhances their noise activity in the next half period when driven back into a defined state. Only if there is an imbalance in the trap densities at the two energetic levels corresponding to the two types of traps, this finally results in a reduction of the total 1/f-noise [9]. If one of the two voltage levels is close to the equivalent Fermi level of mid-gap, where the trap density is lowest, the highest noise reduction effect is observed.

Today's standard compact models are not capable of simulating the effect. However the effects of noise reduction under periodic large signal excitation can be analytically described for compact modeling using a stepwise constant approximation for the gate voltage:

$$S_{Vg}(V_g(t),T,f)=\sum_{i=1}^{k}\left(S(V_{gi})\cdot A_{\omega}^{i}(V_g(t),T,f)\right) \text{ with } V_g(t)=\begin{cases}V_{g1} & for\ n\cdot T<t\le(n+1/k)\cdot T\\ V_{gj} & for\ (n+(j-1)/k)\cdot T<t\le(n+1)\cdot T\\ \vdots\end{cases} \quad (2)$$

Here, A_{ω}^{i} is the Fourier transform of the average autocorrelation function of the noise relevant traps corresponding to the fraction of the period where the gate voltage $V_g(t)$ is equal to V_{gi}. This is detailed in [9]. T is the oscillation period, and j is an integer accounting for the k different constant voltage values, each valid for equal time fractions of the gate voltage oscillation period (repeated for the n-th time).

Figure 3b shows a test circuit for measuring the 1/f-noise of p-MOSFETs under periodic large signal excitation [9,10]. Results of those measurements and of the model (Eq. (4)) are shown in Figure 4a) and b). The model agrees with the experimental observed dependencies for the noise-frequency, the oscillation period and the biasing. For circuit design the effect may be used to reduce 1/f-noise below the constant biasing noise values [8,10] as in the circuit shown in Figure 3b).

STATISTICAL EFFECTS AND 1/F-NOISE

For modern CMOS technologies the amount of traps generating 1/f-noise is relatively small and for the smallest devices even single traps may dominate certain frequency bands of the low frequency noise (see Figure 1a). Compared to small signal gate voltage related changes in the gate referred 1/f-noise, device and intra-die varia-

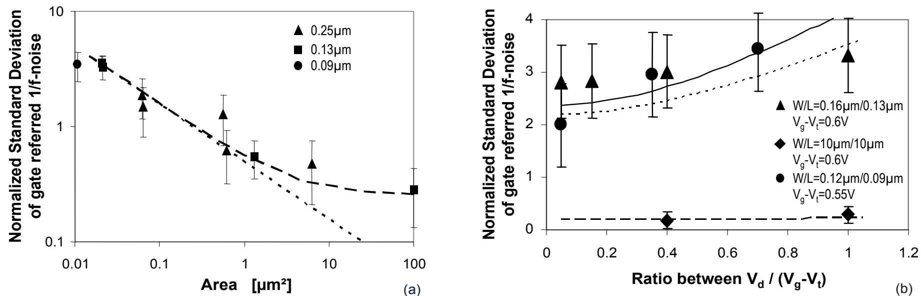

FIGURE 5(a): Standard deviation of 1/f-noise amplitude for several CMOS technologies from 0.25µm to 90nm versus area at V_g-V_t=0.6V, V_d=1V and **(b)** versus ratio of gate to drain voltage. The dashed and the dotted lines in (a) show results of a model for the 0.13µm data which includes and excludes global variations. The lines in (b) are results predicted by the same model.

tions are relatively large, at least for the most relevant operating conditions for analog circuits. A circuit however, has to be designed to yield in production. To cope with this effect, worst case statistics for the noise amplitude needs to be introduced for noise modeling and circuit design [6,11,12]. Since the trap distribution follows a Poisson statistic also the 1/f-noise of an ensemble of different devices approximately follows a similar statistics [6]. For hand calculations a simple worst case function for the 1/f-noise of a single device under 3σ conditions $S_{Vg,3\sigma}$ [12] is given by:

$$S_{Vg,3\sigma}(f,V_g) = S_{Vg}(f,V_g) \cdot \left(1 + 3\sqrt{\frac{\sigma_{N+\mu}}{W \cdot L \cdot N_{t,f}}} \right) \quad (3)$$

Here $\sigma_{N+\mu}$ describes the noise variability of traps for both number and mobility related effects and is in the order of one [6]. In addition to the local variations also global variations due to manufacturing imperfections have to be considered [12]. Figure 5a) shows the 1/f-noise standard deviation versus device area. In this figure both local (left, small area devices) and global (right, large area devices) variations are seen. In Figure 5b) the standard deviation versus operating conditions is shown. Both graphs show good agreement between model and experiment.

Statistical parameter fluctuations in the total 1/f-noise of analog circuits are often larger than noise variations due to voltage or environmental effects. For accurate estimation of noise related yield in larger circuits with many different noise contributors, Monte-Carlo approaches for circuit noise estimation can give more area efficient results than simple worst case approximations.

1/F-NOISE AND RELIABILITY

For analog circuits the two most important reliability aspects are Negative Bias Temperature Instabilities (NBTI) and Hot Carrier (HC) induced degradation.

NBTI today is the most important thread to the reliability of analog circuits [13, 14]. However no report on the impact of NBTI on 1/f-noise does exist so far. The most likely physical origin of NBTI degradation is the Si-H interface bond breaking and movement of hydrogen ions within the gate-oxide [15]. This mechanism involves interface trap formation. Since the energy of the interface states must be close to the Fermi level to have 1/f-noise relevance, NBTI related 1/f-noise degradation is not necessarily expected. Nevertheless 1/f-noise after NBTI degradation should be monitored, especially when new gate-stack materials are introduced into the CMOS technology.

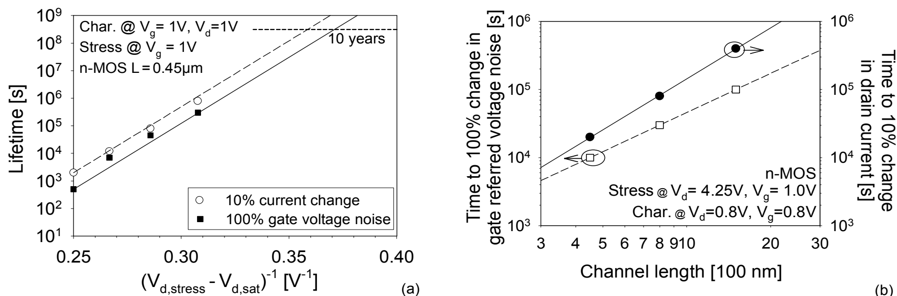

FIGURE 6(a): Lifetime extrapolation for a 100% gate referred voltage noise and a 10% drain current failure criterion. **(b)**: Changes in low frequency noise and drain current of n-MOS transistors after hot carrier stress versus channel length. Process details see [17].

HC damage has frequently been observed in the 1/f-noise characteristics in the past [e.g. 16]. This is also true for operating and stress conditions relevant for analog applications [17]. Hot carrier stress for both p- and n-MOS devices today is mainly caused by interface trap generation between pinch-off and drain. As soon as traps are generated in the oxide close to channel regions where the current density is close to the interface, additional 1/f-noise is resulting. For analog operation in saturation this happens when stress damage generation moves into the region of the pinch-off point [17]. The noise related change in 1/f-noise amplitude $\Delta S_{Vg}(t)/S_{Vg}$ over stress time t approximately follows an effective stress voltage ($V_d - V_{d,sat}$) related power law (Figure 6a):

$$\frac{\Delta S_{Vg}(t)}{S_{Vg}(t=0)} \approx \left(\frac{I_{d,stress}}{W} \cdot \exp\left[\frac{V^*}{V_d - V_{d,sat}} \right] \right)^m \cdot \left[a \cdot t^m + b \cdot t^{n+m} \right] \tag{4}$$

Here $I_{d,stress}$ is the stress drain current, V_d and $V_{d,sat}$ the drain and saturation drain voltage. The other parameters are physics related fit constants [17].

Since hot carrier generation needs a minimum energy, in modern devices with decreasing operating voltages, HC damage is becoming less problematic. However I/O and precision analog devices with higher voltages are incorporated in those technologies. For these devices, HC related 1/f-noise degradation is a concern for reliable analog circuit design. The most important measure to enhance device lifetime in such circuits is to increase the channel length (Figure 6b), but also certain bias conditions [17] may enhance circuit lifetime.

CONCLUSION

We have reviewed the 1/f-noise properties of CMOS devices with emphasis on their application in analog circuits. It is shown that the corner frequency and statistical effects in the 1/f-noise increase for each new technology node. Compact models for the correct description of the statistical effects and the non-equilibrium behavior of the 1/f-noise are discussed. Reliability issues for 1/f-noise in analog designs need to be monitored but are expected to remain non-critical as long as no severe material changes in the device structure are implemented in new CMOS process generations.

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