A Study on Tunneling Current of ONO Films and Data Retention Effects in Flash Memories

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Abstract

In this research, 5 different thicknesses of oxide-nitride-oxide (ONO) inter-poly-gate dielectrics in flash memories are studied. Besides the experiments of analyzing program/erase speeds, various I-V tests have also being conducted to understand the tunneling characteristics of these ONO films. Data retention effects are also investigated by measuring the threshold voltage shifts consecutively up to 200 h of 250 °C baking. All the findings are analyzed and concluded to propose a set of ONO film scaling rules.

KeyWords: Flash Memory, ONO, Nonvolatile Memory, Data Retention.

1. Introduction

Recently, flash memories have been widely employed as non-volatile semiconductor memories in various electronic products such as: IC card, hand-held computer, digital camera, mobile phone and so on. In competing with the hard disk drives and other memories, flash memories must meet the requirements of high integration, fast response, reliability and low power consumption. Hence, the continuance of down scaling is a necessity for advanced flash memories, and the researchers of this field have kept the studies on problems inherited from down scaling hoping to optimize the performance of threshold voltage shift, data retention time, P/E endurance, programming efficiency, program/erase speeds and so on [1, 2].

For the design of advanced flash memories with better characteristics, how to use the oxide-nitride-oxide (ONO) inter-poly-gate dielectric becomes a major concern. The ONO films form a triple layered capacitor structure, which features the high dielectric constant of silicon nitride (Si_3N_4) deposed between two silicon dioxide (SiO_2) films. The structure thus can provide higher program/ erase speeds and better data retention characteristic.

But due to the carriers transportation and trapping mechanisms are complicated and ambiguous [3] in the films, the scaling rule of ONO layer thicknesses has not consolidated. Leaking the consideration of program/erase speeds, Pan and Wu [4, 5], by performing the experiments of data retention, demonstrated that there were three distinct phases of charge loss and suggested that nitride should be thin but both top and bottom oxides should be as thick as possible. Lin [6] fascinated in proving the carriers transportation and trapping mechanisms of ONO films and only provided some trivial hits for the scaling rule of ONO layer thicknesses. Liu [7] focused on charge trapping of thermally nitrided oxides, which built the foundation of the process. Kobayashi [8] suggested that bottom and top oxides should be larger than 3nm in order to prevent charge loss. Mori [9] and his colleagues, by considering charge retention effects, proposed bottom oxide should be 4 nm and top oxide should be greater than 6 nm.

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In this research, to bypass the interesting problems of finding the ways of carrier transportation and trapping, we focus on the effects of various ONO combinations through the experiments of program/erase speeds, I-V performance and device's data retention. The efforts then put on to finding out the solution for the optimal thickness combinations of ONO dielectric films. It is hoped that, through the practical methodology, the experimental results and analyzed findings are applicable in the design and fabrication of future flash memory devices.

2. Specimens

Table 1 lists 5 different ONO films of inter-poly-gate dielectrics, which were implanted into 5 different specimens of floating-gate flash memory cells. Based on 0.25 μm technology with width/length equals to 0.5 μm/0.5 μm, there are fabricated in the following process. A 40Å bottom oxide in the ONO stack is first deposited using high temperature LPCVD at 800°C. A 160 Å, 140 Å or 82 Å CVD nitride is then deposited. Lastly, a 40Å top oxide is formed by a 950°C oxidation of the nitride, which is added to specimens 1, 3 and 4. Another top oxide is deposited on specimens 2 to 5 by using high temperature CVD process. These specimens have special designed to have floating gate wired to facilitate the measurement of ONO film properties.

To stabilize the threshold voltage shift in data retention, all specimens are processed to have 40Å thickness as suggested in Kobayashi [8] and Mori [9]. Also note that the equivalent thickness in Table 1 refers to pure oxide thickness having equal capacitance, which is certainly obtained from measurement. From design viewpoint, the equivalent thickness to be calculated before fabrication is a necessity. From the consideration of capacitors in serial and allowing 10% of process variation, we can obtain the equivalent thickness as being proved in this research as

$$t_{eq} = \frac{3.9}{4.3}\, t_{OCVD} + t_O + \frac{3.9}{7.5}\, t_N \qquad (1)$$

Where t_{OCVD} is the thickness of oxide film prepared by LPCVD process and 4.3 is its dielectric constant.

t_O is the thickness of thermal oxide film and 3.9 is its dielectric constant.

t_N is the thickness of nitride film and 7.5 is its dielectric constant.

3. Experiment Facility

The system setup for the I-V and transient characteristics measurement of flash memories is illustrated in Figure 1. Based on the PC controlled instrument environment via HPIB interface (GPIB, IEEE-488), complicated and long-term characterization procedures during analyzing the intrinsic and degradation behavior in flash memory cells can be achieved. By referring to Figure 1, the characterization equipment, including semiconductor parameter analyzer HP-4156A, pulse generator HP-8110A, switch matrix mainframe Keithley-707 and probe station, provides an efficient capability for measuring the device I-V characteristics and carries out the flash cell program/erase operations.

4. Experiments and Discussions

4.1. Program/erase Speed Experiments

Figure 2 shows the program method and speeds of

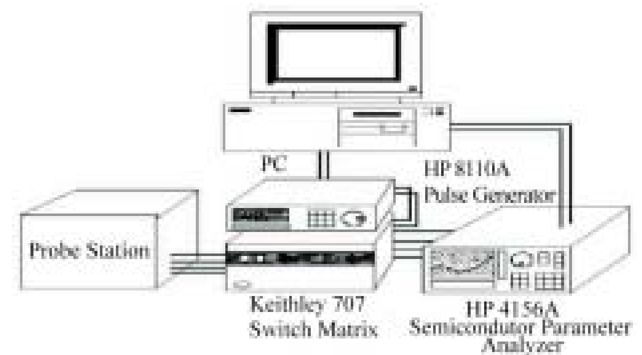

Figure 1. System setup for I-V and transient characteristic measurements of flash devices.

Table 1. The ONO compositions

Specimen	Top oxide	Nitride	Bottom oxide	Equivalent Thickness
1	40A (thermal)	160A	40A(CVD)	163.17A
2	40A (CVD)	140A	40A(CVD)	141.62A
3	80A (thermal+CVD)	140A	40A(CVD)	170.31A
4	80A (thermal+CVD)	82A	40A(CVD)	144.14A
5	40A (CVD)	82A	40A(CVD)	121.05A

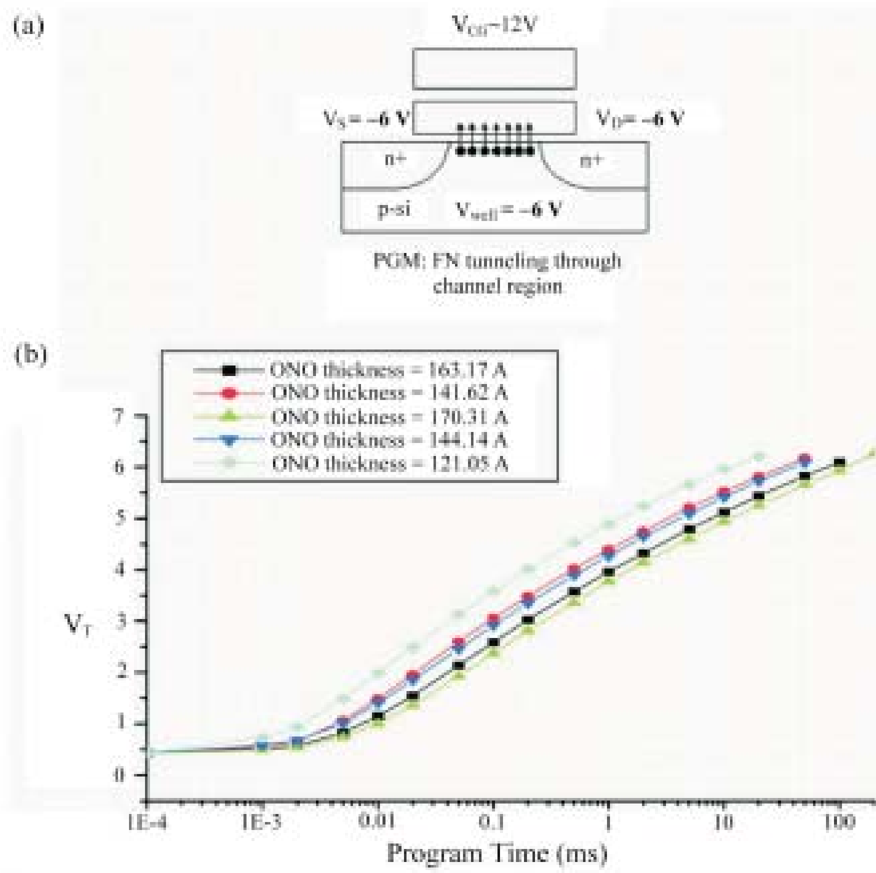

Figure 2. (a) Channel FN tunneling; (b) Program speed comparison between different ONO compositions.

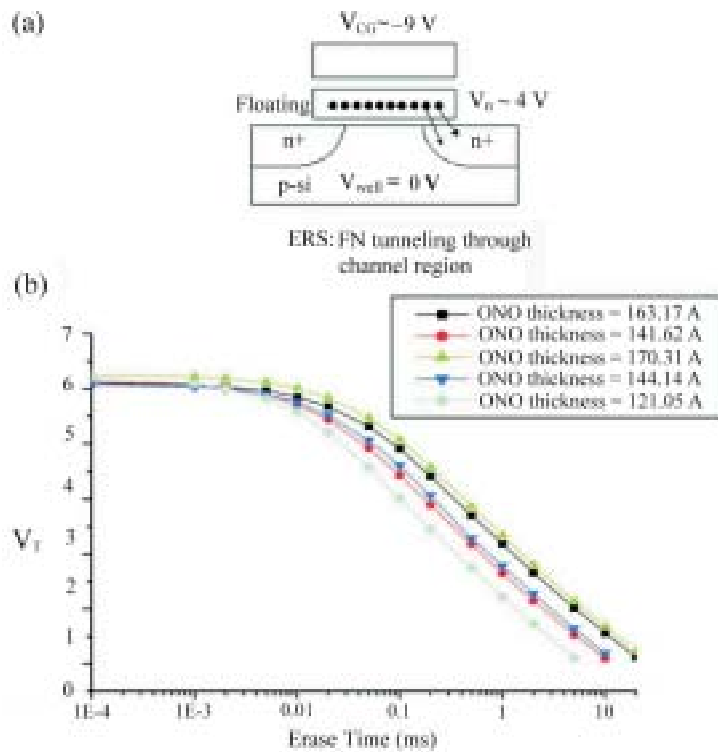

Figure 3. (a) Drain side FN tunneling; (b) Erase comparison between different ONO compositions.

the various ONO compositions. Based on the DINOR-type array operations, the programming operation is "channel FN tunneling". Figure 3 shows the erase method and speeds of the various ONO compositions. The erasing operation is "drain side FN tunneling". As can be expected, the thicker the equivalent film is the slower the program speed. Similar results can be observed in erase operations as the thicker consumes more time in pull out the charges.

Besides judging from equivalent thickness, it is proved in this research that the program coupling ratio (PCR) and erase coupling ratio (ECR) provide good assessment of program/erase speeds. These two quantities are calculated from capacitors of floating gate to control gate, source, channel and drain as defined in Figure 4 as

$$C_{total} = C_{CG} + C_{FG} + C_S + C_D \tag{2}$$

$$DCR = \frac{C_D}{C_{total}} \tag{3}$$

$$PCR = \frac{C_{CG}}{C_{total}} \cong \frac{C_{CG}}{C_{CG} + C_{FG}} \tag{4}$$

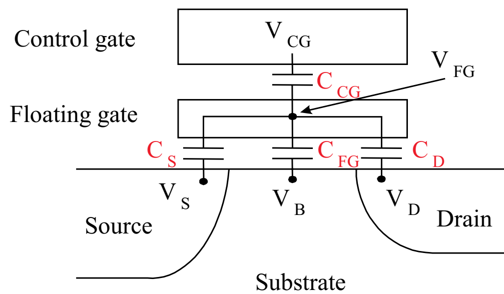

Figure 4. The flash memory cell and its capacitors.

$$ECR \cong \frac{(V_{CG} \times PCR - V_D \times DCR)}{V_{CG} - V_D} \tag{5}$$

4.2. I-V Characteristics

Figures 5 and 6 exhibit the results of double I-V measurements, which recorded the I-V characteristics (−18 to 18 volts was applied to control gate as floating gate connected to 0 volt) of the ONO films before and after stressing. The stress condition is −1 mA/cm^2 (Negative DC power was applied to control gate while floating gate connected to 0 voltage) for 500 seconds. The high voltage I-V measurements before and after stressing are necessary for imitating the program/erase operation of flash memory and accelerating the degradation of dielectrics.

Thus the double I-V measurements reveal some interesting facts about carrier migration in ONO dielectrics, which then influences the characteristics of data retention. The facts and their discussions are listed as follows:

1. From Figure 5 we found that curves can be separated into two groups, those with thermal oxide and their counterpart, for curves 1, 3, 4 apparently lower then curves 2, 5 after control gate voltage larger then -7 volt. This implies that thermal oxide film provides the highest resistance to carrier transportation in ONO films.
2. Comparing Figures 5 to 6, all curves have certain degree of upward movements implying certain degradation happened after stressing. This stress induced leakage current (SILC) should be responsible for data retention problem especially for the case after many cycles of program/erase operations. But the curves 1, 3, 4 moved most obviously to catch curves 2, 5 before control gate voltage reaches 3 volts. This

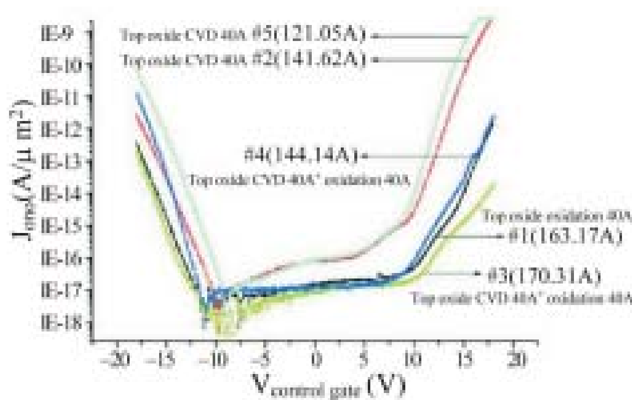

Figure 5. The results of double I-V measurements, before stressing.

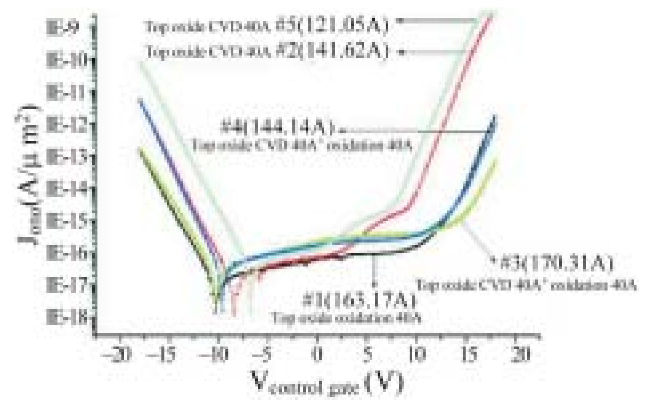

Figure 6. The results of double I-V measurements, after stressing -1mA/cm^2 for 500 seconds.

means thermal oxides suffer from stressing heavier then their counterpart. But after control gate voltage larger than 3 volts, the thermal oxides still efficiently resists the carrier penetration.

3. Comparing curve 2 to 5, 3 to 4 in both figures, they exhibit nitride film do provide resistance to carrier migration, but even comparing to the equivalent thickness of thermal oxide films, the resistance is not significant enough.

4.3. Data Retention Experiments

Figure 7 shows the threshold voltage decreases of programmed flash cells vs. 250°C baking time, up to 200 h, with different ONO compositions. No external bias was applied during the baking. Several key features have been observed and discussed below.

1. As found in Pan and Wu [4, 5], three distinct phases of charge loss can be differentiated, indicating different species or different mechanisms for each phase; but the timing and the observation are not quite the same. There are an initial fast first phase (less than 1 h), a transition second phase (up to about 50 h), and a non-saturating long term third phase shifts.
2. For the first phase, the threshold voltage shifts very quickly, and the shifting is clearly a strong function of nitride thickness as the shifting decreased from curve 1 to 2 and 3 to 4 and 5. This suggests that V_t shift should be attributed to charge movement within the nitride. The thicker the nitride film is the quicker the V_t shifts.
3. For the third phase, the thermal oxide plays a significant role in resisting long term charge loss, as can be observed from curves 1, 3, 4. To avoid misleading by the first and second phases, the V_t decreasing rate has been calculated and shown in Table 2. The same results also confirm that thermal oxides playing dominant role in long term data retention.
4. For the second phase, dominant roles are changing from nitride to CVD and thermal oxides.

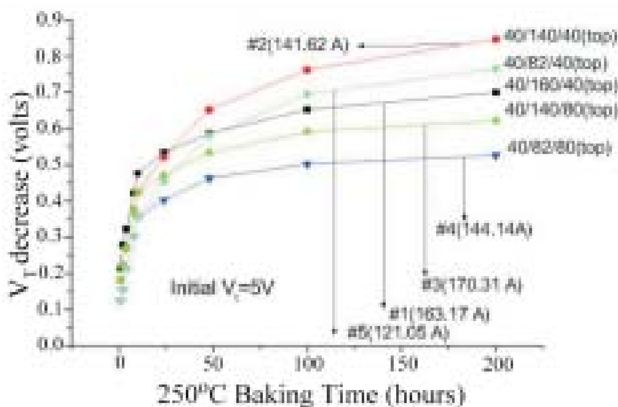

Figure 7. Threshold voltage decreases versus 250°C baking up to 200 hours for programmed flash cells with different ONO compositions.

Table 2. The slopes of 50 hours to 200 hours baking time with different top oxides

	Specimens	Slope (50 h to 200 h)
1	1 163.17A (top oxide: 40A(thermal))	7.547E-4
2	2 141.62A (top oxide: 40A(CVD))	1.296E-3
3	170.31A (top oxide: 80A(thermal+CVD))	5.923E-4
4	144.14A (top oxide: 80A (thermal+CVD))	4.234E-4
5	121.05A (top oxide: 40A(CVD))	1.235E-3

5. Conclusions

It is always interesting and profound to clarify the trapping and tunneling mechanisms in the dielectric films of MOSFETs and flash memories because there are important in understanding the dielectric leakage, degradation and breakdown, which are then critical in further scaling down of those electronic devices. But the manifold researches do not lead to a consensus [3]. In this research, however, we bypass the above attractive questions. Base on the experiments results, we can provide some suggestions to the current flash memory designers to optimize their ONO compositions.

1. A rule of thumb is the program/erase speeds can be estimated before fabrication using the equivalent thickness calculation as equation (1) and prior flash memory data. Hence, the total thickness of ONO films has a constrain.
2. The bottom oxide should be at least 4 nm according to Mori [9]. This research is consistent with that result.
3. The thermal oxide provides best resistance to tunneling current and thus most useful in long term data retention although it is not so helpful in accelerating program/erase speeds.
4. The use of nitride film can greatly reduce the program/erase time, but it is responsible for all phase,

especially in the first phase with large quantity, of data loss.

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