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The Flash memory cell for the nodes to come: material requirements from a device perspective

B. Govoreanu*, J. Van Houdt, M. Jurczak

IMEC, Kapeldreef 75, 3001 Leuven, Belgium
*E-mail: govorean@imec.be, Tel. +32-16-281337

The quest for mass storage and the diversity of end-user applications led to an aggressive scaling of the NAND Flash memory. A key factor to its success is the high density integration potential, which allows fabrication of large memory arrays. Reduction of the feature size below 40 nm may, however, require modifications of the conventional floating gate (FG) cell architecture, due to lack of physical space between neighboring cells [1], which no longer allows wrapping of the control gate (CG) over the floating gate (FG). This has consequences on both **intra-** as well as **inter-cell** levels.

Intra-cell level impact

An immediate implication of the cell planarization [2] is that the CG to FG coupling capacitance is seriously reduced. To restore it, drastic scaling of the interpoly dielectric (IPD) needs to be considered. As the ONO scalability to below 10 nm EOT is not feasible, introduction of the high-k-based IPD's is a must.

High-k materials are known for relatively high defect densities [3]. In order to be useable in Flash memory cells, they need to meet a set of performance and reliability requirements. Apart from the dielectric constant, which ensures a good FG to CG electrical coupling, large bandgap and band offsets (relative to Si) are needed, to provide sufficient margin for the extremely low leakage current, down to 10^{-16} A/cm^2, imposed by the charge retention requirement.

The success of an implementation requires combining efforts for defect density reduction and careful optimization of the thermal budget with FG/IPD interface engineering, IPD/CG interface optimization and eventual use of metal gates. Furthermore, good control of defect density may eventually enable introduction of more innovative structures, e.g. considering replacement of the tunnel oxide [4].

Inter-cell level impact

One of the most severe inter-cell issues is the cell-to-cell interference [5], where several neighboring cells affect the potential of a floating gate in a string, hence altering its Vt. This becomes increasingly important, especially given the NAND array architecture and also taking into account the need for a tight Vt control, required for multilevel cell (MLC) operation.

One possible route to alleviate this effect is to use low-k dielectrics or even air gaps [6] for cell-to-cell isolation. An alternative is to aggressively scale down the FG height. Recent results show that with a smooth, well controlled silicon deposition process [7], the performance and reliability of the FG cells remain unaffected for FG thicknesses scaled down to as thin as 15 nm.

Charge trapping cells

Seen as a natural extension of the FG cell for the future technology nodes, the charge trapping (CT) cells overcome several of the problems inherent to FG structures, such as charge loss vulnerability to a single defect path in the tunnel/blocking dielectrics, cell-to-cell interference, etc. In spite of a simpler process, key to a low-cost product, the CT cell requires optimization of the whole stack [8-10], as well, and its implementation in a state-of-the-art NAND Flash technology is not straightforward.

In this paper, we review some of the above-mentioned issues from a device operation viewpoint, when considering various candidate high-k materials [9-12]. Several points of attention for a successful continued scaling of the Flash memory cell are discussed.

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