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Phosphorus Pile-Up Model for SiO_2-Si Interface of p-Channel MOSFETs

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Dopant distribution is very important when simulating the performance of LSI devices. Therefore dopant segregation should be taken into account when it occurs to the extent that it affects this distribution. This paper suggests that for p-channel MOSFETs the "phosphorus pile-up phenomenon" should be taken into account and proposes a simulation model.

It is conventionally understood that after annealing and oxidation during device fabrication phosphorus dopant finally distributes at the SiO_2-Si interface. We found, however, that the conventional model (Fig. 1(a)) cannot reproduce the threshold voltages of p-channel MOSFETs shown in Fig. 1(b), where each set of process conditions is shown in Table 1. Phosphorus is used as a dopant impurity in the n-well region of p-channel MOSFETs. Oxide removal occurs four times during the fabrication of MOSFETs. Some reports show that a considerable amount of phosphorus piles up at the SiO_2-Si interface [1-3]. A recent report shows that this pile-up layer can be removed by removing the oxide film [3]. It is hard for the conventional segregation model to deal with this phenomena.

We use the assumption of phosphorus pile-up in the interlayer [4, 5] shown in Fig. 2(a), where an interlayer of 0.5 nm absorbs the phosphorus with its specified segregation coefficients and is removed by oxide removal. This model reproduces the threshold voltages of p-channel MOSFETs well (Fig. 2(b)). The segregation coefficients are set to be

$[C]_{Si}/[C]_{interlayer} = 7.2 \exp(-0.7/kT)$ for Si and the interlayer interface and

$[C]_{interlayer}/[C]_{SiO_2} = 4.2 \exp(0.7/kT)$ for the interlayer and SiO_2 interface,

where $[C]$ is the concentration of phosphorus in each layer, k is the Boltzmann constant, T is temperature, and the temperature dependence is derived from empirical equation based on experimental data [3]. The product of these coefficients is 30 and is equal to the segregation coefficient that is generally used for Si/SiO_2 [6].

Figure 3 shows the concentration of phosphorus in the n-well. The simulated result agrees well with the experimental one, so the proposed model is appropriate.

Authors are thankful to Drs. Wada, Amakawa, and Kinoshita of Toshiba Corporation for their providing simulation software and fruitful discussions.

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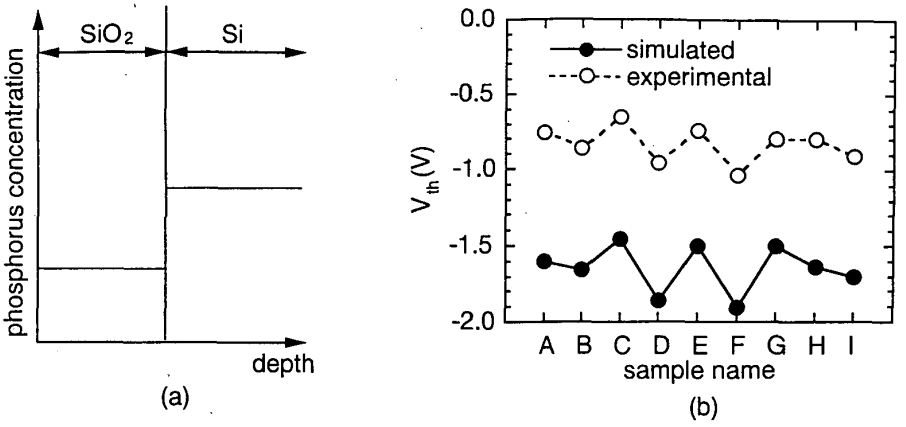

Fig. 1. (a) Schematic diagram of final phosphorus distribution based on ordinary model.
(b) Simulated results for threshold voltage of p-channel MOSFETs.

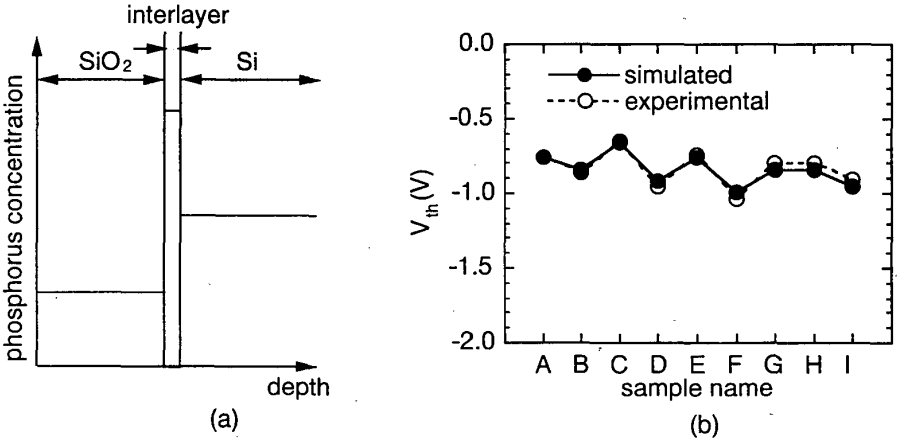

Fig. 2. (a) Schematic diagram of proposed phosphorus pile-up model.
(b) Simulated results for threshold voltage of p-channel MOSFETs.

Table 1. Process conditions for samples.

sample name	t_{ox} [nm]	implantation dose [cm^{-2}]	
		P (n-well)	B (channel)
A	11.0	3.58e13	3.20e12
B	11.0	3.58e13	2.92e12
C	11.0	2.88e13	3.20e12
D	11.0	4.80e13	3.20e12
E	11.0	2.88e13	2.92e12
F	11.0	4.80e13	2.92e12
G	9.0	3.58e13	2.92e12
H	9.0	4.80e13	3.44e12
I	9.0	4.80e13	3.00e12

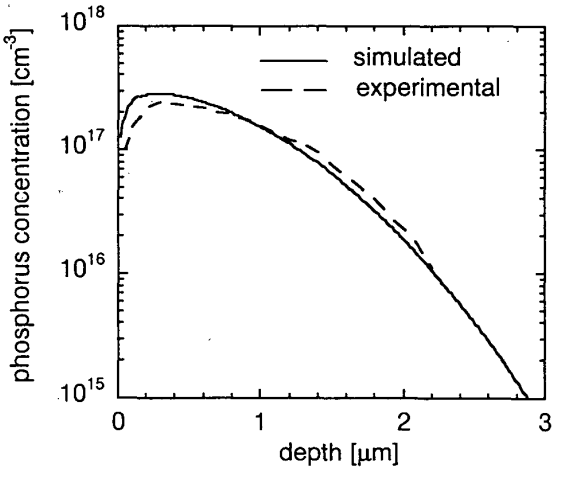

Fig. 3. Concentration of phosphorus in N-well.