DATA - CLOCK SETUP AND HOLD TIMES MARGINS CORRECTION METHOD IN HIGH SPEED SERIAL LINKS

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ABSTRACT

A method of serial links output data and clock signals setup and hold times correction is presented in this paper. The proposed architecture produces a corrected clock which has enough setup/hold time margins respect data signal over PVT, which is needed to avoid data errors and setup/hold violations during the further operation with data. The presented correction mechanism can be used in the special input/output circuits of several standards such as Peripheral Component Interconnect (PCI), Universal Serial Bus (USB), Double Data Rate (DDR), etc.

Keywords

Serializer, Voltage Controlled Delay Line (VCDL), PVT, Clock Corrector (CC)

1. INTRODUCTION

In high speed systems (Fig. 1) and interfaces [1], where signal pulse width becomes small, it needs data sampling clock to be in the middle of data signal for prevent setup/hold times violations and, hence, data errors. For high speed signal processing setup/hold times are important factor and its effects cannot be ignored. When data signals in the inputs of Serialaizer (Fig. 2) come with different delays as a result in the output can lose the data, because data and clock paths are different and it can cause setup/hold violations. In general setup/hold time is the minimum amount of time the data signal should be held steady before/after the clock event so that the data are reliably sampled by the clock. One of the main factors data/clock signals spreading over PVT of high speed devices is rise/fall times and propagation delays distribution due to process variation.

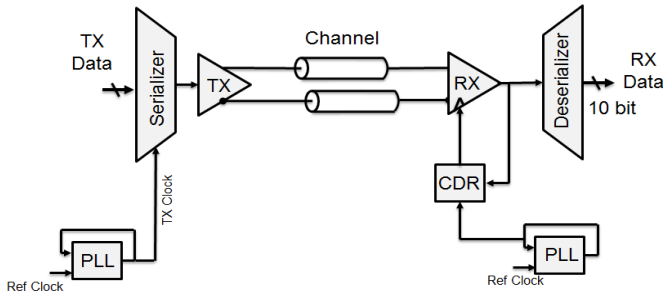


Fig.1. *High Speed Serial link*

It will cause to exclude data lost and setup/hold violations. As a result of the mentioned phenomena, the system may fail to function under some operating conditions such as high temperatures or over-voltages.

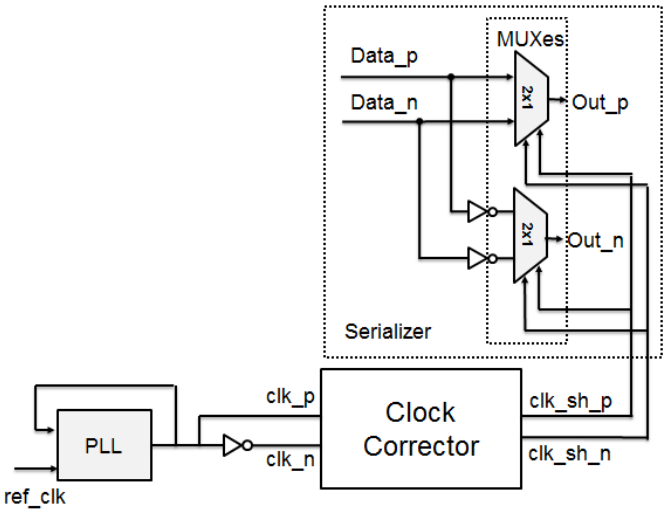


Fig.2. *Serializer/Corrector circuit structure*

In Fig.3 shown clock/data timing diagrams from which it's clear that the data frequancy is two times slower than the clock signal.

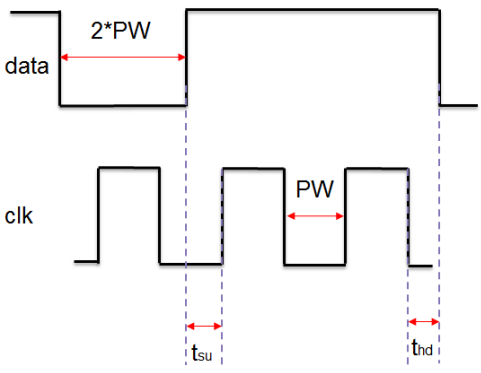


Fig.3. *Timing diagrams with Setup/Hold times*

where PW is the pulse width of signal, t_{su} is setup and t_{hd} is hold times. The proposed method dynamically corrected setup/hold times between Serializer clock and data signals.

2. SETUP/HOLD TIMES CORRECTION CIRCUIT ARCHITECTURE

The structure of proposed setup/hold times Correction Method is presented in Fig.4.

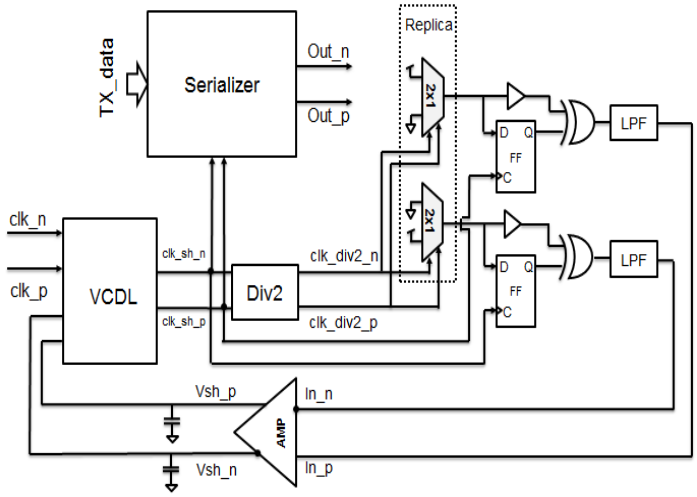


Fig.4. *Setup/Hold time correction circuit structure*

In this architecture Replica part needs corrected clocks, which dynamically fix data signal setup/hold times in the Serializer. For this goal we use Replica in the loop of CC circuit.

Correction circuit contains both analog and digital blocks. In this structure analog blocks are Low Pass Filters (LPF), Amplifier and VCDL. Digital parts are presented with MUXes in replica of CC loop and in Serializer stage.

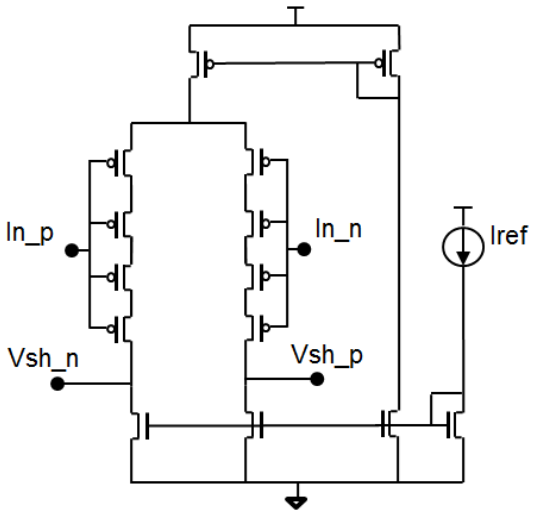


Fig.5. *Delay Control Amplifier*

As we need to have an amplifier that is noise stable and provides integrated voltages on the outputs depended on its inputs, we chose the following architecture in Fig.5.

For that purpose the input diff pairs have a large channel lengths which is implemented using sequential transistors connected with each other. To have integrated outputs capacitance loads are connected to the outputs of amplifier (Fig.5). Delay elements (Fig.6) are controlled by Diff amp outputs Vsh_p and Vsh_n.

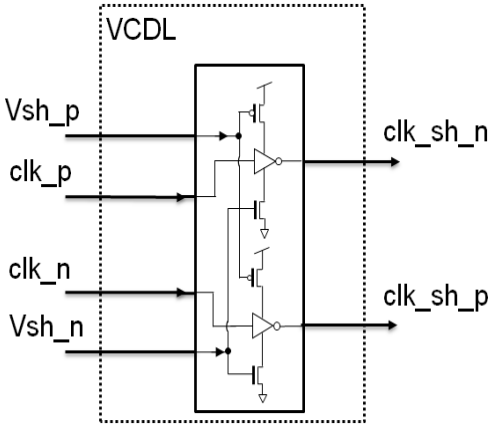
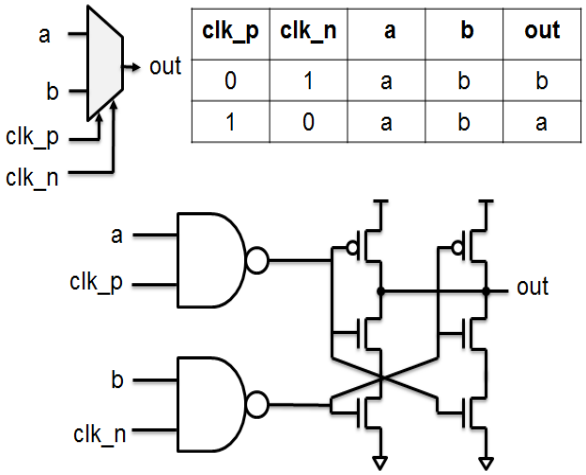


Fig.6. *VCDL circuit structure*

As controlled clocks are differential signals the represented MUXes are operating with 2 control inputs.



clk_p	clk_n	a	b	out
0	1	a	b	b
1	0	a	b	a

Fig.7. *2x1 MUX Serializer*

3. OPERATION PRINCIPLE AND CORRECTION

Block diagram on Fig.8 has been proposed to attain a corrected clock signal nearly to middle of data signal. As it

is known the average DC value of a signal is proportional to its Duty Cycle. Before applying PLL clocks to the Serializer and Deserializer, they are being corrected with the negative feedback system.

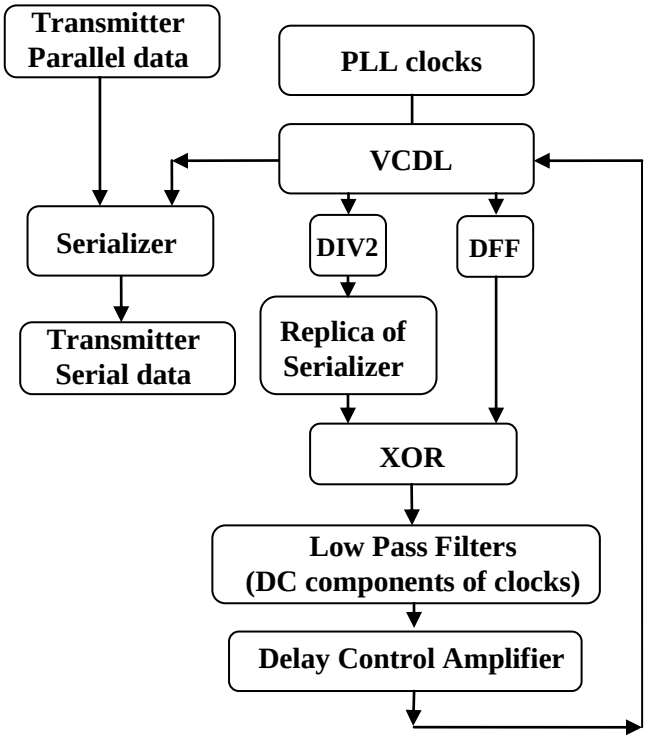


Fig.8. *Block diagram of correction method*

As it was mentioned above the clocks that are needed for serializing data are coming from Phase Locked Loop (PLL) through lines that can affect propagation delays of these clocks over PVT and it can bring setup/hold violations.

CC process starts from VCDL block (Fig.8). VCDL has 2 voltage controlled delay inverters that are changing their output currents when Delay control amplifier changes its output voltages (Vsh_p and Vsh_m). After several iterations, when loop is locked, VCDL generates fixed clock signals which is middle of data signal and has no setup/hold violations.

The output signals of XOR gates are passing through the LPF and so the DC component of this data is used as inputs of Delay Control Amplifier (DCA). As it was said formerly the DCA input diff pair has sequentially connected transistors with large lengths and widths. Large lengths are for noise stability and large widths are for high gain. Besides as LxW is large enough, and taking into account the fact that external capacitor need much are, the capacitor of LPF is implemented here using the input diff pair of DCA.

4. SIMULATION RESULTS

Simulations have been performed using circuit level simulator Hspice[4] for 20 PVT corners, including SS (slow-slow), TT (typical-typical), FF (fast-fast), SF (slow-fast), FS (fast-slow) with supply voltage and temperature variations to estimate accuracy (Setup/Hold time margins (t_{su}/t_{hd})) and the settlement time (t_{set}).

Fig.10 (a) shows CC settlement results for TT (55^{o}) typical corner. It is seen that amplifier's outputs is going to be settled after 42ns when setup time is about 98ps (from 100ps). In this case Vsh_p=0.512V and Vsh_n=0.510V.

Fig.10 (b) and Fig.10 (c) show simulation results for, respectively, FF(-40^{O}) and SS(125^{O}) main PVT corners.

Taking into consideration that USB3.0 protocol works with the 5 Gb/s data rate signal, which means that Data have 400ps pulse period and 200ps pulse width, we have put internal specification for t_{su}/t_{hd} the 25% of period, i.e. after clock can be considered as corrected, when t_{su}/t_{hd} is less near 100ps. In USB3.0 specification book t_{su}/t_{hd} min value defined as 20ps. The next important parameter is Settling time (ST), which shows the time when CC is locked. Table 1 shows results for 3 main corners.

TABLE I. Simulation results of the three main corners

Corner	t_{su}/t_{hd}		Settling time
	N	P	
Unit	ps	ps	ns
TT(55)	98.05/100.93	98.7/100.12	42
FF(-40)	108.08/90.7	107.5/91.32	40
SS(125)	88.05/110.7	89.7/112.3	46

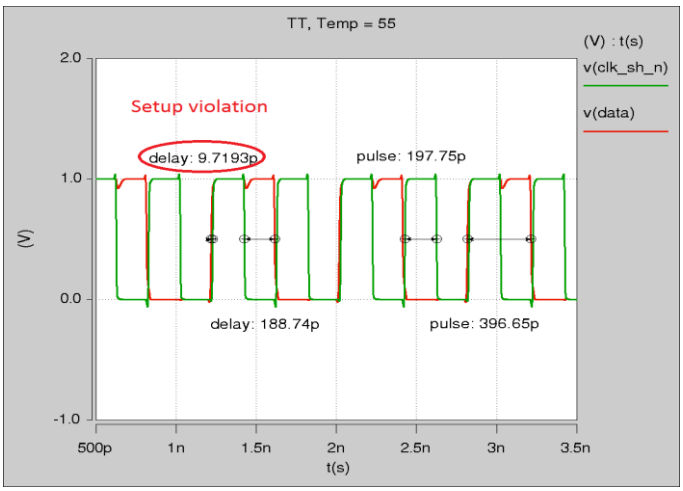
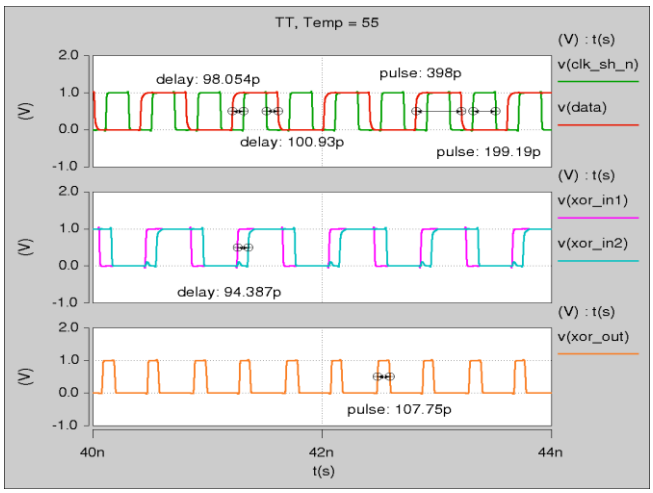
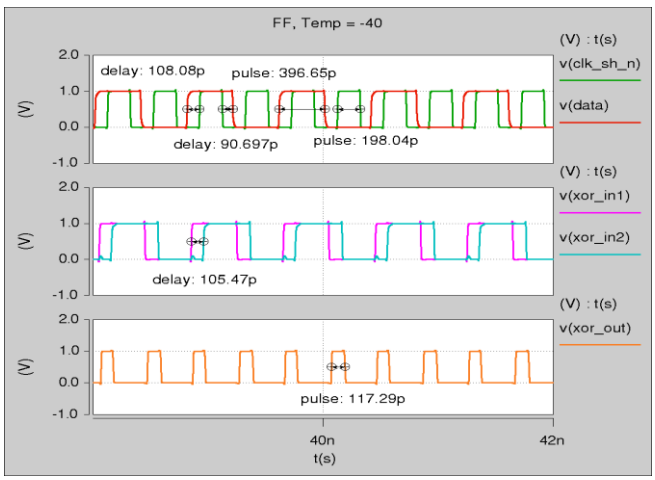


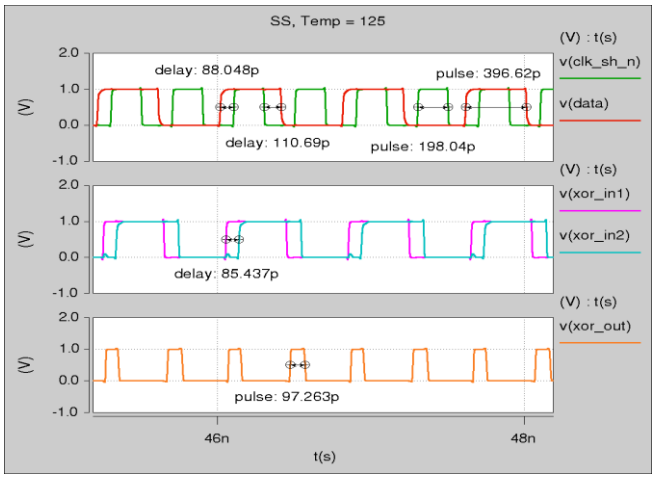
Fig.9. Simulation results in TT case with setup violation



TT (a)



FF (b)



SS (c)

Fig.10. *CC settlement results for TT (a), FF (b) and SS (c) corners*

Fig.9 shows simulation results before setup/hold correction for TT. Table 1 shows duty cycle improvement after correction.

5. CONCLUSIONS

A circuit designed for Serializer final serializing stage output data and clock setup/hold signal correction. The closed loop system with negative feedback integrates clock signals and provides stable signals. Average Deviation for TT corner is equal to 0.085%, after 42ns of settling time, the t_{su}/t_{hd} has the value of 98ps, where the minimum spec of setup/hold time margins from the USB3.0 specification book is 20ps.

The approached method can be implemented for input/output protocols such as USB, PCI, etc.

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