

From Chip to Cooling Tower Data Center Modeling: Influence of Chip Temperature Control Philosophy¹

Ed J. Walsh

e-mail: edmond.walsh@ul.ie

Thomas J. Breen

Stokes Institute,
University of Limerick,
Limerick, Ireland

Jeff Punch

CTVR, Stokes Institute,
University of Limerick,
Limerick, Ireland

Amip J. Shah

Cullen E. Bash

Hewlett-Packard Laboratories,
Palo Alto, CA 94304

The chiller cooled data center environment consists of many interlinked elements that are usually treated as individual components. This chain of components and their influences on each other must be considered in determining the benefits of any data center design and operational strategies seeking to improve efficiency, such as temperature controlled fan algorithms. Using the models previously developed by the authors, this paper extends the analysis to include the electronics within the rack through considering the processor heat sink temperature. This has allowed determination of the influence of various cooling strategies on the data center coefficient of performance. The strategy of increasing inlet aisle temperature is examined in some detail and found not to be a robust methodology for improving the overall energy performance of the data center, while tight temperature controls at the chip level consistently provide better performance, yielding more computing per watt of cooling power. These findings are of strong practical relevance for the design of fan control algorithms at the rack level and general operational strategies in data centers. Finally, the impact of heat sink thermal resistance is considered, and the potential data center efficiency gains from improved heat sink designs are discussed. [DOI: 10.1115/1.4004657]

Keywords: Data center cooling, thermal management, chip to cooling tower, energy efficiency, heat sink

1 Introduction

Data center cooling has emerged as a key problem in the long term objective of realizing sustainable large scale computing as illustrated by Ref. [1]. Reference [2] notes that electricity costs for these facilities in 2005 were in excess of seven billion dollars, which was about 1% of the world's entire electricity production. Importantly over half of the energy use is attributed to cooling the facilities to allow high performance of the systems. As well as cost issues associated with data center cooling that the data center manager must address, another major issue is the availability of power capacity in many regions for new data centers. In the near future it is anticipated that data centers will consume over 2% of the total electrical energy produced within the US. Thus understanding and improving the energy efficiency of data centers is critically important from a cost as well as sustainability perspective to obtain the maximum computing per watt of energy consumed, in both computing and cooling, remains a fundamental challenge to the industry. Figure 1 shows a diagram of the main infrastructure components within the thermal chain of a chiller cooled data center. Although the current analysis is of an air cooled data center with chillers, the method is equally applicable to liquid cooled data centers, and those without chillers. Much work has addressed the issues of improving the energy consumption of individual components, influence of recirculation and layout in the data center [3–7]. While this approach is very useful and worthwhile, within the data center environment there are strong interactions between individual components, and the influ-

ence of one component on the others is not always clear, for example, how does changing the temperature of the return water within the chiller influence the fans, computer room air conditioning (CRAC) units, and chilled water flow rates within the IT room. Therefore, a clear need exists to consider the entire system in a single model and provide a global performance measure. Ultimately, the designer needs knowledge of how changing the layout or varying the thermal constraints would influence the entire system. For example, if the chip temperature is reduced or increased by 1 °C, what influence will that have on the electricity meter? A good objective is to maximize the computing power, while minimizing the cooling power within a data center, and hence the concept of a grand coefficient of performance (COP_{Grand}), defined as the ratio of total power to cooling power, provides a measure of what economic savings can be expected with changes in the thermal chain.

Reference [8] developed a model for the IT room to external ambient conditions and used the model of Ref. [9] to provide some initial validation; however, the model of Ref. [8] did not consider the influence of thermals and fluid flow inside the rack. This paper is focused on heat sink temperature and hence indirectly on processor temperature, within the rack and the influence that different fan and temperature control strategies have on the COP_{Grand} . Heat sinks are generally designed to meet the thermal requirements of processors for a given ambient to heat sink temperature difference, usually represented by the so called thermal resistance of the package. This approach works well for keeping chips operating within their design parameters and is very appropriate at the laptop or personal computer level where the heat is simply dumped to ambient and no further cooling costs are incurred by the owner. However at the data center level, the heat dissipated by each package must be extracted from the room and transferred to the external ambient by the input of high grade electrical energy through the thermal chain of Figure 1. The current literature does not comprehensively address the influence of the

¹© 2010 IEEE. Reprinted with permission from the "12th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)," 2010.

Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the JOURNAL OF ELECTRONIC PACKAGING. Manuscript received April 7, 2010; final manuscript received May 9, 2011; published online September 21, 2011. Assoc. Editor: Saurabh Shrivastava.

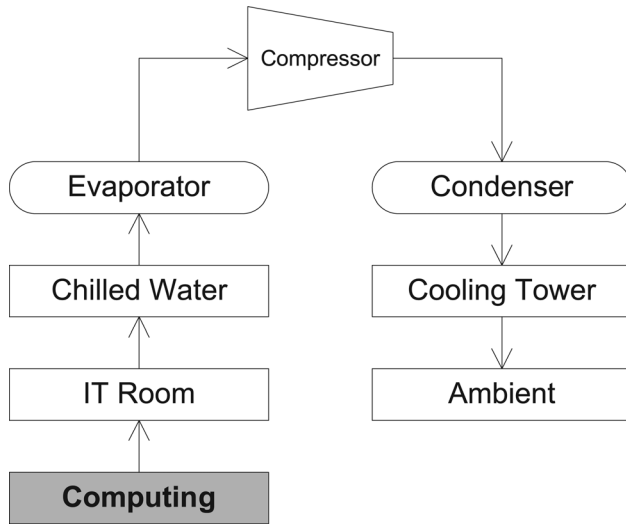


Fig. 1 Elements within the data center

interlinked components of the data center cooling infrastructure from chip to cooling tower. We investigate the condition where the inlet rack temperature is increased in the data center, as this is one of the current methodologies for increasing efficiency, which results in increased fan speed to achieve a heat sink temperature in order to ensure that the electronics continue to operate within their design constraints. The temperature of the heat sink is related to the manufacturer's specifications for the control of fan speed with increasing chip temperature. It is found that the strategy of increasing inlet temperature to improve COP_{Grand} may not be a robust methodology and that a strategy of maintaining a high heat sink temperature should provide an increased COP_{Grand} .

2 Modeling Heat Sinks in Rack With Varying Inlet Conditions

At design conditions for a rack, where the inlet temperature and mass flow rate are fixed, the various components within the system will operate within the designed temperature specifications. However, variations in rack inlet temperature will require alteration of the flow rate to remain within the thermal constraints or to avoid over cooling of the rack. Rather than consider every chip within the rack, the assumption is made that the hottest package will need to be maintained within its thermal constraints while a fixed heat flux is applied. Practically, this constraint means that the user cannot allow any component in the rack to fail. Two extreme cases may be considered when varying the inlet temperature: first where the chip temperature increases linearly with the inlet temperature and second where the chip temperature is maintained at a fixed temperature. To realize the result of these two conditions the scaling of heat sinks must be considered in detail. For any given heat sink where the surface area is constant and assuming that the fin efficiency is constant, the product of the heat transfer coefficient and the heat sink to inlet temperature difference must yield a constant value for all inlet conditions to remove the same amount of heat from the chip. Therefore, as the heat sink to inlet temperature difference increases the heat transfer coefficient may be reduced and vice versa.

In the following analysis, the thermal performance of a heat sink—simplified as channel flow—is expressed as a function of flow rate in order to allow scaling. Similar scaling to flat plate flows has been experimentally correlated for jet flows by Ref. [10], and hence the following model can be expected to provide reasonable results for a wide range of heat sink types. Within a heat sink channel the fully developed region in laminar flow heat sinks can be expressed as

$$Nu_{ITD(Developed)} = \frac{1}{4L^*}; L^* = \frac{x}{D_h Pr Re} \quad (1)$$

based upon a simple energy balance across a channel and isothermal wall conditions. For the developing region in parallel finned heat sinks the Nusselt number relationship originally correlated by Ref. [11] can be expressed as

$$Nu_{ITD(Developing)} = \frac{1}{\left(\frac{\sqrt{L^* Pr^{\frac{1}{6}}}}{0.664}\right) \left(1 + 7.3 \sqrt{Pr L^*}\right)^{-\frac{1}{2}}} \quad (2)$$

where the Nu_{ITD} is the Nusselt number based on inlet temperature difference. The Nu_{ITD} for finned heat sinks where the flow is developing and fully developed can be represented using the intersection of asymptotes method as developed by Ref. [12] to give

$$Nu_{ITD} \approx \left\{ [4L^*]^3 + \left[\left(\frac{\sqrt{L^* Pr^{\frac{1}{6}}}}{0.664} \right) \left(1 + 7.3 \sqrt{Pr L^*} \right)^{-\frac{1}{2}} \right]^3 \right\}^{-\frac{1}{3}} \quad (3)$$

This equation represents the developed and developing flow asymptotes. The hydraulic diameter is chosen as the characteristic length scale as it allows heat sinks of any aspect ratio to collapse to this single equation. The asymptotic correlation indicates a transition to the fully developed flow conditions at $L^* D_h \approx 0.055$, which also provides the reference datum for the heat sink scaling in this work, as it represents an optimum condition where thermal boundary layers merge at the exit of the heat sink. Figure 2 shows the intersection of asymptotes, and the design point graphically, where both asymptotes and design point are labeled.

For an air cooled rack where the geometrical features of the heat sinks are fixed, Eq. (3) can provide the scaling relationship between h_{ITD} and the Reynolds number of the flow. Since variations in Prandtl number are small over the temperature range of interest, they can be assumed negligible.

From applying the reference conditions in Table 1, any heat sink may be scaled to achieve constant heat dissipation by applying the constraint of

$$h_{ITD}(T_{HS} - T_{in}) = const \quad (4)$$

Importantly, as this constraint will only be used for scaling, the actual values of h_{ITD} or area of the heat sink are not required, and hence the methodology becomes applicable to all heat sinks of the finned type and is generally applicable to any rack type. When the inlet temperature is varied, the value of h_{ITD} must also be allowed to vary to maintain the product of the two constant to give

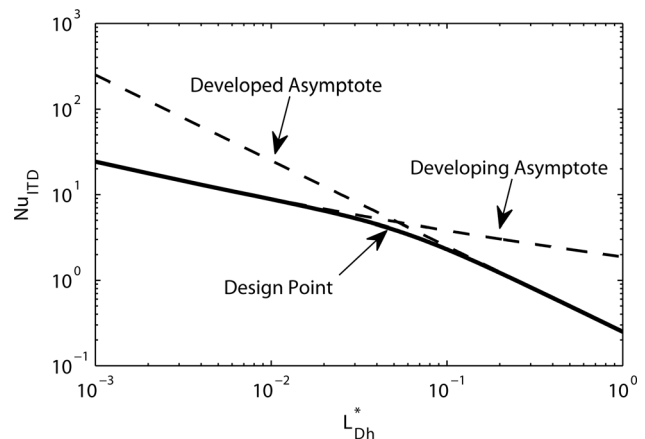


Fig. 2 Intersection of asymptotes method as proposed by Ref. [12] and employed by Ref. [13]

Table 1 Reference conditions in data center

Parameter	Reference value
Mass flow	0.6 kg/s/rack
Computing power	12 kW/rack
Inlet temperature	20 °C
T_{HS}	45 °C
L^*_{Dh}	0.055
Nu_{ITD}	4.85

$$h_{ITD} = \left(\frac{(T_{HS} - T_{In})_{ref}}{(T_{HS} - T_{In})} \right) h_{ref} \quad (5)$$

The properties of the fluid at different temperatures can be obtained from existing data tables. The following scaling can then be applied to determine the required mass flow rate in the system to maintain constant power dissipation with varying inlet temperature to the rack as

$$\frac{L^*}{L^*_{ref}} = \frac{Re_{ref}}{Re} = \frac{\dot{m}_{ref} \mu}{\dot{m} \mu_{ref}} \rightarrow \dot{m} = \frac{L^*_{ref} \mu}{L^* \mu_{ref}} \dot{m}_{ref} \quad (6)$$

Then the new rack exit temperature can be defined as

$$T_{out} = T_{in} + \frac{Q + P_{Fan}(1 - \eta_{Fan})}{\dot{m}c_p} \quad (7)$$

where this equation includes the power lost due to fan inefficiency, as this is known to be non-negligible in practice. Once these parameters are defined the model developed in Ref. [8] may be implemented to assess the variation of inlet conditions across the same rack while maintaining the thermal constraints of the system. This will allow the data center performance from chip to cooling tower to be expressed as a COP_{Grand} rather than just locally at the rack level. The result should allow the identification of the optimum inlet temperature settings to minimize the total cost of cooling or maximize the COP_{Grand} . Also the effect of fan control algorithms at the rack level can be assessed in terms of COP_{Grand} .

It is appropriate to highlight that there are a number of caveats/assumptions upon which this modeling and the results are based. These include:

- Constant and evenly distributed computing load.
- No recirculation and well provisioned cooling.
- No practical minimum or maximum constraints on the mass flow rates.
- No practical limits on temperatures throughout the data center.
- Components of the cooling infrastructure will provide only the required cooling effect at any operating condition.
- Assumption that forced convection laws can always be applied.
- Chiller cooled data center.
- Parameters of all individual components will influence end result and hence each data center may be significantly different.

Although these caveats/assumptions appear limiting in the practical usefulness of the model, it is relatively easy to refine the model to include limits and extend to specific data centers once knowledge of individual components can be obtained. Moreover the aim of this paper is to provide an understanding of the entire data center with minimal constraints, and hence these caveats/assumptions are appropriate.

3 Implementation of Model

Three cases will be considered over a rack inlet temperature range of 5–35 °C.

- (1) Heat sink temperature varying linearly with rack inlet temperature.
- (2) Fixed heat sink temperature with variation of rack inlet temperature.
- (3) Sample fan control algorithms with variation of rack inlet temperature.

For case 1 and 2, the cooling load is broken down into the contributions from room (chilled water and rack/CRAC blowers), chiller, and cooling tower (pumps and fans associated with cooling tower). The temperature range at rack inlet, 5–35 °C, is certainly unrealistic in many instances, where the lower value may result in a risk of condensation and the upper value is too high for many servers. However it does provide some valuable knowledge in the trends that may be expected over such a temperature range, and influence of varying different parameters on COP_{Grand} .

3.1 Case 1. Figure 3 shows the result of increasing the inlet room temperature and heat sink temperature linearly. The total cooling power consumption of the data center increases by about 50% as the inlet temperature is decreased from 35 to 5 °C. The main contribution to this increase, with reduced rack inlet temperature, originates from the contribution of the chiller and is a result of the fluid temperature returning to the chiller at a lower temperature, which requires the chiller to perform more work to remove the same amount of heat. The power at the room level displays the opposite behavior where a modest decrease in power consumption is observed. This decrease is a result of the varying properties of air with increased temperature, namely, density, viscosity, and thermal conductivity which are incorporated in the model. Overall, when the heat sink temperature is allowed to increase linearly with inlet rack temperature improved data center cooling efficiency may be expected.

3.2 Case 2. The power consumption of room, chiller, cooling tower, and total are presented in Fig. 4 for the case where the heat sink temperature is held constant at 45 °C, and the mass flow rate is varied to maintain constant power dissipation at the chip level for the varying inlet rack temperature. The cooling power consumption in this case is varied across the various elements of the thermal chain; below the reference temperature of 20 °C the chiller power increases, while the room power decreases significantly. This balance suggests that the optimum operating point is

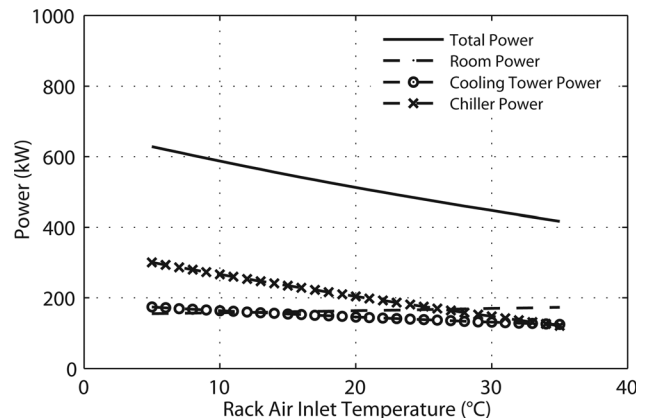


Fig. 3 Total cooling power required for a range of rack inlet temperatures and the contribution of the room, chiller, and cooling tower for case 1

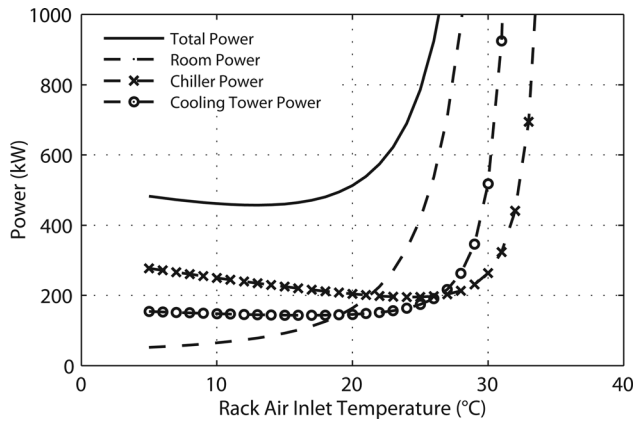


Fig. 4 Total cooling power required for a range of rack inlet temperatures and the contribution of the room, chiller, and cooling tower for case 2

in the region of 15 °C rack inlet temperature. Above the reference temperature, a sharp increase in power consumption at the room level becomes the dominant contribution to cooling work. This is a result of the nonlinear relationship between the heat transfer coefficient and the mass flow rate, i.e., laminar flow scaling on flat plates suggests that the heat transfer coefficient is proportional to the square root of flow velocity. Therefore, to double the heat transfer coefficient at the heat sink would require a four fold increase in mass flow rate, which would result in a 4^3 (64) fold increase in fan power consumption at the room level using fan scaling laws. Clearly such levels are unrealistic and are presented only to demonstrate the trends that can be expected. The chiller power consumption continues to reduce for temperatures above the reference point, until at about 27 °C. The increasing trend for temperatures higher than 27 °C is a result of the additional cooling load associated with cooling infrastructure rather than the computing, such as fan inefficiencies resulting in waste heat. Therefore maintaining a low heat sink temperature over a range of inlet flow conditions will result in severe costs in terms of cooling efficiency as the inlet rack temperature is increased.

Figure 5 shows the COP_{Grand} value for the data center for the limiting cases of 1 and 2. For case 1 it is evident that the reduced energy consumption of the chiller, due to the increased rack inlet temperature, is the dominant factor in the thermal chain, and large gains are evidently possible through a strategy of increasing inlet temperature to server rack while allowing the heat sink temperatures to increase linearly. However for case 2, where the chip temperature is maintained at a constant value, the performance of the

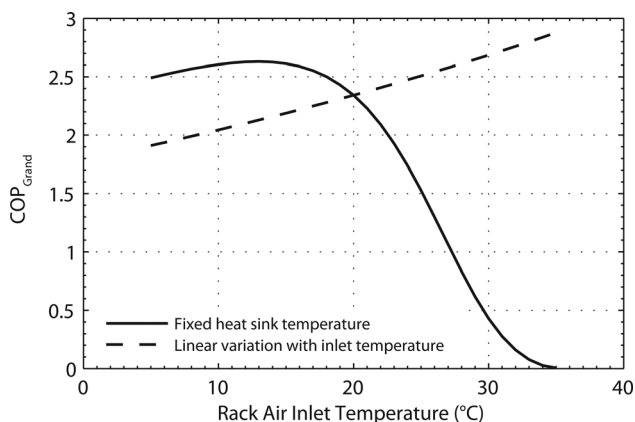


Fig. 5 COP_{Grand} for variation of rack inlet temperature for cases 1 and 2

data center at inlet temperatures above the reference temperature declines rapidly due to the need for increased mass flow to maintain a constant heat sink temperature. In the latter case the methodology of increasing inlet rack temperature is a flawed one.

3.3 Case 3. For case 3 the heat sink temperature is allowed to rise in proportion to the rack inlet temperature using the relation, $T_{HS} = T_{HS(ref)} + (T_{In} - T_{In(ref)})x$, where an x value of 0 and 1 represent the case of constant heat sink temperature (case 2) and linear increase with inlet temperature (case 1), respectively. This relation has practical relevance as a framework for the design of fan control algorithms and describes the full range of heat sink thermal control options. In practical applications a fan control algorithm combines several ranges of x values into a single control algorithm based on threshold operating temperatures. As a result the fan control may allow the heat sink temperature to increase linearly with inlet temperature at low operating temperatures ($x=1$) and increase the value of x as the operating temperatures approach the thermal limits of the system until the heat sink temperature will remain constant ($x=0$). Figure 6 shows the resultant COP_{Grand} for a range of x values. The cases of 1 and 2 bound the results, and for temperatures above the reference temperature combined with scaling factors of $x < 0.6$ the COP_{Grand} measure of data center efficiency is reduced. Hence this implies that the strategy of increasing inlet rack temperature to improve data center cooling efficiency requires the heat sink temperature to increase by at least 0.6 °C for every 1 °C increase in inlet rack temperature. This conclusion is supported by the fan control algorithms that are currently employed where the fan speed is controlled by the heat sink/processor temperature. Since the heat sink can remain within operating conditions at these higher temperatures, a logical question is could the heat sink be maintained at a fixed higher temperature irrespective of inlet conditions and how would this influence the COP_{Grand} .

Figure 7 shows the variation in COP_{Grand} when the inlet temperature to heat sink temperature is fixed at different levels over the inlet temperature range. Hence the same as case 1, but with a number of different heat sink to inlet temperature differences. The lower values of T_{In} to T_{HS} could be considered over cooled states and give an estimation of the actual cost of over-cooling a data center, where a temperature difference of 20 °C results in poor COP_{Grand} values. For any given inlet rack temperature the level of the COP_{Grand} improves with increasing the temperature of the heat sink. Figure 8 represents the COP_{Grand} curves for a heat sink maintained at a fixed temperature over the range of inlet rack temperatures considered. Using this philosophy the optimum rack inlet temperature for a given heat sink temperature can be determined to obtain best facility performance. This also illustrates the benefit of tight temperature controls to maintain the chip at a fixed temperature irrespective of inlet rack temperature. The results are

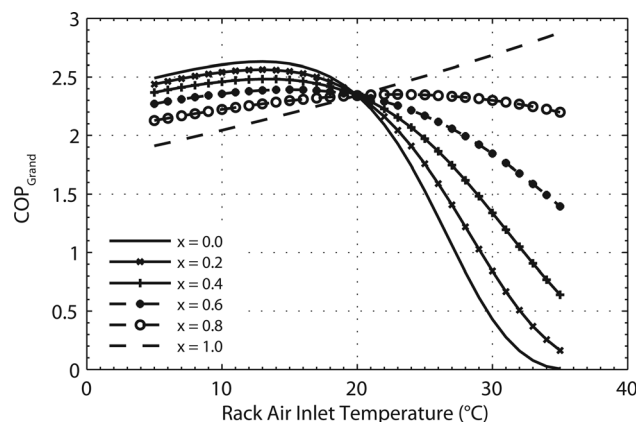


Fig. 6 COP_{Grand} for different chip temperature control algorithms

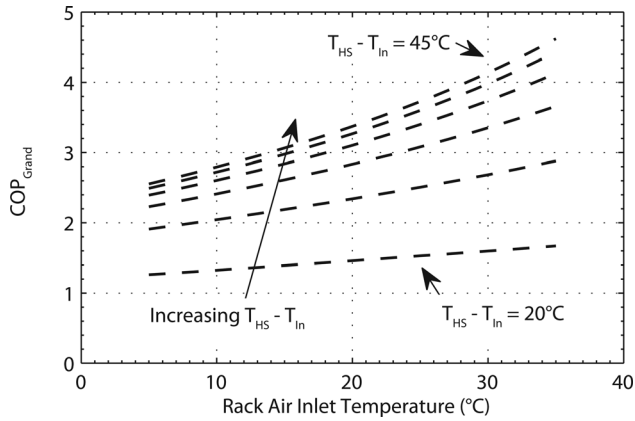


Fig. 7 COP_{Grand} for different fixed chip to heat sink temperature differences. The dashed lines represent fixed heat sink to inlet temperature differences in steps of 5 °C between 20 °C and 45 °C from lower to higher COP_{Grand} , respectively

striking, in that the higher heat sink temperatures result in higher inlet temperatures providing a higher COP_{Grand} . These gains at higher heat sink temperatures are a result of lower fan and CRAC power at the room level and higher temperature fluid returning to the chiller, thereby improving the chiller coefficient of performance. An interesting point that is evident from Fig. 7 is that the same COP_{Grand} can be achieved with many different conditions, for example, a COP_{Grand} of 2.5 is achieved with $T_{HS} = 55$ °C and $T_{In} = 31$ °C and also with the conditions $T_{HS} = 45$ °C and $T_{In} = 18$ °C. Clearly the latter is a better operating point in terms of reliability, and this demonstrates the necessity to understand how the entire data center performance reacts to changing conditions at any point in the thermal chain of components within the data center. The philosophy of, simply, increasing the inlet temperature is not a robust methodology for improvements in cooling efficiency.

Within the heat sink temperature range of 45–65 °C, the maximum COP_{Grand} for each heat sink temperature can be expressed as $COP_{Grand} = 0.057T_{HS}$. This simplified relationship, although not a general result for all data centers incorporates all the nonlinear elements of the data center and demonstrates the strong relationship between heat sink temperature and data center COP_{Grand} . Taking a baseline COP_{Grand} value of 2.5, each 5 °C increase in heat sink temperature results in 15% saving in cooling costs for the data center. This may be a particularly relevant finding for noncritical data centers, where accepting a limited number of fail-

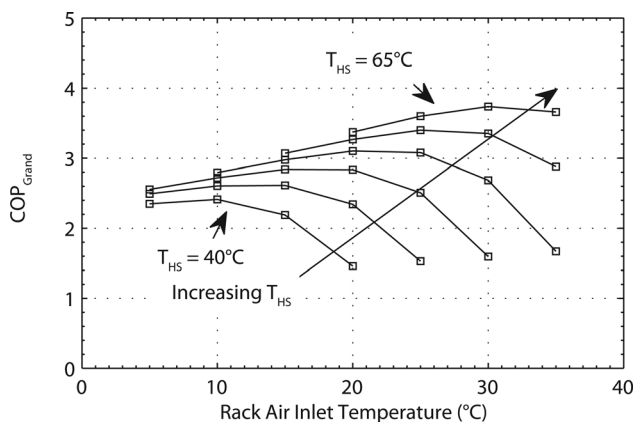


Fig. 8 COP_{Grand} for constant heat sink temperature lines for T_{HS} between 40 °C and 65 °C from lower to higher COP_{Grand} , respectively, in steps of 5 °C

ure due to a higher operating temperature could be more beneficial in terms of sustainability and cost.

The analysis thus far is confined to a fixed heat sink geometry within a rack. For such a case the temperature range proposed in Fig. 8, 40–65 °C, would be extreme and possibly result in processor temperatures operating outside their safe thermal constraints. An alternative option is to replace the heat sinks with higher performance heat sinks to maintain a constant heat sink temperature and thereby package temperature. Hence, an important parameter to understand is the effect of heat sink choice on COP_{Grand} ; such an analysis would allow a cost analysis of heat sink solutions to be undertaken. For example taking the $T_{HS} = 65$ °C curve on Fig. 8 at its maximum COP_{Grand} with a rack inlet temperature of 30 °C and processor power dissipation of 100 W, the resultant thermal resistance for the heat sink under these conditions is 0.3 °C/W. If this heat sink solution is replaced with a higher performance heat sink at the same mass flow rate and thermal resistance of 0.15 °C/W, this would result in a heat sink temperature of 45 °C and hence the same processor temperature as the reference condition. Since all other parameters of the data center remain constant, then the COP curve for this new heat sink would closely follow that of the $T_{HS} = 65$ °C curve on Fig. 8, but now at the lower $T_{HS} = 45$ °C. The maximum COP_{Grand} values for the two heat sink designs at $T_{HS} = 45$ °C are 3.74 and 2.61 for the cases of lower and higher thermal resistances, respectively. This equates to more than 40% reduction in the cooling power as a result of reducing the thermal resistance of the heat sink by 50%. Of course, the additional cost of the heat sinks would need to be considered. Assuming an electricity cost of \$0.1/kWh and processor power consumption of half the non cooling power load, the resultant break even point would be less than ten days for each additional dollar spent on each heat sink within the data center.

Similar curves to those of Fig. 8 would result from varying heat sink designs with a fixed processor temperature. For this case the curves of increased heat sink temperature are replaced with reducing heat sink thermal resistance. The COP_{Grand} values for the two heat sink designs at $T_{HS} = 45$ °C are 3.74 and 2.61 for the cases of lower and higher thermal resistances respectively. Applying the same analysis to the maximum COP_{Grand} values of each curve in Fig. 8, to operate at $T_{HS} = 45$, results in a rough estimate of gains that can be achieved from higher performance heat sinks. Every 1% reduction in heat sink thermal resistance, for a specified mass flow rate, translates to a reduction of 1% in the cooling power required. Therefore high performance heat sinks that are more costly may have a relatively quick payback period for the data center operator.

4 Conclusions

In this paper, an approach to considering the cooling chain from chip to cooling tower in a data center has been applied to examine the impact of increased operating temperatures on energy efficiency in data centers. Increasing the rack inlet temperature by itself does not necessarily guarantee optimal or even nominal improvements in data center energy efficiency. Instead, a co-designed architecture that considers both intrasystem considerations (more specifically, heat sink temperature) along with the data center operating environment is found to lead to the highest COP_{Grand} . For a reference baseline case study, each 5 °C increase in heat sink temperature results in 15% saving in cooling costs for the data center, while reducing the thermal resistance in the heat sink by about 50% is found to yield an improvement in data center cooling efficiency of nearly 40%.

This work has several implications for future data center design and management. First, there has been a recent movement towards the use of outside air for cooling of data centers. While such elimination of the chiller infrastructure is certainly desirable, the present study suggests that significant savings can be achieved within existing infrastructures through integrated system and facility design. Second, there has been a push in the industry to increase allowable limits for rack inlet air temperatures. While this can

indeed be a step in the right direction for many facilities, this paper suggests that in other cases the benefits of increasing rack inlet temperature may be small or nonexistent due to increased fan power at the system level. Thus, instead of simply focusing on facility design that allows for operation at elevated rack inlet temperatures, a more viable option may be system redesign in order to allow operation at elevated heat sink temperatures. Finally, this paper presents a starting point for the design of facility-aware fan control algorithms within computer systems. As the data center itself becomes the computer, the traditional approach of designing and managing system architectures based on a specified inlet temperature may need to be revisited in favor of a more holistic approach. Particularly with the ability for increased sensing in the data center environment and infrastructure, an opportunity exists to derive further efficiencies in the cooling infrastructure through improved system-level thermal management. Future work will consider this thread in more detail.

Acknowledgment

Funding provided by the Irish Research Council for Science Engineering and Technology under the Enterprise Partnership Scheme in collaboration with Hewlett-Packard Laboratories.

Nomenclature

D_h = hydraulic diameter, m
 COP_{Grand} = overall coefficient-of-performance ($P_{IT}/P_{Cooling}$)
 c_p = specific heat capacity of air, kJ/kgK
 L^* = inverse Graetz number ($X/DRePr$)
 Nu = Nusselt number
 P = power, kW
 Pr = Prandtl number
 Q = computing load, kW
 Re = Reynolds number
 T = temperature, °C
 h = heat transfer coefficient, W/m²K
 \dot{m} = mass flow rate, kg/s

Greek

μ = viscosity, kg/m.s
 η = efficiency, %

Subscripts

ITD = inlet temperature difference
 In = server inlet
 HS = heat sink
 Out = server outlet
 Ref = reference condition

References

- [1] Watson, B. J., Shah, A. J., Marwah, M., Bash, C. E., Sharma, R. K., Hoover, C. E., Christian, T. W., and Patel, C. D., 2009, "Integrated Design and Management of a Sustainable Data Center," ASME InterPACK, San Francisco, July 19–23 2009.
- [2] Koomey, J. G., 2007, "Estimating Total Power Consumption by Servers in the US and the world," Lawrence Berkeley National Laboratory, Stanford University.
- [3] Bash, C. E., Patel, C. D., Shah, A. J., and Sharma, R. K., 2008, "The Sustainable Information Technology Ecosystem," 11th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems.
- [4] Shah, A. J., Carey, V. P., Bash, C. E., and Patel, C. D., 2008, "Exergy Analysis of Data Center Thermal Management Systems," *ASME J. Heat Transfer*, **130**, p. 021401.
- [5] Shrivastava, S. K., Iyengar, M., Sannakia, B. G., Schmidt, R., and VanGilder, J. W., 2009, "Experimental-Numerical Comparison for a High-Density Data Center: Hot Spot Heat Fluxes in Excess of 500 w/ft (2)," *IEEE Trans. Compon. Packag. Technol.*, **32**, pp. 166–172.
- [6] Rambo, J., and Joshi, Y., 2007, "Modeling of Data Center Airflow and Heat Transfer: State of the Art and Future Trends," *Distrib. Parallel Databases*, **21**, pp. 193–225.
- [7] Bhopte, S., Agonafer, D., Schmidt, R., and Sannakia, B., 2006, "Optimization of Data Center Room Layout to Minimize Rack Inlet Air Temperature," *ASME J. Electron. Packag.*, **128**, pp. 380–387.
- [8] Breen, T. J., Walsh, E. J., Punch, J., Shah, A. J., and Bash, C. E., 2011, "From Chip to Cooling Tower Data Center Modeling: Influence of Server Inlet Temperature and Temperature Rise Across Cabinet," *ASME J. Electron. Packag.*, **133**, p. 011004.
- [9] Patel, C. D., Sharma, R. K., Bash, C. E., and Beitelmal, M., 2006, "Energy Flow in the Information Technology Stack: Coefficient of Performance of the Ensemble and its Impact on the Total Cost of Ownership," HP Labs Technical Report No. HPL-2006-55.
- [10] Jeffers, J. P., Walsh, E. J., and McLean, M., 2009, "Heat Transfer From Novel Target Surface Structures to a Normally-Impinging and Submerged and Confined Water Jet," *ASME J. Thermal Sci. Eng. Appl.*, **1**, pp. 1–9.
- [11] Sparrow, E. M., 1955, "Analysis of Laminar Convection-Heat Transfer in the Entrance Region of Flat Rectangular Ducts," NACA Technical Note 3331.
- [12] Teertstra, P., Yovanovich, M. M., and Culham, J. R., 2000, "Analytical Forced Convection Modeling of Plate Fin Heat Sinks," *J. Electron. Manuf.*, **10**, pp. 253–261.
- [13] Stafford, J., Walsh, E. J., Egan, V., Walsh, P., and Muzychka, Y. S., 2010, "A Novel Approach to Low Profile Heat Sink Design," *ASME J. Heat Transfer*, **132**, p. 091401.