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Low Power CMOS Analog Multiplier

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Abstract
In this paper Low power low voltage CMOS analog multiplier circuit is proposed. It is based on flipped voltage follower. It consists of four voltage adders and a multiplier core. The circuit is analyzed and designed in 0.18um CMOS process model and simulation results have shown that, under single 0.9V supply voltage, and it consumes only 31.8μW quiescent power and 110MHZ bandwidth.
Keywords: analog multiplier; flipped voltage follower ; multiplier core; Gilbert cell.

I. INTRODUCTION

A multiplier is an important building block for many analog applications. Real time multiplication of two analog signals is one of the important operations in analog signal processing. The main building block of analog signal processing circuits is a multiplier such as frequency translators, modulators, automatic gain controllers etc. The Gilbert cell is a most oldest and popular structure in IC technologies due to wide dynamic range and high frequencies performance in CMOS technology, the approaches which are important for most applications in CMOS multipliers using MOS transistors in saturation region and non-saturation region. In order to decrease battery size and weight and extend the battery life requires new low-voltage, low-power analog multipliers. A CMOS analog multiplier classified as type IV(using V_{gs}^2 with voltage adders) which has a single low supply voltage and is compatible with low power operation. This can be very important multiplier for low power operation. CMOS analog multiplier consists of a multiplier core and four voltage adders. The transistors of the circuit operate in the saturation region. The circuit uses flipped voltage follower to get a low power consumption.

II. CIRCUIT DESCRIPTION

The proposed circuit consists of four flipped voltage followers and two multiplier basic. The operation of all the transistors in the circuit are in saturation region. The main blocks of the multiplier are discussed here.

A. Multiplier Core

Here the multiplier core is based on V_{gs}^2 technique [1]. As shown in the figure1, there are four transistors in the multiplier core which operates in saturation region. And their drain currents are expressed as:

$$I_{d1} = K_1 [(V_{DD}-V_4 - aV_1-b) -V_{TP}]^2 \qquad (1)$$
$$I_{d2} = K_2 [(V_{DD}-V_3 - aV_1-b) -V_{TP}]^2 \qquad (2)$$
$$I_{d3} = K_3 [(V_{DD}-V_3 - aV_2-b) -V_{TP}]^2 \qquad (3)$$

$$I_{d4} = K_4 [(V_{DD}-V_4 - aV_2-b) -V_{TP}]^2 \qquad (4)$$

Thus, the output current obtained from the equations above:

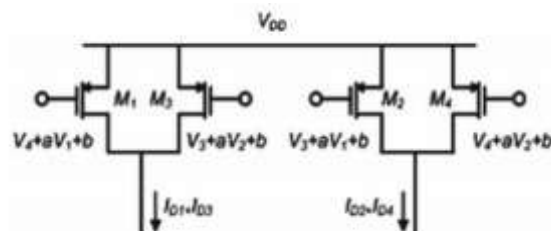$$I_{out} = (I_{d1} + I_{d3})- (I_{d2} + I_{d4}) = 2aK_1(V_1 -V_2)(V_3 -V_4) \qquad (5)$$

Fig.1: Multiplier core

The input signals (V_4+aV_1+b), (V_3+aV_1+b) (V_3+aV_2+b) and (V_4+aV_2+b) of the multiplier core will be generated by using voltage adder circuits[1].

B. Voltage Adder Circuit

The simple analog voltage adder limits the input voltage range, they are not suitable with the one volt supply. Flipped voltage follower is the powerful way to implement a low power low voltage analog multiplier circuit as they are suitable for low input range supply also. The FVF[1] is shown in figure2.

If all the transistors are working in saturation region in this figure, then the voltage applied at Node C (V_C) will follow the voltage applied at Node D with a DC level shift V_{gs}.

It is determined by the current I & the parameters of transistor; the V_C can be written as:

$$V_C = V_D - V_{gs} = V_D - \sqrt{(I/K_6)} - V_{th} \qquad (6)$$

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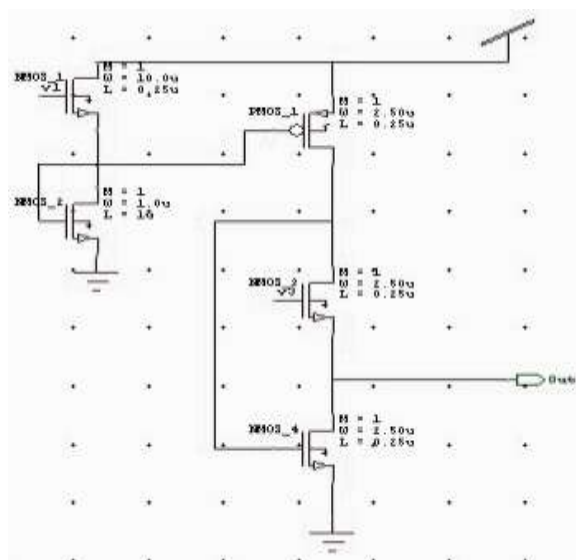*ISSN: 2248-9622, Vol. 5, Issue 12, (Part - 2) December 2015, pp.01-04*

Fig.2: FVF cell

The current equation of figure2 is expressed as:

$$I = K(V_{dd} - V_N - V_{th})^2 \qquad (7)$$

By the equations (6) & (7), V_C can be obtained as

$$V_C = V_D + \surd(K_5/K_6)V - [\surd(K_5/K_6)(V_{dd}-V_{tp}+V_{tn}]$$
$$= V_D + \surd(K_5/K_6)V_B - V_b \qquad (8)$$

For increasing the range of the inputs in figure2, the two NMOS transistors nmos_1 & nmos_2 are used that are added.

As the transistors are working in saturation region, $K_8 = K_9 = 0.5uC_{ox}W/L$.

$$\text{So, } I_8 = I_9 \qquad (9)$$

Equating the above equation, we get

$$K(V_A - V_B - V_{tn})^2 = K(V_B - V_{tn}) \qquad (10)$$
$$\text{Thus, } V_B = V_A/2 \qquad (11)$$

Therefore put V_B into equation (8)

$$V_C = V_D + \surd(K_5/K_6)V_A - V_B \qquad (12)$$

V_1 & V_4 input signals are applied at A & D nodes.

$$V_C = V_4 + aV_1 + b \qquad (13)$$

Where, $a = \surd(K_5/4K_6)$, $b = -V_b$

The equations above indicates that the addition of V_C & V_B with coefficient $\surd(K_5/K_6)$ can be achieved in the first two terms of equation.

However, V_C also includes a level shift V_b that represents $\surd(K_5/K_6)(V_{dd} - V_{tp}) + V_{tn}$.

C. Completed Multiplier

The block diagram representation of the complete multiplier circuit is shown in figure 3. The first four blocks represent the flipped voltage follower cell as in the final multiplier circuit the four FVF cells are used. And the two multiplier core are used which are labeled as V to I converter.
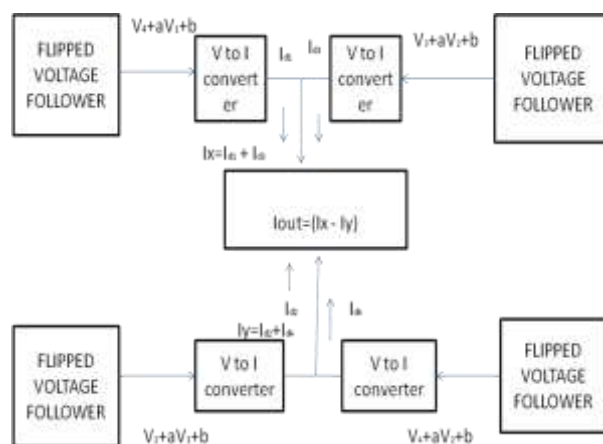

Fig.3: Block representation of the complete multiplier circuit.

The output voltage of the multiplier can be expressed as:

$$V_O = R_L[(I_{d1}+I_{d3})-(I_{d2}+I_{d4})] = R_L I_{out} \qquad (14)$$

On putting I_{out} in equation (14) above can be written as:

$$V_O = 2aKR_L V_X V_Y \qquad (15)$$

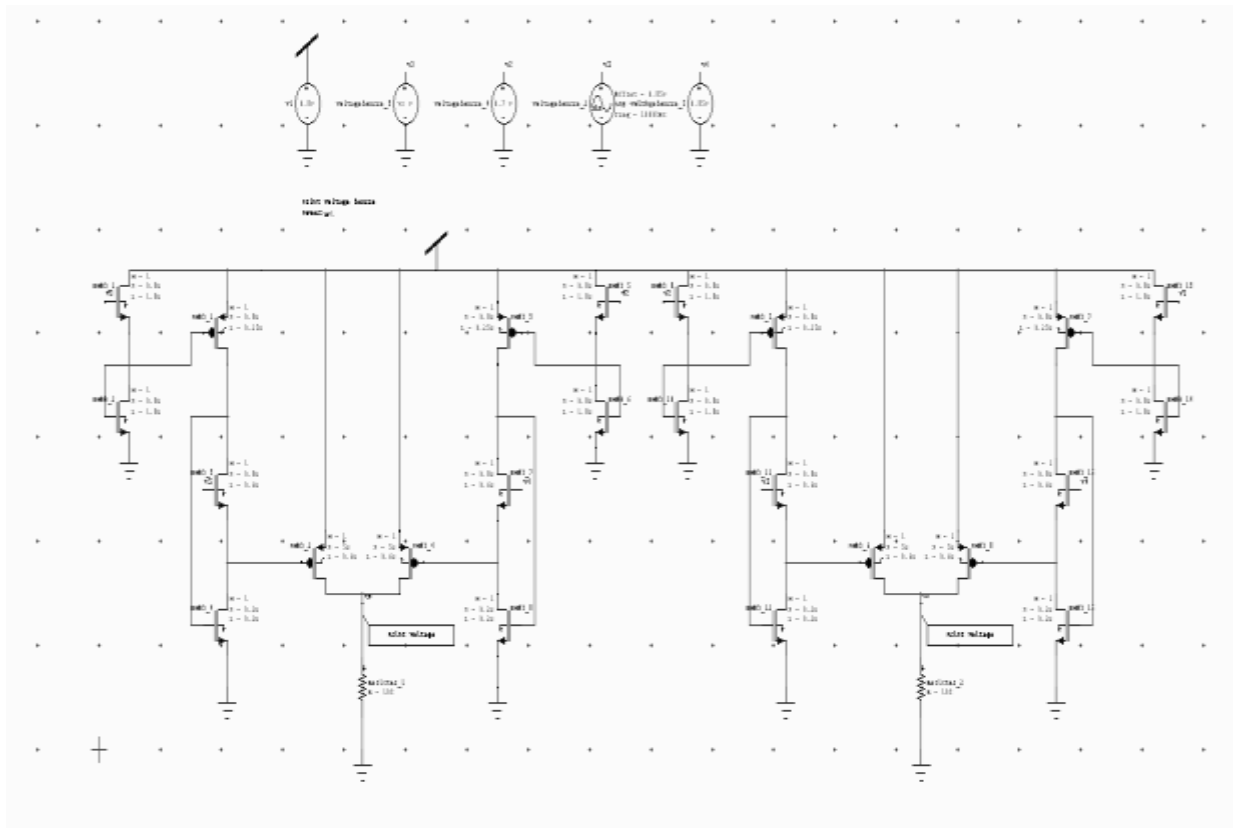Where V_X & V_Y are (V_1-V_2) & (V_3-V_4) respectively.

Fig.4: The Complete Multiplier Circuit

III.   SIMULATION RESULTS

The proposed multiplier is simulated using 0.18um- TSMC. The power supply is 0.9V & R_L are 10KΩ.

The DC transfer characteristics curve of the multiplier are shown in figure5 and V_O output voltage V_X, between ±400mV, respectively.
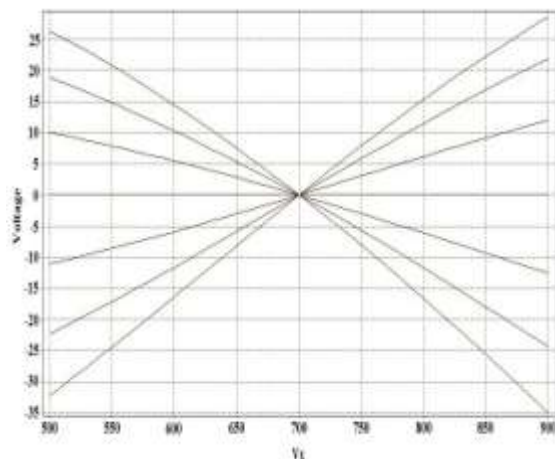

Fig.5: DC transfer characteristics curve versus V_X

The linearity error of the proposed multiplier can be calculated by fixed input V_X while V_Y varied and vice versa. The result of the linearity error of the circuit is 0.7%.

The figure 6 shows the frequency responses of the output voltages versus V_X of the complete multiplier circuit respectively.
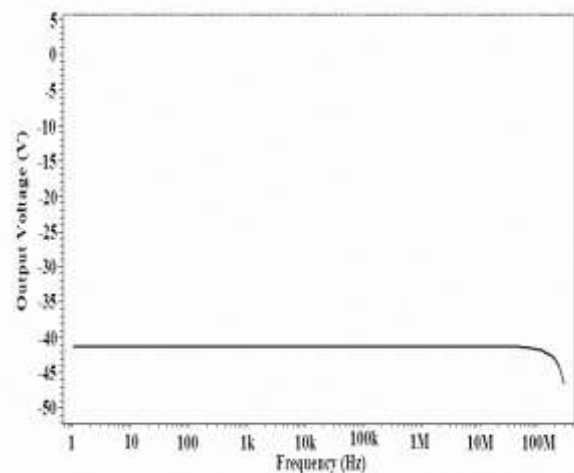

Fig.6: Frequency response V_O vs V_X

Figure 7 shows the application of the proposed multiplier as one of the modulation technique known as amplitude modulation technique. The input signals V_X & V_Y are 1MHZ & 10MHZ with $400mV_{p-p}$ amplitude performed the modulation. The result shows that the output voltage is a sinusoidal waveform of double the input frequency.
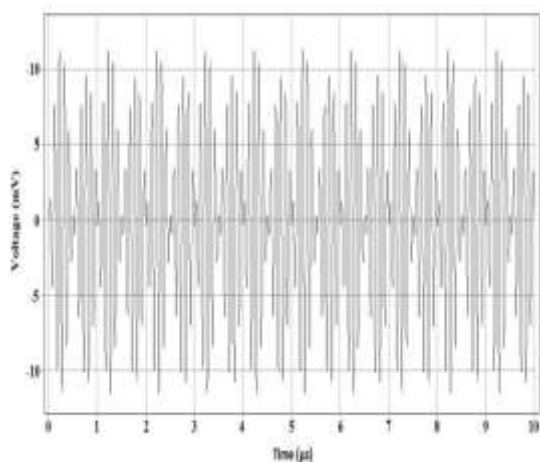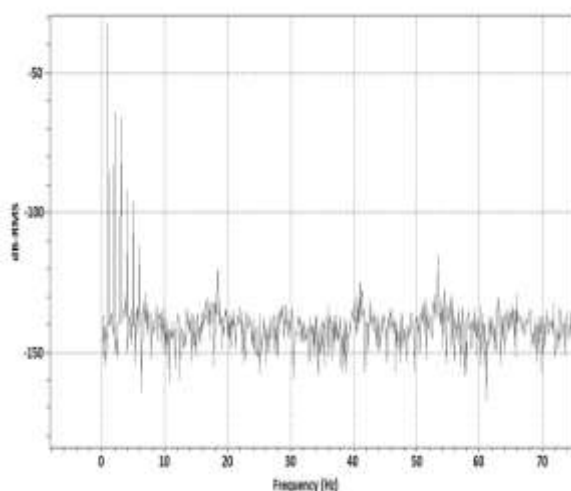
Fig.7: Modulation technique as an application

Fig.8. Total harmonic distortion waveform

In figure 8 the total harmonic distortion (THD) of the complete circuit is about 1.8% when V_X is $400mV_{p-p}$ sinusoidal input signal with frequency of 1MHZ & V_Y is a 200mV and vice versa. The power consumption of the circuit is 31.8μW.

IV. CONCLUSIONS

The completed multiplier works with a single supply of 0.9V. The various parameters which are analysed are power, linearity, total harmonic distortion. It has low power consumption (31.8μW), linearity error of 0.7% for linear range $400MV_{P-P.}$ THD is 1.8%.

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