Digital Variable Frequency Control for Zero Voltage Switching and Interleaving of Synchronous Buck Converters

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***Abstract*—When a synchronous buck converter is operated with zero voltage switching (ZVS) and fixed frequency, the direction of the current in the output inductor is alternated each switching period. Thus the output current ripple of the converter is high to ensure zero voltage switching operation at maximum load. With interleaved outputs this leads to high circulating currents at low loads. In this paper, to minimize circulating currents at low loads, solutions for digital control of ZVS with variable switching frequency and interleaving control for bidirectional power flow are presented. The methods have been implemented in a DSP and verified by measurements.**

I. INTRODUCTION

When the synchronous buck converter is operated with zero voltage switching (ZVS), the direction of the current in the output inductor is alternated each switching period. The energy stored in the output inductor is used to charge the drain- source capacitance of the transistors, and the voltage is naturally commutated from one transistor to the other. This converter in ZVS operation is also called quasi square wave (QSW) converter due to the resonant transition of the drain- source voltage, V_{ds}.

The advantages of the ZVS operation are reduced turn-on losses, minimized switch voltage stress, natural commutation of the body diode, and minimizing the output inductor with regard to stored energy. The disadvantages are high input and output current ripple, which leads to increased turn-off losses, increased conduction losses, increased inductor losses, and large filtering capacitors [2].

By interleaving multiple converters the input and output current ripple can be significantly reduced. The interleaved quasi square wave converter is documented to have high power density, and fast transient response [1].

It is most common to implement the converter control with a fixed switching frequency, as in [3] and [6]. With fixed frequency, the output current ripple of each of the paralleled converter outputs is fixed. The peak to peak output current ripple of each converter must be more than twice the maximum average output current in order to maintain zero voltage switching for the whole operating region. This leads to high circulating currents at low loads. Therefore, even if the efficiency of the ZVS operation is comparable to the hard switching operation at high loads, the efficiency of ZVS operation is much less at low loads due to the circulating currents between the parallel outputs. The similar circuit topology in ZVS operation for DC-AC conversion is also known as the resonant pole inverter (RPI) [4].

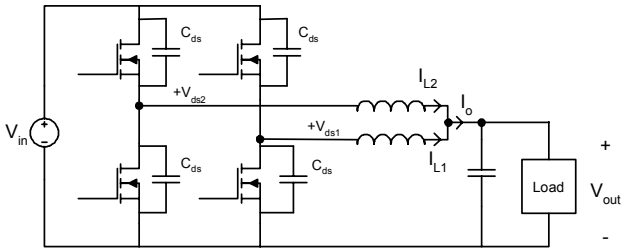

Fig. 1. Interleaved ZVS synchronous buck converters

For the resonant pole inverter, analog control methods with variable switching frequency have been presented. These control methods minimizes the current ripple but do not actively control interleaving of the paralleled outputs. Paralleled outputs cancel out the current ripple only stochastically, as discussed in [5].

In this paper, solutions for digital control with variable switching frequency and with interleaving control of synchronous buck converters are suggested. The converter topology and the definitions of voltage and current polarity are shown in Fig. 1. These methods use the inductor current value, which could be indirectly observed or directly measured, in order to generate interrupts that controls the switching frequency. Both parallel outputs are synchronized to this frequency.

The first method presented, calculates the upper transistor on-time (for positive reference current) directly based on measured input and output voltage, the inductance, and the reference current value. The second method uses the synchronized sampling of the peak current to calculate a change in the upper transistor on-time (pos. ref. current). The third method is similar to the second method except that it uses the inductance, the measurement of the upper transistor off-time, and the output voltage to estimate the peak current.

These methods are presented for DC-DC converters but could be applied to inverter control, and allow bidirectional power flow. These methods could be used for any number of paralleled outputs, but to simplify discussions, two interleaved outputs are discussed in this text.

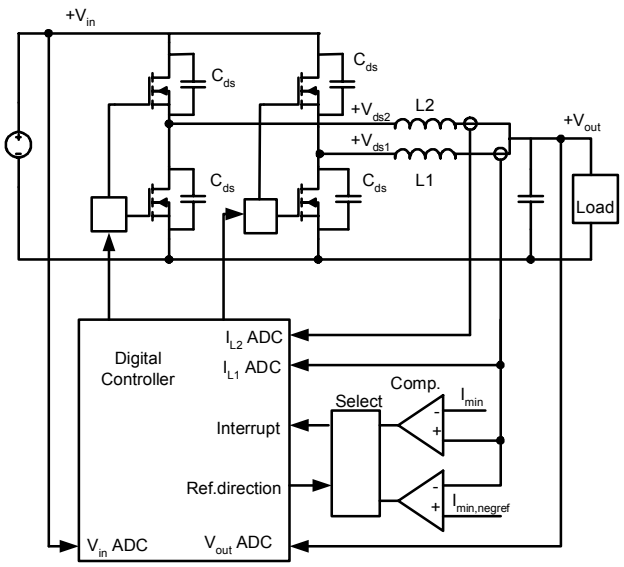

Fig. 2. Control system set-up.

II. The ZVS Control Strategies and Principle of Operation

Fig. 2 shows the set-up of the interleaved converters interfaced to the digital control system. The input voltage, the output voltage, and the inductor currents are sampled.

One of the converter outputs is used as a master. For the master output, two comparators are used on the measured inductor current to generate interrupts that controls the switching frequency. Which comparator used to control the switching frequency depends on the direction of the reference current, $i_{avg,ref}$.

When $i_{avg,ref}$ is positive, the comparator with the I_{min} input is used to control the frequency. When $i_{avg,ref}$ is negative, the comparator with the $I_{min,negref}$ input is used to control the frequency. The value of I_{min} and $I_{min,negref}$ is based on the minimum current required in the inductor in order to ensure zero voltage switching.

When $i_{avg,ref}$ is positive, the inductor current is digitally controlled by controlling the upper transistor on-time. When $i_{avg,ref}$ is negative, the inductor current is digitally controlled by controlling the lower transistor on-time. To simplify further discussions, the more detailed description of the control is described for positive reference current only.Fig. 3 shows the waveforms of the master output in ZVS operation.

When upper transistor is off the inductor current, i_{L1}, falls linearly based on the output voltage, v_o, and the inductance, L_1. The current passes trough zero and reach the minimum current required, I_{min}, to ensure zero voltage switching. When I_{min} is reached, the comparator generates an interrupt to the digital control, which controls the turn-off of the lower transistor. The inductor current then flows through the drain-source capacitance, C_{ds}, and commutates the drain-source voltage, v_{ds}, in a resonant transition. After the transition the upper transistor is turned on and the inductor current, i_{L1}, rises according to the, input voltage, v_{in}, the output voltage, v_{out}, and the inductance L_1.

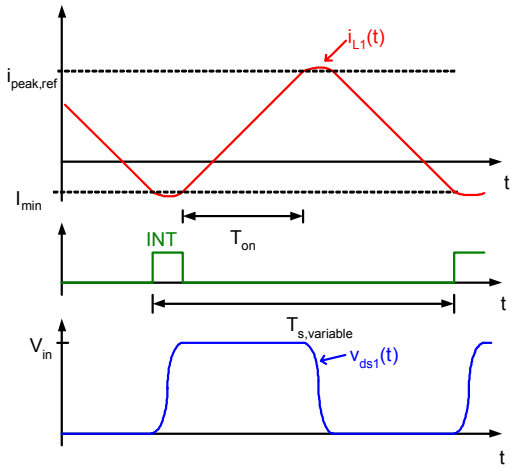

Fig. 3. Current and voltage waveforms

A. Control of inductor current by direct calculation of on-time

The control objective is to control the average inductor current. Since the current at turn- on, I_{min}, is well defined the average current can be calculated.

The peak current, i_{peak}, after a specific upper transistor on-time, t_{on}, can be estimated to be based on the basic differential equation of the inductor current in (1), as shown in (3). The digital control by direct calculation set the on-time directly based on (6). The calculation uses the variable reference input, $i_{avg,ref}$, the variable sampled input and output voltage, v_{in} and v_{out}, the the output inductance, L_1, and the minimum inductor current for ZVS, I_{min}. I_{min} may also be sampled to compensate for delays in the interrupt generating circuit.

The sampling of input and output voltage, v_{in} and v_{out}, and the inductor currents are synchronized with the turn-off of the upper transistor. This way, the peak current will be sampled. With the direct calculation control strategy, the sampled currents are used for error detection only.

$$L_1 \frac{di_{L1}}{dt} = v_{L1} \tag{1}$$

$$\int_{I_{min}}^{i_{peak}} di = \int_{0}^{t_{on}} \frac{v_{in} - v_{out}}{L_1} dt \tag{2}$$

$$i_{peak} = \frac{v_{in} - v_{out}}{L_1} \cdot t_{on} + I_{min} \tag{3}$$

$$i_{avg} = \frac{i_{peak} + I_{min}}{2} \tag{4}$$

$$i_{peak,ref} = 2 \cdot i_{avg,ref} - I_{min} \tag{5}$$

$$t_{on} = \frac{2 \cdot L_1 \cdot (i_{avg,ref} - I_{min})}{(v_{in} - v_{out})} \tag{6}$$

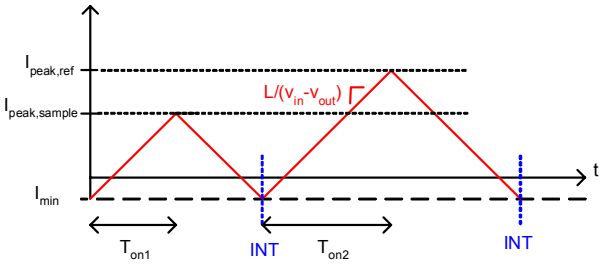

Fig. 4. Control with sampled peak current feedback.

B. *Control with sampled peak current feedback*

With the feedback of sampled currents, t_{on} does not need to be calculated directly. The change in the on-time, Δt_{on}, is calculated. Fig. 4 shows the principle. After sampling the peak current, the difference between reference current, $i_{peak,ref}$ and the measured current, $i_{peak,sample}$, is used to calculate the change in on-time.

The equation to calculate the change is shown in (7). The next on-time, t_{on2}, can then be calculated based on, the previous on-time, t_{on1} and the calculated change as shown in (8). The variable frequency interrupt is what stabilizes the control loop.

With the peak current measurement feedback it is not necessary to use the sampled input and output voltage to calculate t_{on2}. Instead a constant may be used, as shown in (9). The constant will be a fixed gain that can be further reduced to stabilize the control loop. The control response will not be as fast as the control with direct calculation, but a not desirable division is avoided. With direct calculation, the on-time calculated must be used for all parallel outputs. This means that the current sharing will be passively governed. By using the peak current feedback method, the peak current on all parallel outputs may be sampled to set a separate on-time on each output. With the peak current feedback method, active current sharing control between all parallel outputs is possible.

$$\Delta t_{on} = \frac{L_1}{(v_{in} - v_{out})} \cdot (i_{peak,ref} - i_{peak,sample}) \tag{7}$$

$$t_{on2} = t_{on1} + \Delta t_{on} \tag{8}$$

$$\Delta t_{on,prop} = \frac{L_1}{V_{in,\max}} \cdot (i_{peak,ref} - i_{peak,sample}) \tag{9}$$

C. *Control with estimated peak current feedback*

The upper transistor turn-off time, t_{off}, is calculated at each interrupt based on t_{on} and $t_{s,variable}$ as shown in (10). The peak current can then be estimated based on t_{off}, v_{out}, and L_1, as shown in (11). The estimated peak current, $i_{peak,est}$, is then used to calculate the change, $\Delta t_{on,prop}$, instead of the sampled peak current, $i_{peak,sample}$ in (9).

$$t_{off} = t_{s,variable} - t_{on} \tag{10}$$

$$i_{peak,est} = \frac{v_{out} \cdot t_{off}}{L_1} \tag{11}$$

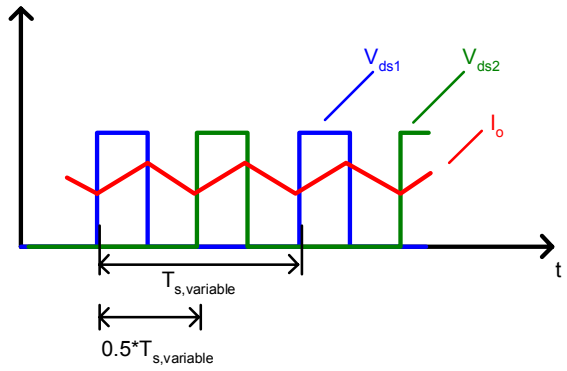

Fig. 5. Variable frequency interleaved waveforms

D. *Generating interleaved switching waveforms*

Fig. 5 illustrates the waveforms of two interleaved parallel outputs.

The interrupt generated by the inductor current in L_1 do not only control the frequency of the first output. Also the 180 degrees shifted timer of the second output can be adjusted digitally by this interrupt.

All the timers of any number of parallel outputs may be synchronized to the same frequency and phase shifted 360/n degrees to generate the interleaved switching waveforms. The slave phases are reloaded with new timer period value at its period interrupt, and the timers are also adjusted for correct phase shift at this time.

III. Test Set Up and Measurements

A control board with a Texas Instruments F2812 DSP is used to test the digital control techniques. Two parallel synchronous buck converters are coupled together. The input voltage, v_{in}, the output voltage, v_{out}, and the current, i_{Lx}, in each of the two inductors are sampled. The method implemented was with peak current feed back. The current sharing was not done by active control, but passively governed by the resistance in the transistors and inductances. This way, current measurement of the slave output was not needed.

Fig. 6, Fig. 7 and Fig. 9 show the steady state inductor current waveforms, for two different load conditions. The sum of the inductor currents is the brown waveform. The measurements show how the frequency changes for the different load conditions with the same reference current. The current is the same for all three load conditions and the output load resistance is varied. It can be seen how the duty ratio varies, i.e. the output voltage. It also shows how the current ripple is reduced out for different duty ratios.

Fig. 9 shows the inductor current and output voltage transient to a current reference step. The gain had to be reduced significantly lower than the theoretical limit in order for the control loop to be stable. The yellow curve, CH1, is the output voltage. The green and purple curve, CH3 and CH4, are the interleaved currents.

Fig. 10, shows the interrupt timing. The blue curve, CH2, shows the interrupt timing. The first leftmost pulse on CH2 is the externally triggered interrupt, here the new time period (i.e. frequency) is set and a period interrupt for the master phase, CH3, is triggered. The second pulse is the master phase period interrupt. In this interrupt the next

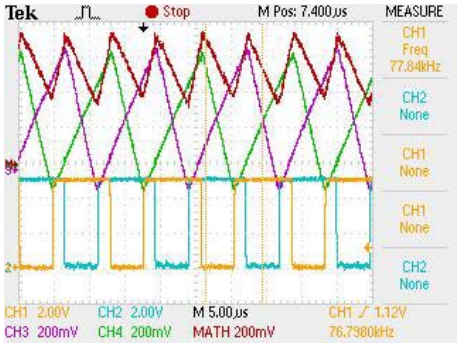

Fig. 6. Steady state waveforms 1st load condition. 78kHz switching frequency

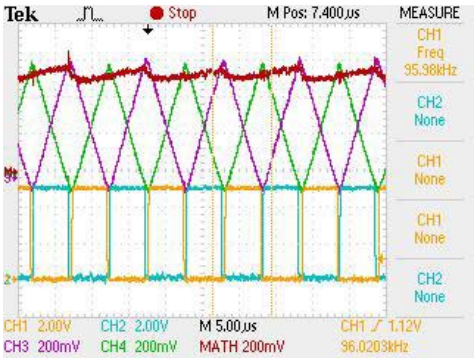

Fig. 7. Steady state waveforms 2nd load condition. 96kHz switching frequency

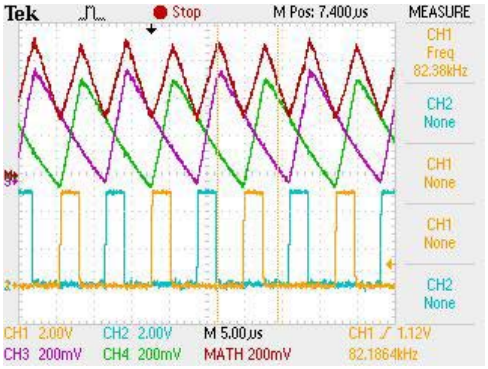

Fig. 8. Steady state waveforms 3rd load condition. 82kHz switching frequency

on-time is calculated. The third pulse is the slave phase, CH4, period interrupt. In this interrupt the next period and on-time for the slave phase is loaded. Also the timer for the slave phase is adjusted for the optimal phase-shift.

IV. Conclusion

This paper has presented and discussed methods to implement a digital control with variable frequency that enables interleaving and zero voltage switching of paralleled synchronous buck converters with bidirectional power flow. The peak current feedback method has been implemented in a DSP and verified by measurements.

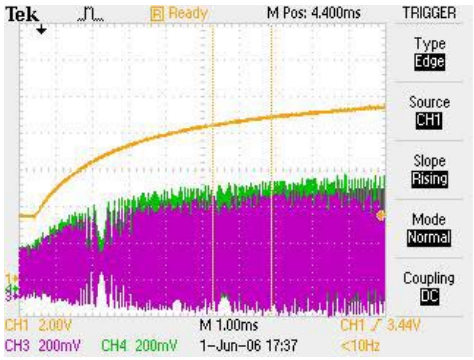

Fig. 9. Reference step transient

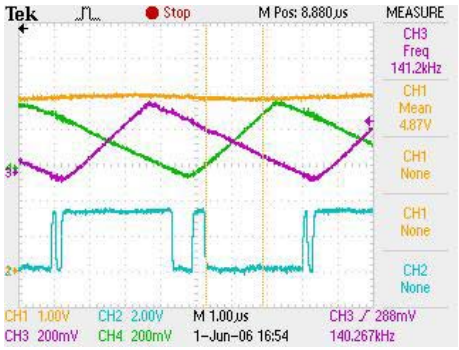

Fig. 10. Real time control interrupts timing, CH2

It was sufficient to let the current sharing be passively governed by the output resistance due to a sufficiently high resolution on the pulse width modulating output.

The tests in the laboratory showed that the gain in the feedback loop had to be significantly reduced below the theoretical calculated limit in order to stabilize the control. The reason for this is not fully explored yet.

Acknowledgment

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