The Stochastic Modeling of TiO_2 Memristor and Its Usage in Neuromorphic System Design

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***Abstract*—Memristor, the fourth basic circuit element, has shown great potential in neuromorphic circuit design for its unique synapse-like feature. However, though the continuous resistance state of memristor has been expected, obtaining and maintaining an arbitrary intermediate state cannot be well controlled in nowadays memristive system. In addition, the stochastic switching behaviors have been widely observed. To facilitate the investigation on memristor-based hardware implementation, we built a stochastic behavior model of TiO_2 memristive devices based on the real experimental results. By leveraging the stochastic behavior of memristors, a macro cell design composed of multiple parallel connecting memristors can be successfully used in implementing the weight storage unit and the stochastic neuron – the two fundamental components in neural network (NN)s, providing a feasible solution in memristor-based hardware implementation.**

1. Introduction

As traditional von Neumann computing systems based on CMOS technologies gains less performance increment and energy efficiency from device scaling, neuromorphic hardware systems that potentially provide the capabilities of biological perception and information processing within a compact and energy-efficient platform have gained great attentions [1][2]. However, the hardware development of NNs in traditional VLSI circuits still falls behind from the following perspectives. First, the weight matrix storage by digital-analog convertors, capacitors, or floating gates, has low precision, high power consumption, and high area overhead. Second, the voltage-based matrix computation induces many design issues including voltage offset, noise generation and voltage saturation. Last but not the least, the architecture and connection of such neuromorphic systems are hard to scale up, limiting the size and function of hardware implementations [3].

Theoretically, an idea memristor exhibits similarly as a synapse in bio-tissues [4]: it "remembers" the total electric flux through the device as its memristance M, which can be leveraged as the weight between an input voltage and an output current such as $I = V/M$. Such device feature potentially provides a complementary solution in neuromorphic design.

However, at current stage, a large gap exists between the theoretical memristor characteristics and the experimental data obtained from real devices, raising severe concerns in feasibility of memristor-based hardware design. For instance, the memristor theory expresses a continuous and stable memristance change. Though an arbitrary intermediate state can be obtained by carefully setting current compliance and period in a single metal oxide memristor, the corresponding realization at large scale, *e.g.*, crossbar array, is very difficult after including intrinsic design constrains, process variations, *etc*. Keeping a memristor in its ON or OFF state (R_{on} or R_{off}), on the contrary, is much more controllable. Thus, memristors nowadays are utilized as "memristive switches" [9].

Moreover, metal oxide based memristor behaves stochastically and hence even a single memristive device demonstrates large variations in performance. More specific, the *static states* of a single memristive switch, *i.e.*, R_{on} and R_{off}, are not fixed, but have large variations with skewed distributions and heavy tails [10]. The switching mechanism of a memristive switch, that is, its *dynamic behavior*, performs as a stochastic process [11], which has been widely demonstrated in various materials [19][20]. Previous statistical analyses on memristors were limited to the binary switching as data storage. However, as an analog device in NN application, it is necessary to understand and model memristor's analog stochastic characteristic. Here, we refer memristor to TiO_2 thin-film device.

In this work, we built a stochastic behavior model of TiO_2 memristive devices based on the real measurement results [9][10] to better facilitate the exploration of memristive switches in hardware implementation. The model bypasses material-related parameters while directly linking the device analog behavior to stochastic functions. Simulations show that the proposed stochastic device model fits well to the existing device measurement results.

To overcome the gap between the theoretical and real characteristics of memristive devices, we propose a macro cell design composed of a group of parallel connected memristive switches. It utilizes multiple memristors to represent an analog value by leveraging the stochastic behavior. Though the design sacrifices the design density, it is still more efficient than the CMOS implementations in floating gates or capacitors [18]. The usage of macro cells in weight storage unit and stochastic neuron, the two fundamental elements of neuromorphic system [12], is then demonstrated. The macro cells can be naturally integrated into memristor crossbars that previously were proposed as weight storage in neuromorphic computation [21].

The remainder of the paper is organized as follows. Section 2 provides the preliminary knowledge. Section 3 describes the stochastic model and calibrates it with experimental data. Section 4 presents the macro cell design and shows its usages. At last, we conclude the paper in Section 5.

2. Preliminary

2.1 Fundamental Components in Neural Network

Inspired by biological system, NNs mimic neuron-synapse networks, in which synapses transmit weighted signals and neurons process these signals based on activation functions. Many NN functionalities can be obtained through different network topologies, training methods, and activation functions. However, two fundamental components are always essential:

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- ***The weight carrier*** for weight storage and signal modulation. The weights shall be represented by continuous analog state (or at least highly accurate digital states).
- ***The stochastic neuron*** can be taken as neuron with a probabilistic activation function. It has been widely used in modern NNs, *e.g.*, *Restricted Boltzmann Machine* (RBM).

2.2 Memristor and Its Potential in Neural Network

As illustrated in Figure 1(a), a memristor describes the relationship between flux (φ) and charge (q). The first physical demonstration of memristor was announced in 2008 through a TiO_2 thin-film material [14] depicted in Figure 1(b). The basic theoretical model contains of the static state represented by memristance M as $V = I \cdot M(w)$ and the dynamic behavior described by the movement of an internal state w under electrical excitation as $\frac{dw}{dt} = f(V, w)$. Note that the internal state w is physically meaningful. For example, w in a TiO_2 thin-film material is the width of its barrier. Memristor is considered as a potential candidate for efficient neuromorphic circuit realization. Many researches on theoretical analysis [5][6] and hardware implementation [7][8] were demonstrated.

2.3 Characteristics of Real Memristive Devices

Compared to theoretical characteristics of ideal devices, many non-ideal features have been revealed in real memristive devices. For example, a geometrical variation aware TiO_2 device model illustrated in Figure 1(c) was developed [15]. More importantly, although a single memristor can be tuned to arbitrary analog state, it is difficult to generalize this approach to large-scale designs because of the sneak paths. We face the unfortunate reality that only "memristive switches" presenting binary states are practical for designs with nano-devices [4].

Moreover, the stochastic behavior in dynamic switching process and large variations in static states have been widely observed in experimental results of metal oxide materials. In brief, the time to successfully change the state of a single memristive switch is not deterministic but follows a long tail distribution [9]. And R_{on} and R_{off} follow skewed distributions [10]. These non-ideal characteristics shall be considered in hardware implementations built with memristive switches.

Though many physical memristor models were built based on insight mechanisms [11][16][17], they cannot reflect the large variation induced by stochastic switching behavior. Stochastic models can better link the statistical measurement data to probability functions. But the existing stochastic models are limited to only the binary switching behaviors [9][10] and hence cannot capture the intermediate analog state.

3. Stochastic Model for Memristive Switch

We proposed a stochastic model for TiO_2 memristive switch based on both the inspection of the physical mechanisms [11][17] and the statistical analysis of experimental data [9][10]. Our model describes the stochastic memristive switching based on the behavior analysis in both static states and dynamic switching process.

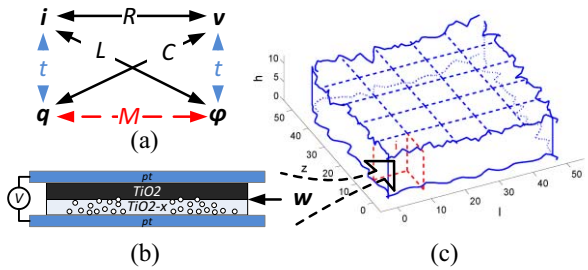

Figure 1. (a) Memristor is the fourth basic circuit element. (b) The ideal TiO_2 memristor model. (c) The geometric variation model.

3.1 On and OFF Static States

The static stochastic behavior can be described by the distributions of R_{on} and R_{off} . In TiO_2 memristor, the initial barrier width w follows a normal distribution and the device resistance exponentially depends on w. Therefore the distribution of state resistance follows the lognormal *probability density function* (pdf) function, which is [11]:

$$f_x(x;\mu,\sigma) = \frac{1}{x\sigma\sqrt{2\pi}} \cdot \exp\left(-\frac{(\ln x/\mu)^2}{2\sigma^2}\right), \quad x > 0. \tag{1}$$

Here, μ is the normal mean and σ is the standard deviation. Note that R_{on}or R_{off} does not change within a given static state because w remains constant. Therefore, we can use lognormal function (Lognorm) to generate the sampling data, such as

$$R_{\text{on}} = \text{Lognorm}\,(\mu_{\text{Ron}}, \sigma_{\text{Ron}}), \text{ and} \tag{2a}$$
$$R_{\text{off}} = \text{Lognorm}\,(\mu_{\text{Roff}}, \sigma_{\text{Roff}}). \tag{2b}$$

3.2 Dynamic Switching Process

The dynamics in TiO_2 memristor is a complex oxide electro-forming process. It can be explained as an electro-reduction and vacancy creation process caused by high electric fields and enhanced by electrical Joule heating. Usually the barrier width w is used to model the vacancy channeling mechanism. Although the vacancy channeling mechanism has been evidenced by experiments [11], it is difficult to match it to a pure physical model. Instead, our model is based on the analysis of three major behaviors; we start with a mathematical analysis of the analog stochastic switching behavior from the statistical aspect, and then bridge the parameters in mathematical expression with the physical excitation. At last, the impact of over tune is integrated into the stochastic model.

3.2.1 Analog Stochastic Switching Behavior

The stochastic resistance changing has been observed in high frequency measurement at low voltage [17]. The time dependency of switching probability can be approximated by the *cumulative probability function* (CDF) of lognormal distribution, such as [9]:

$$P(\text{Success switch}) = F(t_{\text{switch}};\mu_t,\sigma_t) = \frac{1}{2}\text{erfc}\left[-\frac{(\ln t_{\text{switch}}/\mu_t)^2}{\sqrt{2}\sigma_t{}^2}\right] \tag{3}$$

Here, t_{switch} represents the pulse width of activation time. And μ_t and σ_t are related to the external voltage V.

Instead of studying the complicated physical mechanism and its impact, we use mathematical method to analyze the ON-OFF switching probability. According to Eq. (3), the ON-OFF switching probability can be approximated by a CDF of lognormal distribution, differentiation of $P(\text{Success switch})$ at t_{switch}, then is a pdf of the lognormal distribution, such as

$$\frac{dP(\text{Success switch})}{dt_{\text{switch}}} = f_{t_{\text{switch}}}(t_{\text{switch}};\mu_t,\sigma_t). \tag{4}$$

Eq. (4) describes the distribution of the increment of switching probability $dP(\text{Success switch})$ at time t_{switch} when applying a signal with a short pulse width dt_{switch}.

The switching mechanism of a memristive device is intrinsic. Hence, the characteristic of the stochastic behavior remains unchanged and follows the same probability function during its switching process. From its physical meaning perspective, Eq. (4) reflects the increment of switching probabil-

ity at time t_{switch}, which can be associated to the resistance change ΔR. Physically, a successful switching event with a pulse of t_{switch} indicates that the device resistance changes from R_{on} to R_{off}, or vice versa, that is, $\Delta R = |R_{\text{off}} - R_{\text{on}}|$.

Considering that both ON and OFF switching are the cumulative results of the analog resistance changing and the increment of switching probability is directly reflected by the change of resistance, the change of analog resistance at time t_{switch} can be generated by mapping to the distribution of the increment of switching probability, leading to

$$\frac{dR}{dt} = (R_{\text{off}} - R_{\text{on}}) \cdot f_{t_{\text{switch}}}(t_{\text{switch}}; \mu_t, \sigma_t). \quad (5)$$

3.2.2 Time & Voltage Dependency of Switching Probability

Time and voltage dependency of switching probability describes the switching probability of memristive switch under applied voltage V and activation time t_{switch}. The switching process resulted from the cumulative impact of input signals can be modeled with CDF function. The lognormal switching time distribution comes from the nonlinear switching dynamics of the devices. Considering that the median switch time (μ_t) is exponentially dependent on the applied voltage amplitude V, we approximate μ_t as an exponential function, such as:

$$\mu_t = \exp(aV + b), \quad (6)$$

where a and b are fitting parameters.

Since σ_t has only a weak dependence on V, we can approximate the relationship between σ_t and V by a hard threshold squashing function, such as

$$\sigma_t = \begin{cases} \sigma_{\text{thres\_H}} & (\sigma_t \geq \sigma_{\text{thres\_H}}) \\ cV + d & (\sigma_{\text{thres\_L}} < \sigma_t < \sigma_{\text{thres\_H}}) \\ \sigma_{\text{thres\_L}} & (\sigma_t \leq \sigma_{\text{thres\_L}}) \end{cases}. \quad (7)$$

Where, c and d are fitting parameters. $\sigma_{\text{thres\_H}}$ and $\sigma_{\text{thres\_L}}$ are the upper and lower boundaries, respectively. Our model applies two individual sets of fitting parameters to ON and OFF switching processes.

3.2.3 The Resistance Shifting Due To Over Tune

Over tune stands for the behavior when one or more external voltage pulses continue being applied in the switching direction after the state switching of memristor already successes. For example, apply an ON switching signal to a device already in ON state. Based on the vacancy channeling mechanism, the over tune in OFF state continues eliminating the oxygen vacancy until all the oxygen vacancies disappear and the device becomes an insulator. In ON state, the over tune creates more oxygen vacancies to form more conducting channels. The device mechanism becomes less appropriate to be modeled with barrier width w since the channel frontier no longer exists. The resistance shifting in real devices is even more complex after including thermal, electron kinetic energy, and other physical issues. During over tune, a memristor device remains in the same static state and the resistance shifting follows the static resistance distribution. However, a systematic impact on μ_{Ron} and μ_{Roff} has been observed [10].

Here, we use a statistical method to analyze the impact of over tune on the resistance shifting. The charge q flowing through the device is used as the input variable, which has a direct impact on the number of oxygen vacancies and the device resistance. To exhibit the trend of resistance shifting, a linear approximation can be assumed between the passing charge q and the mean shifting μ_{shift} as [14]:

$$\mu_{\text{shift}} = e \cdot q = e \cdot \left(\frac{V}{M}\right) \cdot t \quad . \quad (8)$$

Here, e is the fitting parameter that describes the shift speed of mean, M is the current memristor resistance. The new μ_{Ron} and μ_{Roff} can be calculated from Eq. (7):

$$\mu'_{\text{Ron}} = \mu_{\text{Ron}} - \mu_{\text{on-shift}} = \mu_{\text{Ron}} - e_{\text{on}} \cdot q, \ \mu'_{\text{Ron}} \geq 0. \quad (9a)$$
$$\mu'_{\text{Roff}} = \mu_{\text{Roff}} + \mu_{\text{off-shift}} = \mu_{\text{Roff}} + e_{\text{off}} \cdot q. \quad (9b)$$

Though more complicated fitting equations can be established, such an approach is impractical and unnecessary at current stage considering of insufficient experimental data available. The resistance shifting caused by over tune is constrained within the target resistance state, demonstrating less impact on the overall memristor characteristic compared to the ON-OFF switching.

3.3 Stochastic Model Verification

We verified the proposed stochastic model from perspectives of static states and dynamic switching process.

Static States: Figure 2 shows the resistance distributions of a memristive switch in ON and OFF states. The blue bars in the figure are real measurement data of a TiO_2 memristive switch [10]. The results show that the lognormal distribution fits well to the real device data in ON state. However, in OFF state, the heavy tail is captured but the median value is slightly skewed. Though the distribution of R_{off} is not perfectly fitted, the error in distribution fitting of R_{off} has ignorable impact in the circuit simulation since R_{off} is more than two orders of magnitude higher than R_{on}.

Dynamic Switching Process: Figure 3 shows the time dependencies of ON and OFF switching probability at different applied voltages. The results have high approximation to the experimental results [9]. The error mainly comes from the approximation of the relationship between σ_t and V. As aforementioned, establishing a more reliable estimation of σ_t requires more experimental data.

Figure 4 shows the simulated analog resistance changing process of a TiO_2 memristor to better demonstrate the time and voltage dependency of switching probability and the resistance shifting due to over tune. The external voltage is set as $-3.0V$ to switch the memristor from R_{off} to R_{on}. The 100 curves in the figure represent the resistance changings by repeating 100 times of the ON switching procedure for the same device. The distribution of 100 tests agrees well with the switching probability curve at -3.0V in Figure 3(a): about 40% of the curves reach R_{on} before 0.1 S.

Considering the obvious stochastic behavior of memristive device at nanometer regime, traditional device modeling based on curve fitting is not enough. In this work, we built a stochastic model for TiO_2 memristor by bridging the key physical

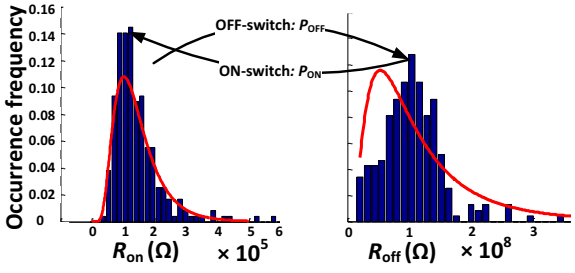

Figure 2. The static state distributions of a memristive switch.

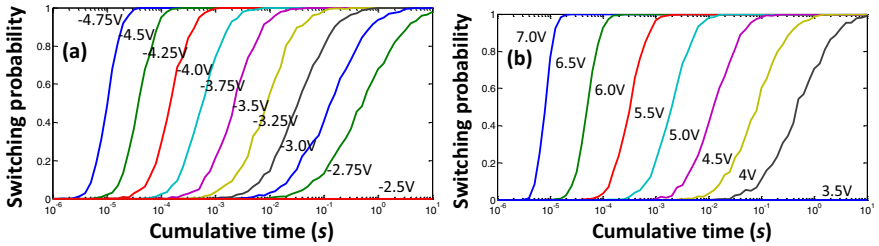

Figure 3. The time dependency of ON (a) and OFF (b) switching at different external voltages *V*.

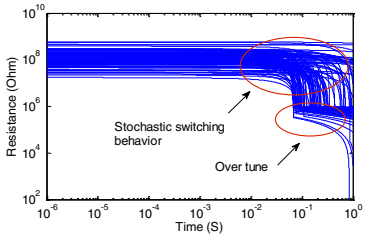

Figure 4. The analog switching process of a TiO_2 memristor.

mechanisms and the experimental data fitting. *The model combines the stochastic characteristics in static states and dynamic switching process together, and extends the stochastic study to the analog state while still holding high approximation to the existing data.* The accurate and fast estimation on the distribution of device's analog states makes the proposed model more meaningful for higher level circuit and system designs. This model can be generalized to other metal oxide memristors [19][20] for the same stochastic nature, that is, the percolation property of the thin dielectric soft breakdown [22]. The proposed model can be further enhanced by integrating with reliable physical model that precisely describes the stochastic switching mechanism. The complex and slow physical model generates the required distribution data to develop the proposed fast stochastic model.

4. Memristive Switches in Neural Network

Our primary interest is to effectively utilize memristive switches and provide feasible designs for NN hardware. Rather than digging into specific NNs, we realized two fundamental NN components with memristive switches: the weight storage unit and the stochastic neuron for binary/continuous value generation. To ease the following discussion, we change the expression of memristive switches from resistance R (in unit Ω) to conductance G (in unit S), where $G = 1/R$.

4.1 Weight Storage Units

Storing high-precision continuous weight is beyond the capability of a single memristive switch. We proposed a ***macro cell*** design composed of a group of parallel connected memristive switches for weight storage.

4.1.1 Characterization of Multiple Memristive Switches

Multiple memristive switches connected in serial or in parallel can provide multi-level conductance (resistance) values by simply combining the ON and OFF states of these devices. Comparing the two connection topologies, the design of parallel connection can be easily adapted on crossbar arrays. Also, it can provide a linear function of the read-out current, mitigating the pressure on sensing circuit. Thus, a group of parallel connected memristive switches is adopted in our design. The programming/detecting on the different ON and OFF combinations is realized through the peripheral circuit.

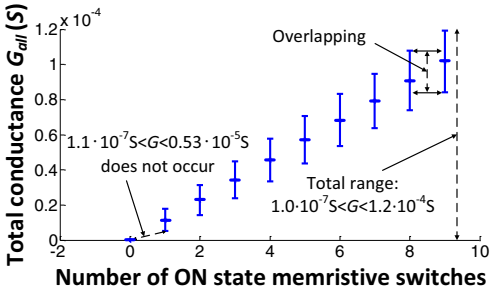

Figure 5. The conductance distribution of parallel connected memristive switches.

Here we take 9 parallel connected switches as an example. Figure 5 shows the distribution of its overall conductance G_{all}. To evaluate the impact of resistance in OFF state, we gradually increase the device number in ON state and remain the others in OFF state. The simulation result shows that the mean and deviation of G_{all} linearly grows as the number of ON memristive switches increases. Moreover, when all the memristive switches are in OFF state, the variation is negligible, indicating the variation in OFF State has little impact on the total conductance. In other words, the ON-state variation dominates the distribution of G_{all}. Thus, with more memristors in a macro cell, it can achieve larger conductance range, roughly proportional to G_{ON} times number of memristors.

4.1.2 Macro cell – A Continuous Weight Storage Unit

The parallel connection of memristive switches can be easily adopted in crossbar arrays. Let's use a 3×3 memristive switch crossbar in Figure 6(a) as an example. By combining the three inputs wires together and connecting the three output wires, the 9 memristive switches in this structure are parallel connected. We name such a structure as a ***macro cell***.

The given example has 10 possible ON-OFF device combinations, corresponding to 10 different conductance levels. Ideally, the 10 conductance levels can be differentiated by tuning the number of memristive switches in ON state. Unfortunately, as the simulation result in Figure 5 shows that the large resistance variation of ON state causes overlapping of conductance distribution, which is problematic in realizing traditional digitalized data storage for lacking of noise margin between adjacent levels. However, it also indicates continuous analog weight storage since a macro cell can achieve any arbitrary conductance within the overlapping range. For instance, the total conductance G_{all} of the macro cell in Figure 6(a) ranges from $0.53 \cdot 10^{-5}$S to $1.2 \cdot 10^{-4}$S. The unreachable conductance ranges from $1.1 \cdot 10^{-7}$S to $0.53 \cdot 10^{-5}$S, corresponding to the region from the upper bound of 9 switches in OFF state to the lower bound when only one switch is in ON state.

4.1.3 Feedback Attempt Scheme

A feedback attempt scheme can be used to achieve target conductance in macro cells. Figure 6(a) illustrates the conceptual diagram of the programming scheme. First, the number of memristive switches in ON state is determined to tune the overall conductance roughly. The output current is detected to check if the target G has been reached. A feedback control then is given to finely tune the macro cell memristor conductance. If the detected current is not within the absolute error threshold E, an ON state memristor is randomly selected to reset and then set again. Under a given operation condition, the

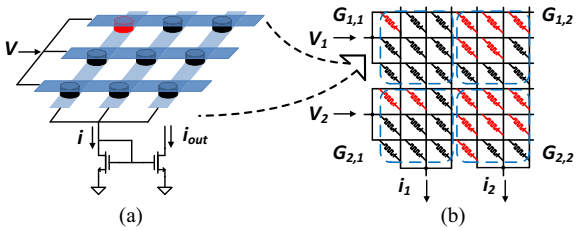

Figure 6. (a) A macro cell containing of 9 memristive switches on a 3x3 crossbar. (b) Partitioning a 6x6 memristive switch crossbar to obtain a 2x2 macro cell crossbar for continuous weight storage.

target conductance may not be obtained within a certain number of tryouts, indicating that either one or more memristors are too conductive or too resistive. We need to gradually reduce or increase the memristor number on ON state until the total conductance falls into tunable range. Then, restart the programming through the random attempt scheme.

In weight storage unit design, voltage pulses are used to control the switching of memristive switches. The pulse width t_{switch} is fixed, which is determined by the speed requirement. The amplitude V with ~100% switching probability is required to ensure the deterministic switching.

Figure 7 summarizes the average and the worst-case reconfiguration cycles to approach the different target conductance. The target conductance G_{Tar} can be generated by comparing to a reference current signal. Each data in the figures represents the statistical results of 1 million samples. The simulation results show that reconfiguration cycles increases linearly as the target conductance rises, while dramatically increases as the threshold error E decreases. More importantly, it shows that the proposed feedback attempt scheme can already achieve high precision programming within affordable attempts: any target conductance can be approached within on average 25 attempts with the error of $E = 0.1 \cdot 10^{-5}$S, corresponding to only 1% of the achievable conductance range. In the worst-case study, when $E = 0.3 \cdot 10^{-5}$S, the macro cell reaches the target conductance within 50 attempts in most cases. A rough calculation of $(G_{max} - G_{min})/2E$ implies that the macro cell can achieve at least 17 non-overlapping conductance levels rather than 10 levels obtained from ON/OFF combinations. If more attempts are affordable, we can increase to 50 non-overlapping conductance levels by reducing E to $0.1 \cdot 10^{-5}$S.

4.1.4 *Macro Cells in Crossbar*

The proposed macro cell can be easily adopted on larger crossbar structure. Figure 6(b) shows an example in which a 6×6 memristive switch crossbar is partitioned into 4 macro cells to implement a 2×2 weight matrix. The design sacrifices density while offering a practical and reliable way to realize continuous resistance state for analog storage and computation via binary switching memristors. The biggest advantage of such a design is the dramatical decrement of programming complexity: a complex and slow feedback scheme is necessary when tuning a memristor to a specific analog state. In contrast, binary switching of memristors can adopt the existing memory programming scheme that is simple and reliable.

Compared with the crossbar array implementation by using floating gates or capacitors [18], memristors enable simpler structure. Moreover, the charge-based CMOS devices require certain dimension to guarantee data accuracy, while the memristor technology can easily shrink. Thus, though a macro cell employs multiple memristors, it still provides better area efficiency (1~2 orders) over CMOS technologies.

4.2 Stochastic Neurons

The stochastic switching process is a severe issue for non-volatile memories with memristive switches. However, with careful design, it can be leveraged in designing stochastic neurons. Generally, stochastic neurons can be categorized into the binary neuron and the continuous value stochastic neuron.

4.2.1 *Binary Stochastic Neuron*

Binary stochastic neuron generates random binary pulse signals, which uses external voltage signals to control the probability of 0 (OFF) or 1 (ON) generation. Figure 8 illustrates the design of a binary stochastic neuron with a memristive switch. The operation timing diagram is given in the inner set of the figure. Figure 9 shows the voltage dependency of ON and OFF switching of a TiO_2 memristive switch. Each curve has a fixed pulse width. The voltage dependency shows a normal dependency between the applied voltage and the switching probability, where t_{switch} has a log impact on the means and deviations of switching distributions.

Accordingly, the binary stochastic neuron can control the probability of random numbers by applying a fixed pulse width t_{switch} and adjusting voltage amplitude V. Figure 9 also demonstrates the tradeoff between t_{switch} and the tunable range of V. The longer pulse width results in the lower applied voltage and the wider tunable range, which alleviates the hardware design complexity but the speed of circuit operation exponentially reduces. The shorter pulse width makes the circuit run much faster, at the cost of smaller tunable range and the increased risk of device damage. A related work partially verified our design by using contact-resistive random-access-memory to build random number generator [13].

4.2.2 *Continuous Value Stochastic Neuron*

Continuous value stochastic neuron generates random pulse signal. The voltage amplitude of the pulse signal is an analog value, which falls into a given distribution with controllable mean and noise. As illustrated in Figure 8, a continuous value stochastic neuron can be constructed by replacing the single memristive switch in a binary stochastic neuron with a macro

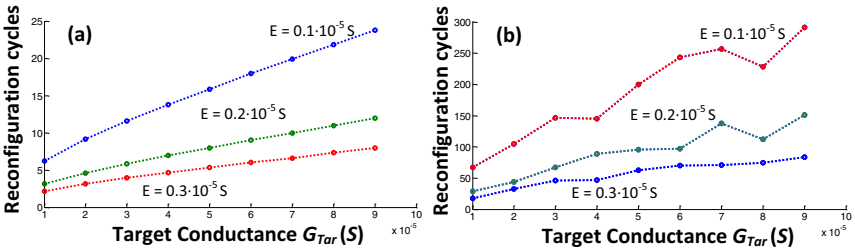

Figure 7. Average (a) and Worst-case (b) reconfiguration cycles to reach target conductance with different absolute error E.

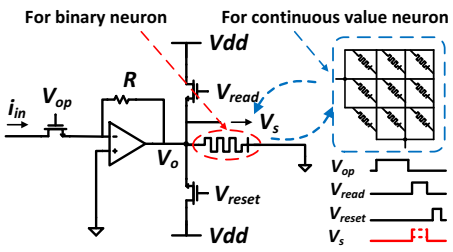

Figure 8. Binary/continuous value stochastic neuron design.

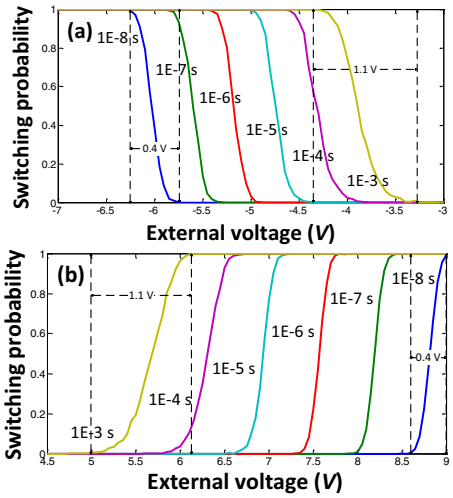

Figure 9. Voltage dependency of ON (a) and OFF (b) switching at different pulse widths t_{switch}.

cell. The noise and mean are controlled by the external voltage signal and the number of memristive switches in a macro cell.

Figure 10 shows the means and standard deviations of the noise generated by the proposed continuous value stochastic neuron. The designs with different macro cells containing $N = 4, 9, 16, 25$ memristive switches are compared. The means and the deviations of total conductance are controllable through the applied voltage. When a zero-mean noise signal is required, an offset current/voltage source can be added at the output V_s to cancel out the mean shifting considering that the voltage amplitude dependency of mean follows a normal CDF.

The variation comes from both the stochastic ON switching process and the randomness of ON state resistance. When $V > -3.95\,V$, the major contribution to variation comes from stochastic switching. Hence, the standard deviation decreases as the voltage amplitude drops down. When $V < -3.95\,V$, a memristive switch has >80% probability to successfully change to ON state, as shown in Figure 9. Thus, the randomness of ON state dominates and the deviation is saturated. After all, using memristive switches, it is possible to replace the traditional continuous stochastic neuron [12] with memristive switch based circuit to obtain higher area/ power efficiency.

5. Conclusion

In this paper, we proposed a stochastic memristor model from the macro perspective of stochastic characteristics in memristive switches. With the help of the model, we evaluated the performance of practicable memristive switches on two fundamental NN components. Weight storage unit for continues value is realized by using parallel connected memristive switches, or macro cell. A programming scheme is provided to tune the macro cell to any desired approachable conductance with high precision. For stochastic neurons, we made use of the stochastic behavior of memristive switches to benefit the natural generation of binary/continuous random values with controllable mean and variation. The controllability of noise has been also analyzed and demonstrated.

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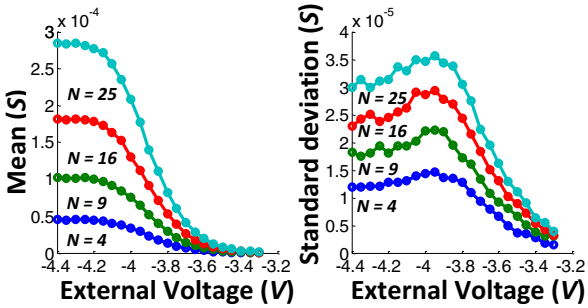

Figure 10. Voltage dependency of macro cell conductance. *N* is the number of memristive switches.

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