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A low-voltage band-gap reference circuit with second-order analyses

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SUMMARY

A new band-gap reference (BGR) circuit employing sub-threshold current is proposed for low-voltage operations. By employing the fraction of V_{BE} and the sub-threshold current source, the proposed BGR circuit with chip area of 0.029 mm^2 was fabricated in the standard 0.18 μm CMOS triple-well technology. It generates reference voltage of 170 mV with power consumption of 2.4 μW at supply voltage of 1 V. The agreement between simulation and measurement shows that the variations of reference voltage are 1.3 mV for temperatures from −20 to 100°C, and 1.1 mV per volt for supply voltage from 0.95 to 2.5 V, respectively. Copyright © 2010 John Wiley & Sons, Ltd.

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KEY WORDS: low-voltage; band-gap reference; sub-threshold current; voltage variation; second-order analysis

1. INTRODUCTION

Voltage references are key elements in the design of biasing schemes for analog or mixed-signal circuits. Today's major IC reference technology may be categorized into several types, such as band-gap references (BGRs), threshold voltages, and buried Zeners. These reference types use additional on-chip circuitry to provide a voltage or current that is insensitive to supply voltage, temperature or process variations, and should be conveniently implemented in the standard fabrication process. To meet the requirements, the BGR circuit is widely used in modem IC design for the most stable, less corner-sensitive, and popular reference voltage generators [1, 2].

Scale-down semiconductor technologies enable the development of circuits with structure size reduction [3, 4]. The shrinking of the transistors leads to the trend of low-power, low-voltage design [5]. A BGR voltage output of 1.2 V requires supply voltage over 1.5 V, which limits the applications at very low supply voltage. Many efforts have been made to reduce the reference voltage lower than 1.2 V for sub-1 V operation [6–8]. Technical literatures of curvature-compensated BGR circuit [9–11] were also proposed to improve issues of non-linear I–V characteristics of a diode or an N-time large diode with serial resistors. Those circuits employed operational amplifiers (OA), which resulted in larger chip area, more power consumption, and design efforts, especially for low supply voltages. The offset of the OA is also critical due to the difficulty to preserve temperature

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independence. There is a BGR circuit with a low-offset OA architecture in small area of $0.02\,\text{mm}^2$ for low-voltage, low-power applications [12]. However, it employed 130-nm CMOS technology and still consumes moderate power consumption. The sub-threshold characteristics of MOSFET's have been applied to generate low reference voltages for sub-1 V operation [13, 14]. However, the variation of reference voltage is still an issue due to the mobility and threshold voltage sensitivity with process corners.

This work proposes a simple BGR circuit using sub-threshold current without OA for low-power sub-1 V operations. The key idea is that a small fraction of V_{BE} in parasitic bipolar transistors and the difference of two V_{BE}'s are combined to generate the reference voltage of 170 mV. The proposed BGR circuit and its operation are described in Section 2. Further analyses of the proposed circuit with second-order effects are presented in Section 3. The simulation and measurement results are demonstrated in Section 4. The last section gives conclusions.

2. THE PROPOSED BGR CIRCUIT

Generally, the BGR voltage utilizes circuit techniques to compensate temperature variation of V_{BE} in a bipolar transistor with thermal potential $V_T(=kT/q)$, where T is the absolute temperature, $q=1.6\times10^{-19}\,\text{C}$, and $k=1.38\times10^{-23}\,\text{J/}^{\circ}\text{K}$. Since V_{BE} has a negative temperature coefficient

$$\gamma_{V_{\text{BE}}}\left(=\left.\frac{\partial V_{\text{BE}}}{\partial T}\right|_{T=T_{\text{r}}}<0\right)$$

it can be linearly extrapolated around the reference temperature T_{r}, i.e.

$$V_{\text{BE}}\cong V_{\text{BE0}}+\gamma_{V_{\text{BE}}}\cdot(T-T_{\text{r}}) \tag{1}$$

where V_{BE0} is the base-to-emitter voltage of a bipolar transistor at temperature T_{r}. Based on the concept of compensating temperature variation, a BGR scheme shown in Figure 1(a) is proposed to improve the circuit with merits of small area, low power, low supply voltage, etc. The proposed circuit can be divided into three parts. The first part is the start-up circuit with two MOS transistors (M6, M7) and a capacitor (C1). The next is the sub-threshold current generator circuit composed of the four MOS transistors (M1–M4) and a resistor (Rs). The core of the BGR circuit utilizes

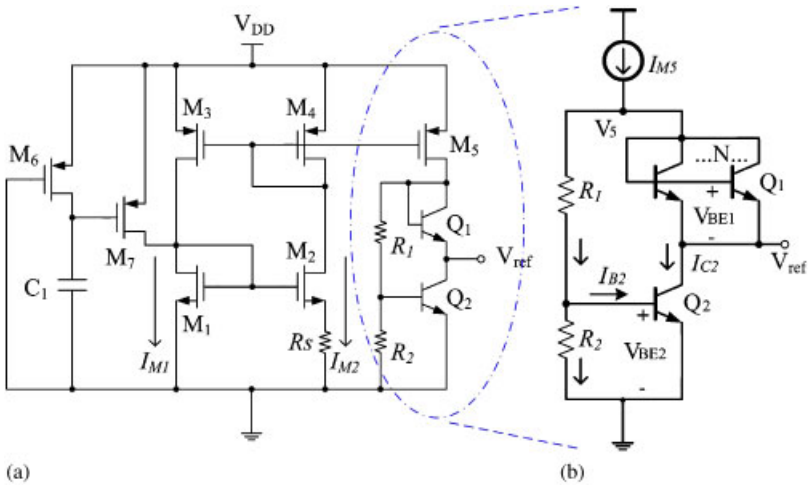

Figure 1. (a) The proposed band-gap reference circuit and (b) simplified sub-1 V band-gap reference core circuit.

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Table I. Detailed dimensions of the devices.

Component	Parameter
M_1	$W=2\,\mu m,\ L=2\,\mu m$
M_2	$W=100\,\mu m,\ L=2\,\mu m$
M_3, M_4	$W=25\,\mu m,\ L=6\,\mu m$
M_5	$W=28\,\mu m,\ L=2\,\mu m$
M_6	$W=1\,\mu m,\ L=20\,\mu m$
M_7	$W=60\,\mu m,\ L=1\,\mu m$
R_1	$130\,k\Omega$
R_2	$800\,k\Omega$
Rs	$350\,k\Omega$
Q_1(Emitter area)	$2\,\mu m\times 2\,\mu m\times 8$
Q_2(Emitter area)	$2\,\mu m\times 2\,\mu m$

one MOS transistor (M5), two BJT transistors (Q1, Q2), and two resistors (R_1, R_2). The detailed dimensions of the devices are listed in Table I.

The purpose of start-up circuit is to avoid degeneracy of the current source circuit. The p-MOS (M7) is 'on', since the voltage across the capacitor C1 is zero as the circuit is activated at the beginning; thus, the current sourced by M7 forces the gate voltages of M1 and M2 to increase. Therefore, the current source circuit deviates from the degenerate status. The capacitor C1 charges as transistor M6 is 'on'. The transistor M7 goes into cut-off region when the voltage drops across C1 approaching V_{DD}.

The second part named current source circuit provides constant current source independent of the supply voltage. At the initial state, the four MOS transistors M1–M4 might work at some operating Q point (e.g. all in cut-off region). After start-up, these transistors can be operated in strong or weak inversion depending on the sizes of M1–M4, and Rs. If the transistor is in weak inversion for low-power consumption, the drain current (I_D) can be expressed as [15]

$$I_D = \frac{W}{L}\cdot I_{D0}\cdot \exp\left(\frac{V_{GS}}{nV_T}\right) \tag{2}$$

where W and L are the channel width and length of MOS transistor, I_{D0} is a characteristic current and the slope factor n is $1+C_d/C_{ox}$, in which C_d is the surface depletion capacitance, C_{ox} is the gate oxide capacitance. From Equation (2) the gate source voltage V_{GS} then can be expressed as follows:

$$V_{GS} = nV_T\cdot \ln\left(\frac{I_D}{(W/L)\cdot I_{D0}}\right) \tag{3}$$

when the MOS transistors M1 and M2 are operated at weak inversion, voltage drop across the resistor Rs is

$$V_{Rs} = \Delta V_{GS} = V_{GS1} - V_{GS2} = nV_T\cdot \ln\left(\frac{(W/L)_2 I_{M1}}{(W/L)_1 I_{M2}}\right) \tag{4}$$

The current through Rs can be written as I_{M2} with $I_{M1}=I_{M2}$, if M3 and M4 are identical.

$$I_{M2} = \frac{V_{Rs}}{Rs} = \frac{n}{Rs}V_T\cdot \ln\left[\frac{(W/L)_2}{(W/L)_1}\right] = \frac{n}{Rs}\frac{kT}{q}\cdot \ln\left[\frac{(W/L)_2}{(W/L)_1}\right] \tag{5}$$

It can be observed that I_{M2} is nearly independent of supply voltages. Although the current may slightly increase as temperature increases, the current of the NPN transistors in the BGR core also increases. The important point is that the voltage drop in the NPN transistors is a logarithmic function of current. The reference voltage can still remain almost constant for such current variations.

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Figure 1(b) illustrates the simplified sub-1 V BGR core circuit, where the current source is provided from the sub-threshold current generator. By assuming the transistors Q1 and Q2 in forward active mode, the collector currents can be represented as follows:

$$I_{C1} = N \cdot I_S \cdot \exp\left(\frac{V_{BE1}}{V_T}\right) \tag{6a}$$

$$I_{C2} \cong I_S \cdot \exp\left(\frac{V_{BE2}}{V_T}\right) \tag{6b}$$

where N is defined as the area ratio of NPN transistors Q1 and Q2. They are obtained by vertical n+/p-well/deep n-well structures, which is provided by normal CMOS triple-well process. With the relation of $I_{C2} = I_{C1} \cdot (\beta_1 + 1)/\beta_1$, where β_1 is the current gain of Q1, the following expression is obtained:

$$N\left(\frac{\beta_1 + 1}{\beta_1}\right) = \exp\left(\frac{V_{BE2} - V_{BE1}}{V_T}\right) \tag{7}$$

It also means that for $\beta_1 \gg 1$

$$\Delta V_{BE} \equiv V_{BE2} - V_{BE1} = V_T \cdot \ln\left[N \cdot \left(\frac{\beta_1 + 1}{\beta_1}\right)\right] \approx V_T \cdot \ln N \tag{8}$$

By referring to Figure 1(b), the current source provides current through Q1 (I_{C2}) and the current through R_1(I_{R1}), which is the sum of current through R_2(I_{R2}) and the base current of Q2 (I_{B2}). The relation is given as

$$I_{M5} = I_{C2} + I_{R1} = I_{C2} + (I_{R2} + I_{B2}) = I_{C2} + \left(\frac{V_{BE2}}{R_2} + \frac{I_{C2}}{\beta_2}\right) \tag{9}$$

Rearranging the above equation, we have

$$I_{M5} - I_{C2} = \frac{V_{BE2}}{R_2} + \frac{I_{C2}}{\beta_2} \tag{10a}$$

$$I_{C2} = \frac{\beta_2}{\beta_2 + 1} \cdot \left(I_{M5} - \frac{V_{BE2}}{R_2}\right) \tag{10b}$$

The reference output voltage has the relation of

$$V_{ref} + V_{BE1} = (I_{M5} - I_{C2})R_1 + V_{BE2} \tag{11}$$

By manipulating the above equation, the reference voltage is written as

$$V_{ref} = (I_{M5} - I_{C2})R_1 + (V_{BE2} - V_{BE1}) \tag{12}$$

Substituting Equations (8), (10a), and (10b) into Equation (12)

$$\begin{aligned} V_{ref} &= (I_{M5} - I_{C2})R_1 + V_T \ln N \\ &= \left(\frac{V_{BE2}}{R_2} + \frac{I_{C2}}{\beta_2}\right) \cdot R_1 + V_T \ln N \\ &= \frac{R_1}{R_2} V_{BE2} + V_T \ln N + \frac{R_1}{\beta_2} \cdot \frac{\beta_2}{\beta_2 + 1}\left(I_{M5} - \frac{V_{BE2}}{R_2}\right) \\ &= \frac{R_1}{R_2} V_{BE2} + V_T \ln N + \frac{R_1 \cdot I_{M5}}{\beta_2 + 1} - \frac{1}{\beta_2 + 1} \cdot \frac{R_1}{R_2} V_{BE2} \\ &= \frac{\beta_2}{\beta_2 + 1} \cdot \frac{R_1}{R_2} V_{BE2} + V_T \ln N + \frac{R_1 \cdot I_{M5}}{\beta_2 + 1} \end{aligned} \tag{13}$$

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The current I_{M5} can be replaced by the sub-threshold current source expressed in Equation (5) (denoted as I_{M2}) with multiplication factor M,

$$\begin{aligned} V_{\text{ref}} &= \frac{\beta_2}{\beta_2+1}\cdot\frac{R_1}{R_2}V_{\text{BE2}} + V_T \ln N + \frac{R_1}{\beta_2+1}\cdot M\cdot\frac{n}{\text{Rs}}\cdot V_T\cdot\ln\left(\frac{(W/L)_2}{(W/L)_1}\right) \\ &= \frac{\beta_2}{\beta_2+1}\cdot\frac{R_1}{R_2}V_{\text{BE2}} + V_T\cdot\left[\ln N + \frac{M\cdot n}{\beta_2+1}\cdot\frac{R_1}{\text{Rs}}\cdot\ln\left(\frac{(W/L)_2}{(W/L)_1}\right)\right] \\ &= \frac{\beta_2}{\beta_2+1}\cdot\frac{R_1}{R_2}V_{\text{BE2}} + \frac{kT}{q}\cdot\left[\ln N + \frac{M\cdot n}{\beta_2+1}\cdot\frac{R_1}{\text{Rs}}\cdot\ln\left(\frac{(W/L)_2}{(W/L)_1}\right)\right] \end{aligned} \tag{14}$$

The reference output voltage is composed of the negative temperature coefficient term of V_{BE2} and the positive term of V_T as we can see from Equation (14). By adjusting the devices properly, the constant reference voltage can be obtained. The important benefit of the second term

$$\frac{n}{\beta_2+1}\cdot\frac{R_1}{\text{Rs}}\cdot\ln\left(\frac{(W/L)_2}{(W/L)_1}\right)$$

of the positive temperature coefficient helps reduction of the area ratio N.

3. ANALYSES OF SECOND-ORDER EFFECTS

The non-linear terms with second-order effects, including the fraction of V_{BE2} and the factor of $1/\beta_2$, are further analyzed.

3.1. The analysis of V_{BE2}

The V_{BE2} of the BJT transistor Q2 is a function of temperature, according to the relationship proposed in [16], and is given by

$$V_{\text{BE2}}(T) = V_g(T) + [V_{\text{BE2}}(T_{\text{r}}) - V_g(T_{\text{r}})]\cdot\left(\frac{T}{T_{\text{r}}}\right) - (\eta-\alpha)\frac{kT}{q}\ln\left(\frac{T}{T_{\text{r}}}\right) \tag{15}$$

where η is bipolar structure-dependent factor (~ 4), and α is temperature coefficient ($=1$ for PTAT current in the BJT [17]). If the temperature variation of $V_g(T)$ for Si is negligible, we may get the temperature coefficient of V_{BE2} by differentiating the above equation with respect to temperature T,

$$\gamma_{V_{\text{BE2}}}(T) = \frac{\partial V_{\text{BE2}}}{\partial T} \approx \frac{1}{T_{\text{r}}}\cdot[V_{\text{BE2}}(T_{\text{r}}) - V_g(T_{\text{r}})] - (\eta-\alpha)\frac{k}{q}\left[1+\ln\left(\frac{T}{T_{\text{r}}}\right)\right] \tag{16}$$

where $V_g(T_{\text{r}}) = 1.12\,\text{V}$, $V_{\text{BE2}}(T_{\text{r}}) = 0.65\,\text{V}$, and $\gamma_{V_{\text{BE2}}}$ is approximately $-1.8\,\text{mV}/^\circ\text{K}$ at $T_{\text{r}} = 300^\circ\text{K}$ (i.e. $\gamma_{V_{\text{BE2}}}(T_{\text{r}})T_{\text{r}} \approx -0.54\,\text{V}$). After Equation (16) is substituted into Equation (15), the negative temperature variation of V_{BE2} can be obtained.

$$V_{\text{BE2}}(T) = V_g(T) + \gamma_{V_{\text{BE2}}}(T)\cdot T + (\eta-\alpha)\frac{kT}{q} \tag{17}$$

The second term $\gamma_{V_{\text{BE2}}}(T)\cdot T$ in the above equation is negative, which contains a non-linear term $-(\eta-\alpha)kT/q\ln(T/T_{\text{r}})$ shown in Equation (15). If an appropriate positive temperature coefficient term is added to V_{BE2}, the dominant temperature effects will be compensated. By subtracting the linear term from $V_{\text{BE2}}(T)$, the compensated constant reference voltage V_{comp} can be expressed as follows:

$$\begin{aligned} V_{\text{comp}}(T) &= V_{\text{BE2}}(T) - (\eta-\alpha)\frac{kT}{q} - \gamma_{V_{\text{BE2}}}(T_{\text{r}})\cdot(T-T_{\text{r}}) \\ &= -(\eta-\alpha)\frac{kT}{q}\ln\left(\frac{T}{T_{\text{r}}}\right) + [V_g(T) + \gamma_{V_{\text{BE2}}}(T_{\text{r}})\cdot T_{\text{r}}] \end{aligned} \tag{18}$$

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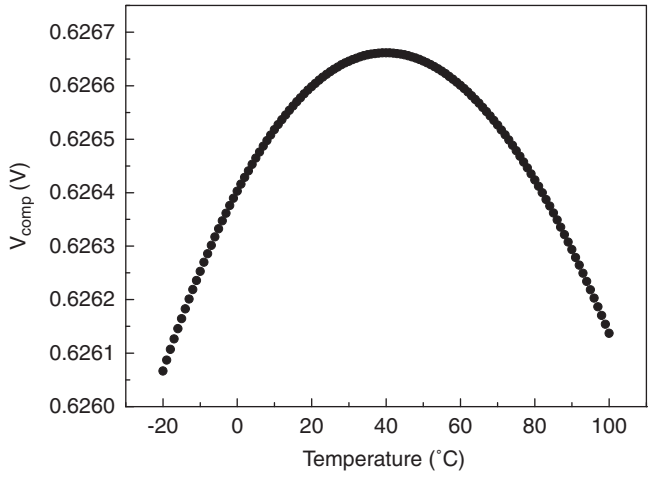

Figure 2. The compensated V_{BE}, V_{comp} shows the second-order effect of V_{BE2}.

The simulated V_{comp} is illustrated in Figure 2, in which the downward-concave second-order effect of V_{comp} with the constant offset of $V_g(T)+\gamma_{V_{\mathrm{BE2}}}(T_{\mathrm{r}})\cdot T_{\mathrm{r}}$ is demonstrated.

3.2. The analysis of current gain β_2

The reference output voltage shown in Equation (14) is also varied with $1/\beta_2$, which is also a function of temperature. In the proposed circuit, the BJT Q2 may be biased in the low-current region and is close to saturation mode. Therefore, the recombinations of carriers at the surface and in the emitter–base depletion region, as well as the formation of emitter–base channels make variations of $I_{\mathrm{B2}}/I_{\mathrm{C2}}(=1/\beta_2)$, which can be expressed as a function of temperature according to [17, 18].

$$\frac{1}{\beta_2(T)}=\frac{1}{\beta_{\mathrm{F}}}+\frac{1}{\beta_{\mathrm{R}}}\cdot\exp\left(\frac{q}{kT}(V_{\mathrm{BC2}}-V_{\mathrm{BE2}})\right)+\frac{I_{SE}}{I_{\mathrm{S}}}\cdot\exp\left(\frac{qV_{\mathrm{BE2}}}{kT}\left(\frac{1}{n_{EL}}-1\right)\right) \tag{19}$$

where β_{F}, and β_{R} are defined as the common-emitter short-circuit (B to C) current gains under forward and reverse active conditions, respectively. I_{S} is reverse saturation current between PN junctions,

$$I_{\mathrm{S}}(T)=K\cdot T^3\exp\left(\frac{-qV_g(T)}{kT}\right).$$

n_{EL} is an non-ideal low-current base–emitter emission coefficient, and I_{SE} is the non-ideal base–collector saturation current,

$$I_{SE}\equiv I_{SE}(T)=I_{\mathrm{S}}(T_{\mathrm{r}})\left[\frac{I_{\mathrm{S}}(T)}{I_{\mathrm{S}}(T_{\mathrm{r}})}\right]^{1/n_{EL}}$$

To verify that the value of β_2 is influenced by temperature, let us select $V_{\mathrm{BC2}}=0.52\,\mathrm{V}$ when $V_{\mathrm{CE2}}=0.18\,\mathrm{V}$, and $V_{\mathrm{BE2}}=0.7\,\mathrm{V}$. By substituting the values: $\beta_{\mathrm{F}}=27.2$, $\beta_{\mathrm{R}}=0.302$, and $n_{EL}=1.22$ (extracted from devices), it can be observed that the first term $1/\beta_{\mathrm{F}}$ on the right side of Equation (19) is temperature independent, and the second term

$$\frac{1}{\beta_{\mathrm{R}}}\cdot\exp\left(\frac{q}{kT}(V_{\mathrm{BC2}}-V_{\mathrm{BE2}})\right)$$

is increased with temperature, whereas the third term

$$\frac{I_{SE}}{I_{\mathrm{S}}}\cdot\exp\left(\frac{qV_{\mathrm{BE2}}}{kT}\left(\frac{1}{n_{EL}}-1\right)\right)$$

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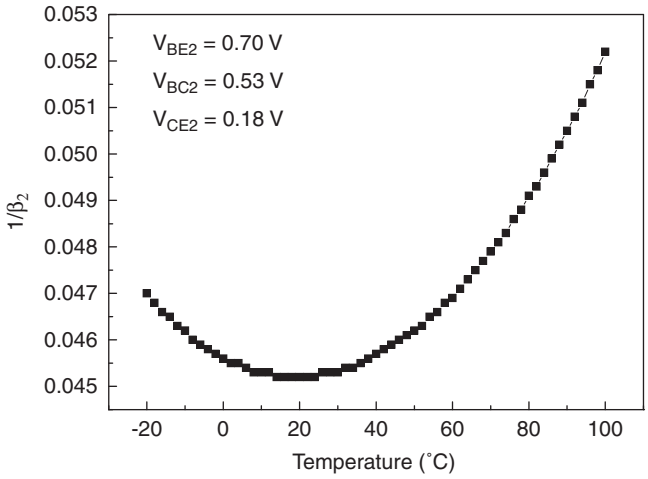

Figure 3. The $1/\beta_2$ varies with temperatures for $V_{BE2}=0.7\,V$, $V_{BC2}=0.52\,V$, and $V_{CE2}=0.18\,V$.

is decreased with temperature. Specifically, the third term dominates for low temperature ($<40^{\circ}C$), whereas the second term is more dominant at higher temperatures ($>40^{\circ}C$). The mathematic deduction confirms the simulation results of $1/\beta_2$ with temperatures from -20 to $100^{\circ}C$ in Figure 3.

According to the analyses of V_{BE2} and the β_2, thanks to $1/\beta_2$ with upward-concave variation with temperature that partially compensates downward-concave variation caused by V_{comp} in the proposed reference output voltage given in Equation (14).

4. SIMULATION AND MEASUREMENT RESULTS

The new BGR circuit was designed and implemented by using mixed-mode 0.18 μm triple-well CMOS technology. The deep n-well process is a standard build-in layer for the p-type substrate wafers in order to provide individual well potentials for N-MOS transistors. Thus, the n+/p-well/deep n-well structure forms NPN parasitic transistors at no extra manufacture cost. Since the NPN transistors are the parasitic components, the current gain $\beta_2=I_{C2}/I_{B2}$ may be lower. Figure 4 demonstrates the β_2 value as a function of V_{CE2}, in which β_2 is around 17 at room temperature when V_{BE2} is 0.7 V and V_{CE2} is over 0.16 V. Since the reference voltage (V_{ref}) is 0.17 V for the proposed BGR circuit, transistor Q2 shown in Figure 1(b) is still in forward active mode but close to saturation. Note that the β_2 value of 17 is still large enough for the proposed BGR circuit.

The ratio for the resistors and NPN transistors are chosen to be $R_1/R_2=\frac{13}{80}$ and $N=8$ in the proposed BGR circuit, respectively. Since the ratio R_1/R_2 is smaller than one, a fractional portion of band-gap voltage (V_g) is utilized. That is also why it can be operated at supply voltage lower than 1 V. To measure the reference voltage, an extra unity gain buffer was also included. The die microphotograph with core area $0.029\,mm^2$ is shown in Figure 5, including the unit gain buffer.

Figure 6 demonstrates the waveform of the proposed BGR circuit when the power supply is just turned on to 1 V. The time for the reference voltage reaching 170 mV is within 15 ms, which is shorter than the supply voltage switching time of 20 ms, since the circuit starts to work at the supply voltage lower than 1 V.

The comparisons of the simulated results of different process corners with the measured data for various supply voltages at room temperature and for various temperatures at supply voltage of 1 V are shown in Figures 7 and 8, respectively. The agreement between measurement and simulation is also observed. The measured data that increase or decrease by steps result from the resolution limitation of our oscilloscope. The variation of reference voltage is about 1.1 mV/V for supply voltage from 0.95 to 2.5 V, whereas the variation of reference voltage is 0.76% for temperatures from -20 to $100^{\circ}C$ at supply voltage of 1 V. It is worthily noted that the variations of reference

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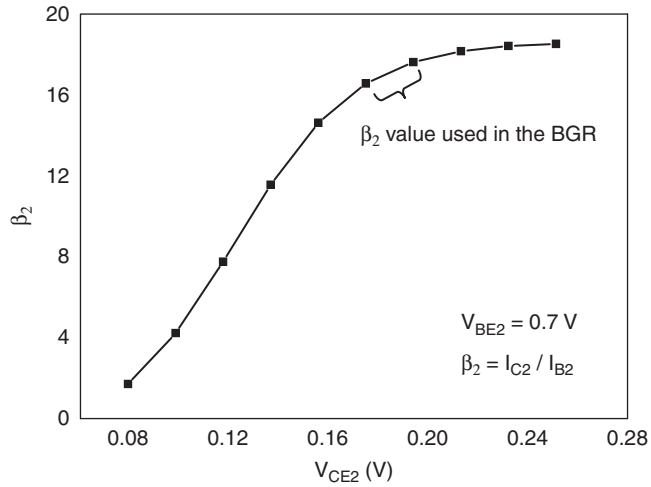

Figure 4. The β_2 values as a function of V_{CE2} with $V_{BE2}=0.7\,V$.

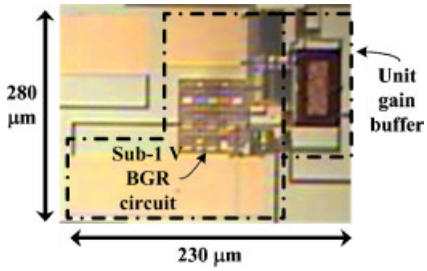

Figure 5. Microphotograph of the proposed BGR circuit.

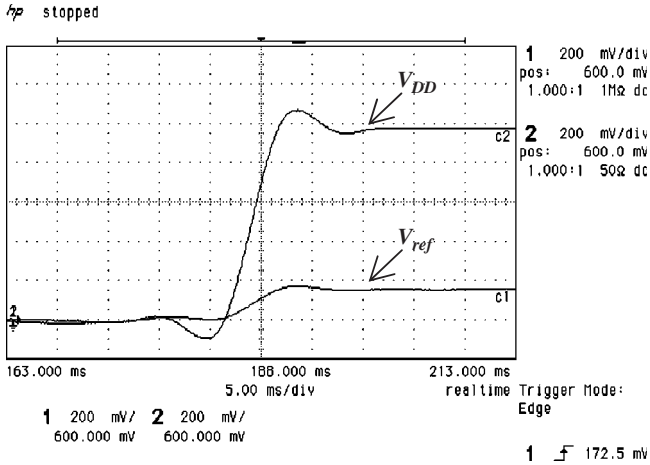

Figure 6. The waveform of the reference voltage when the power supply of 1 V is just turned on.

voltage for different process corners are much smaller than those using threshold voltages [13, 14] instead of band-gap.

The performance of the proposed circuit is summarized in Table II, which is compared with the band-gap voltage reference operated in 1.5 V (1.5 V BVR) [9], the curvature-compensated BGR with trimming (CCBRT) [10], the curvature-compensated Bi-CMOS band-gap (CCBG) circuit

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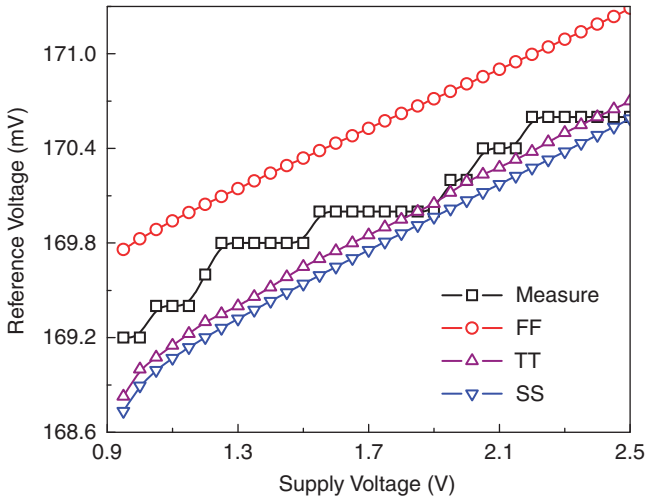

Figure 7. Comparison of the simulated results and the measured data for various supply voltages at room temperature.

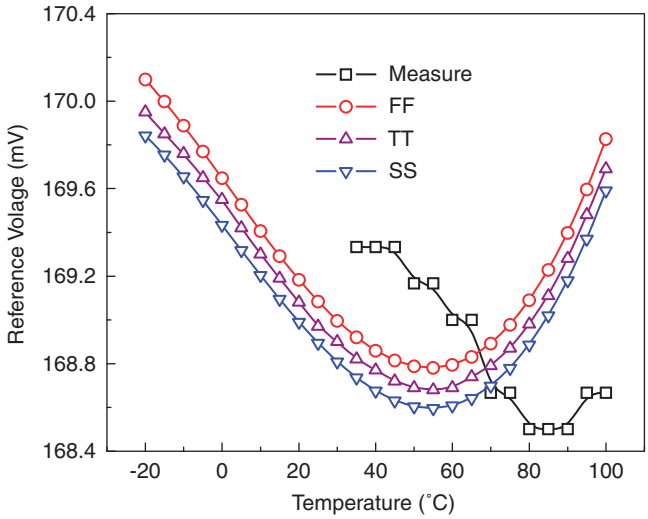

Figure 8. Comparison of the simulated results and the measured data for various temperatures at supply voltage of 1 V.

[11], and the BGR with a low-offset OA [12]. The proposed band-gap circuit achieves less power consumption at lower and wide-range supply voltages in smaller area.

5. CONCLUSIONS

The proposed simple BGR circuit by using parasitic NPN transistors achieves sub-1 V and low-power operation. The circuit was fabricated by 0.18 μm CMOS triple-well technology on chip area of 0.029 mm^2. The theoretical analysis of the proposed circuit shows the advantages of low BJT transistor ratio and slight compensation of the second-order effect. The measurement results also confirm those superior characteristics. It should be very useful for applications in many low-power analog circuits with small area at sub-1 V operations.

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Table II. Comparisons and specifications of the proposed CMOS BGR circuit design.

Parameter	Value				
	The proposed band-gap	[9]	[10]	[11]	[12]
Technology	0.18 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.8 μm Bi-CMOS	130 nm CMOS
Supply voltage	0.95–2.5 V	1.5 V	1.5 V	1 V	$1\sim2\,V$
Reference voltage @25°C	169.4 mV	1.117 V	1.112 V	536 mV	798 mV
Temperature Variation	0.76% (−20–100°C)	0.27% (0°C–80°C)	10 ppm/°C	20 ppm/°K (0°C–80°C)	6.64 ppm/°C (−50–160°C)
Power consumption	2.4 μW @$V_{DD}=1$ V	0.22 mW	82.5 μW	92 μW	26 μW @$V_{DD}=1$ V
Number of NPN transistors (diodes)	2	2	2	4	(2)
Area (mm^2)	0.029	0.057	0.71	0.25	0.02

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