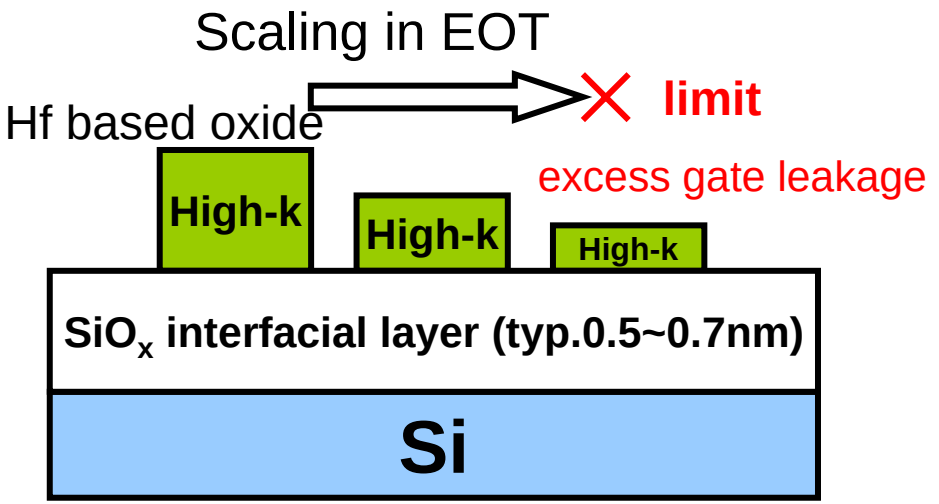
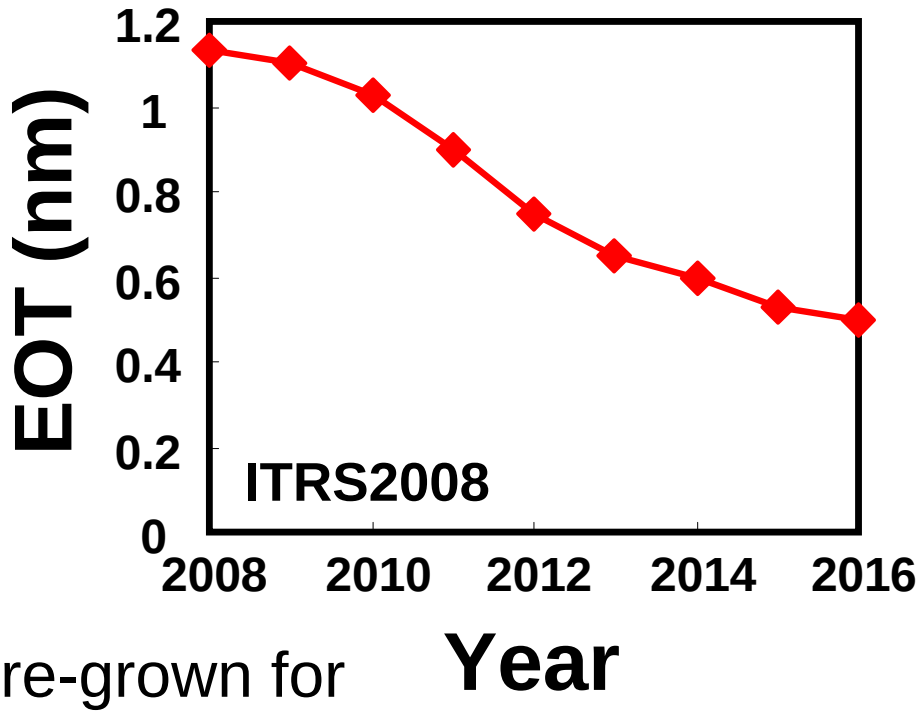
Selection of Rare Earth Silicate with SrO Capping for EOT Scaling below 0.5 nm

K. Kakushima, K. Okamoto*, T. Koyanagi*,
K. Tachi*, M. Kouda*, T. Kawanago*, J. Song*,
P. Ahmet*, K. Tsutsui, N. Sugii, T. Hattori*, H. Iwai*

Interdisciplinary Graduate School of Science and Engineering,
*Frontier Research Center
Tokyo Institute of Technology

Continuous scaling in gate dielectrics



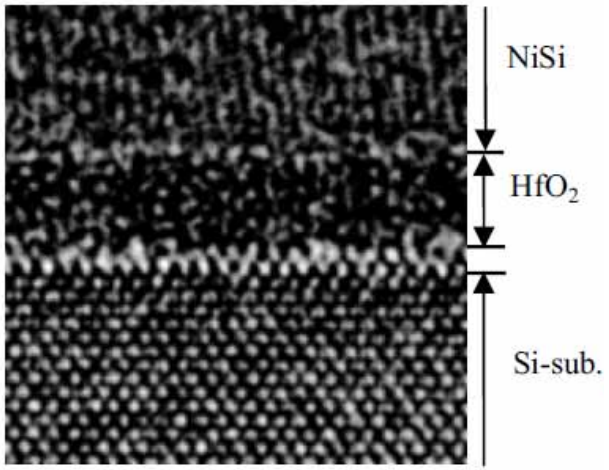


SiO_2 interfacial layer inserted or re-grown for
- recovery of degraded mobility
- interface state, reliability (TDDB, BTI), etc.

- **SiO_2-IL free structure (direct contact of high-k/Si) is required for EOT=0.5nm**
- **EOT scaling is expected down to 0.5 nm in ITRS**

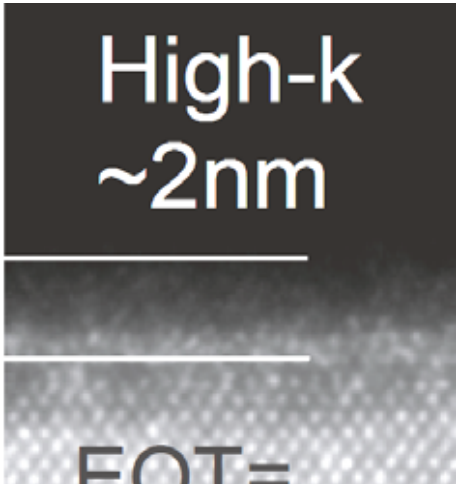
High-k gate dielectrics without SiO_x IL

EOT=0.49nm



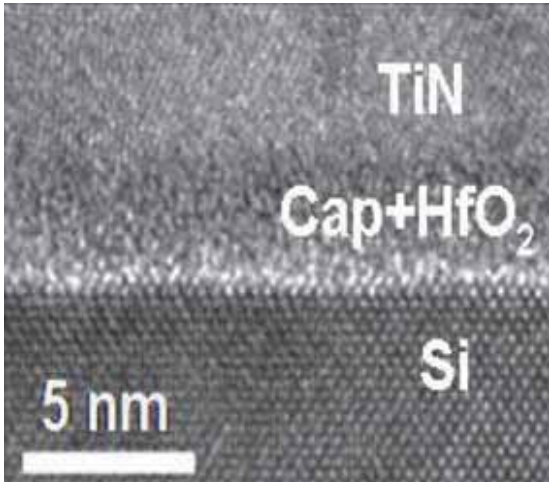
M. Takahashi, IEDM(2007)

EOT=0.59nm



J. Hauang, VLSI symp.(2009)

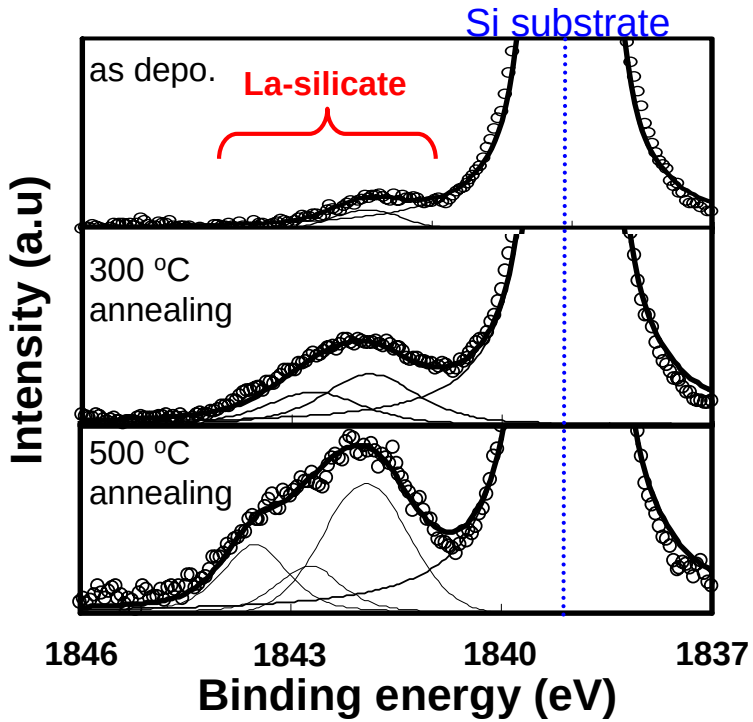
EOT=0.55nm

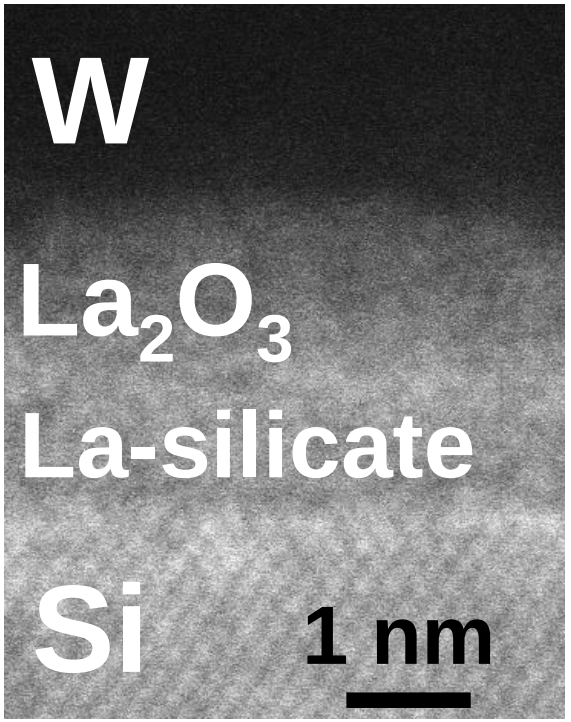


K. Choi, VLSI symp.(2009)

Special process and metal selection controlling oxygen atoms against SiO_x-IL formation

La_2O_3 for gate dielectrics





k=23

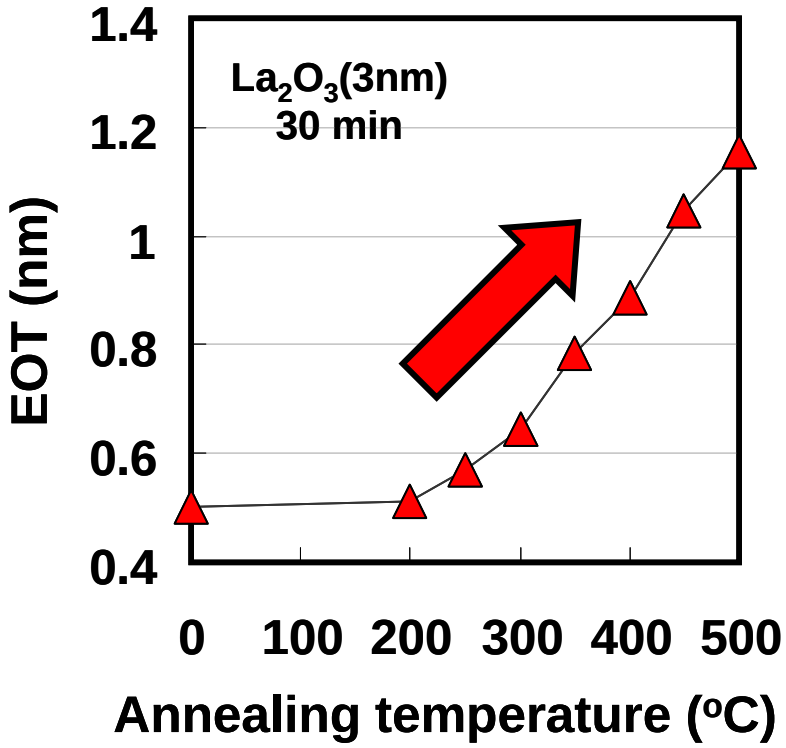
k=8~14

La_2O_3 + Si + nO_2

→ **La_2SiO_5, $La_2Si_2O_7$, $La_{9.33}Si_6O_{26}$, $La_{10}(SiO_4)_6O_3$, etc.**

La_2O_3 can achieve a SiO_x-IL free structure by forming La-silicate at the interface

Silicate reaction at La_2O_3/Si interface



1. Reactivity with Si substrate

ΔG ~ -100kJ/mol

2. Stable silicate phases

Reported La-silicate:
La_2SiO_5, $La_{10}(SiO_4)_6O_3$,
$La_{9.33}Si_6O_{26}$, $La_2Si_2O_7$, etc.

$LaO_{1.5}$:SiO_2 from 1:1 to 1:2

Prevent the excess silicate reaction

1. proper metal selection: ECS Trans. **11** (4), 319 (2007)
2. short period annealing: Appl. Phys. Lett. **90**, 102908 (2007)
3. other RE-silicates for interfacial layer (this work)

Purpose of this work

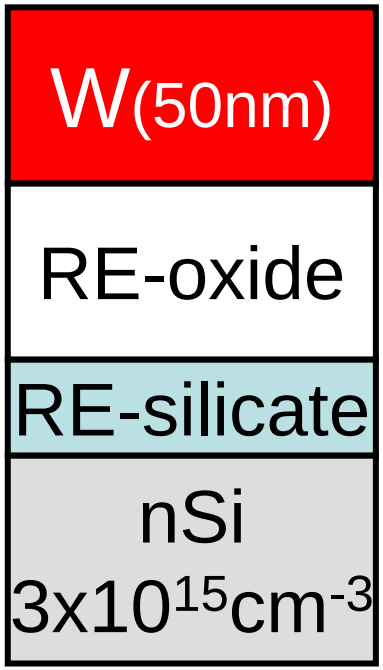
1. Material selection of RE-silicate as an interfacial layer for SiO_x-free gate stack

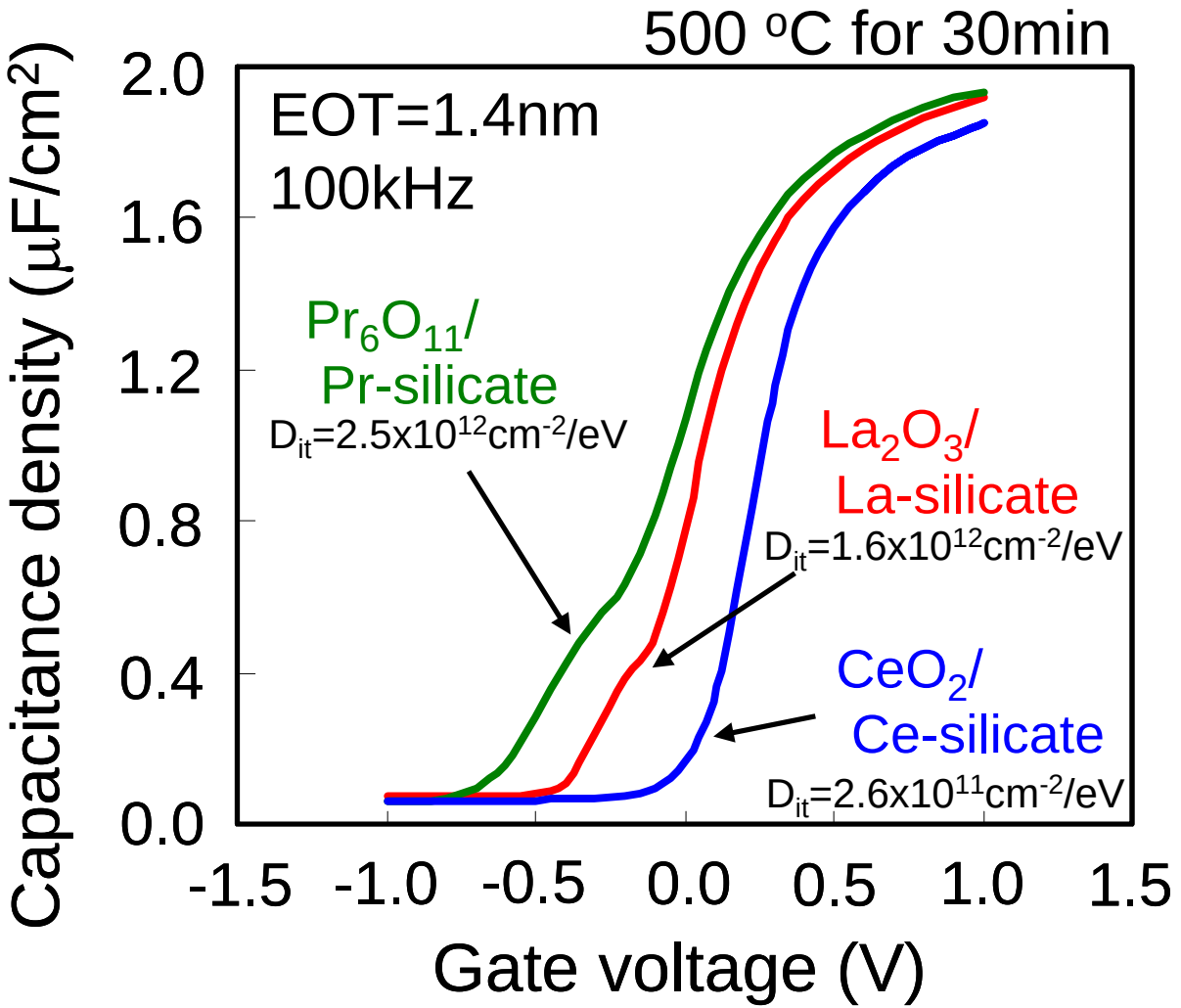
Selected RE-oxides:
La_2O_3 (k~23), CeO_x (k~32), PrO_x (k~32)

2. SrO capping effect for further EOT scaling

Selection of RE-silicate for interfacial layer

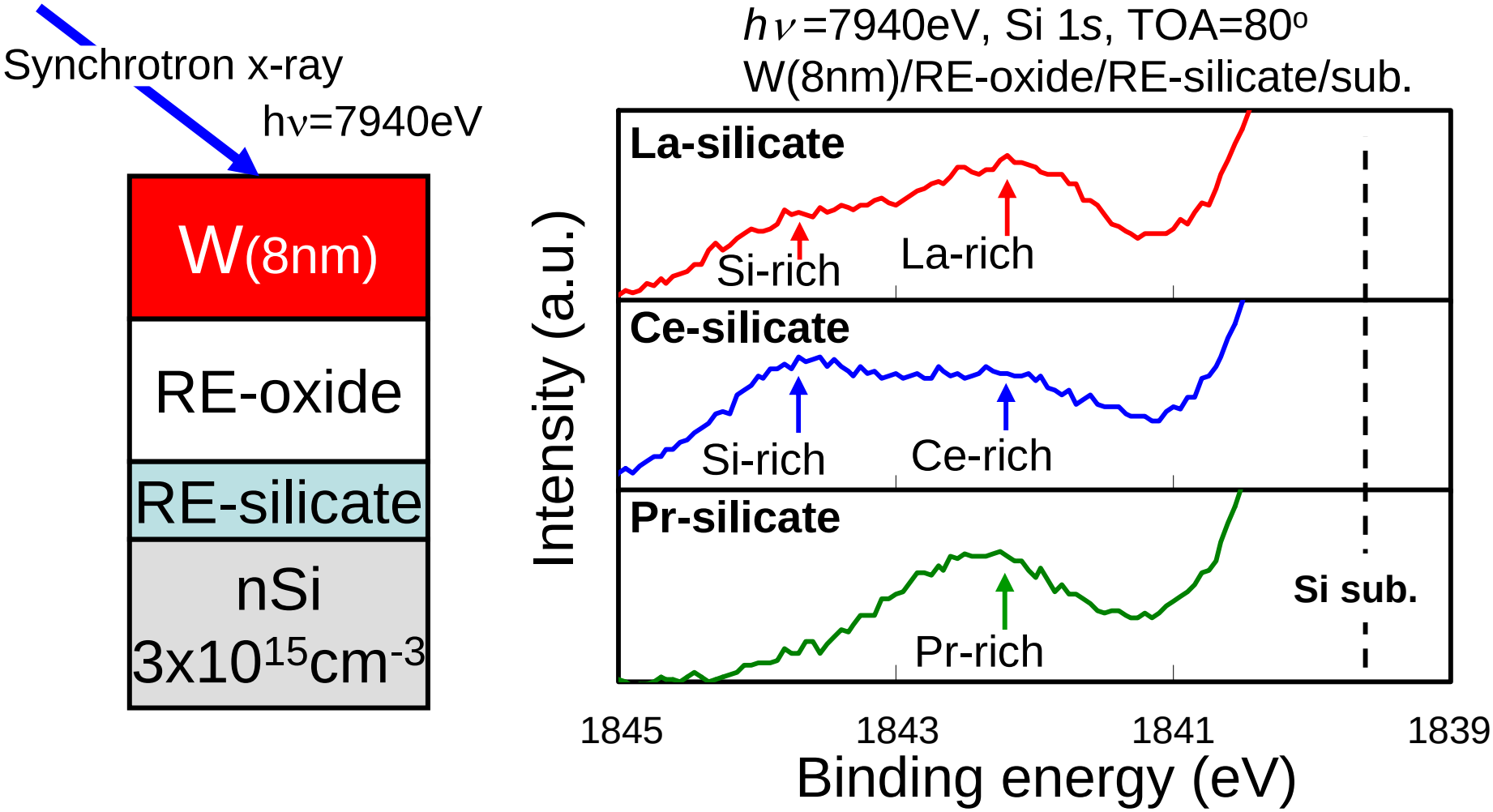
CV curves with La, Ce, Pr-silicates





Low D_{it} can be obtained with Ce-silicate

XPS measurement of La, Ce, Pr-silicates



Si-rich phase is formed with Ce-silicate

Strong correlation with D_{it} observed in CV

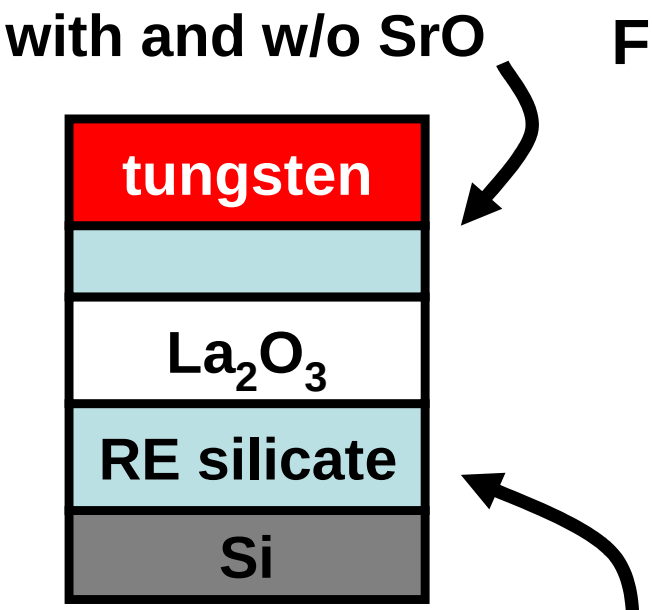
Material selection for EOT=0.5nm

Oxide	Dielectric constant	E_g (eV)
La_2O_3	~24	5.5
CeO_x	~32	3.2~3.7
PrO_x	~32	3.2~4.5
La-silicate	~9	~ 6.4
Ce-silicate	~21	~ 6.1
Pr-silicate	~10	~ 6.5

Ref: S Sathyamurthy, Nanotech 16 1960 (2005) HJ Osten et al., SSE 47 2161 (2003), A. Sakai, APL 85(22) 5322 (2004), O. Seifarth, J Vac Sci Tech B 27 271 (2009)

Combination of La_2O_3 (E_g=5.5eV) and Ce-silicate (k~21) can be a good candidate for scaled gate oxide

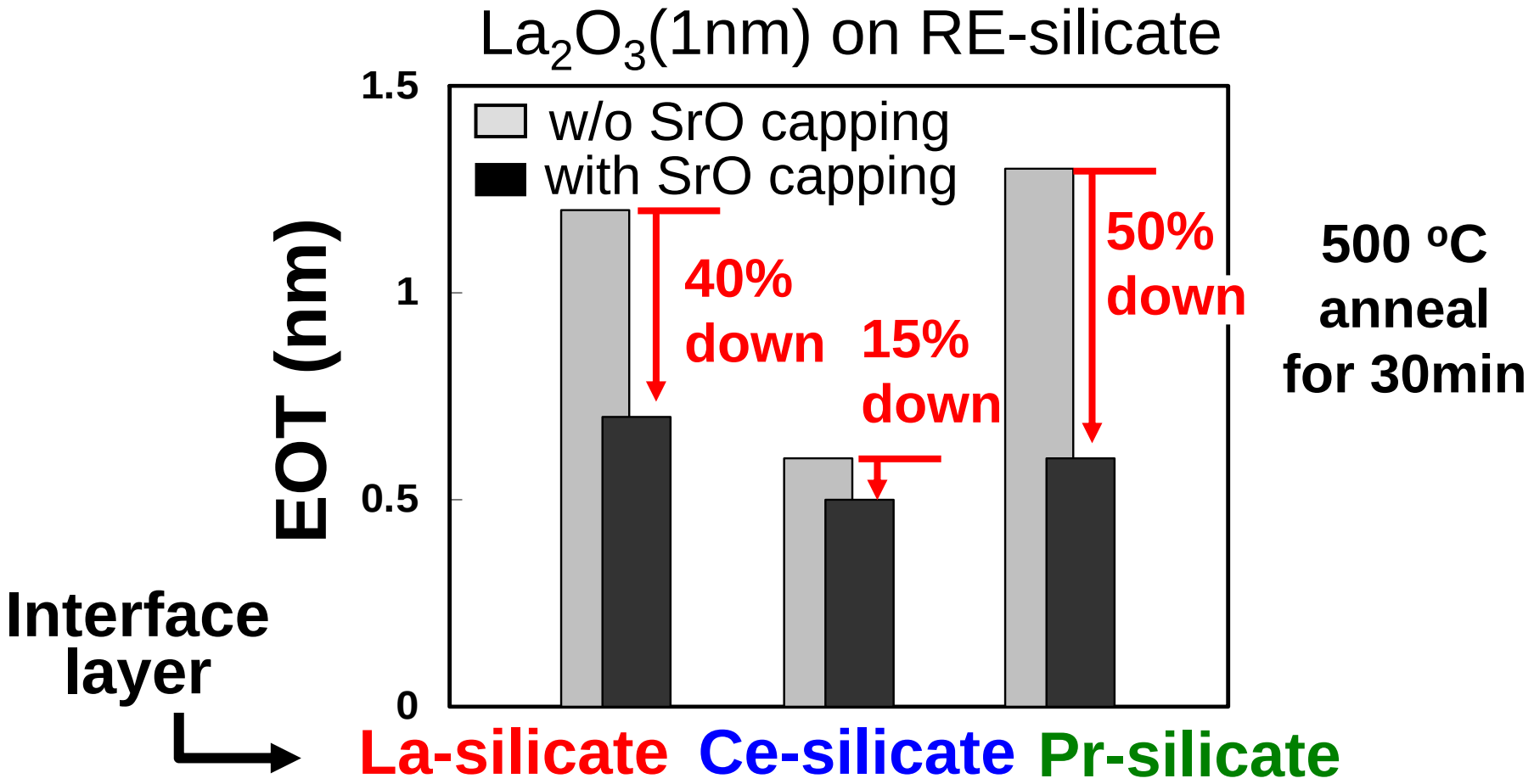
La_2O_3 with RE-silicate interfacial layer



Fabrication process

- HF-last Si wafer
- La_2O_3, CeO_x, PrO_x depo. (300^{o}C)
- La_2O_3 (1nm) deposition
- SrO (1nm) deposition (option)
- Sputter tungsten depo. (60nm)
- Gate lithography, etching
- Annealing at 500^{o}C for 30min

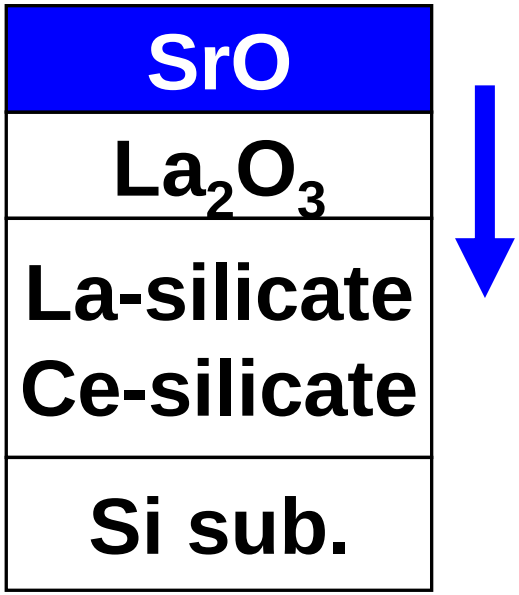
RE-silicate IL for EOT=0.5 nm

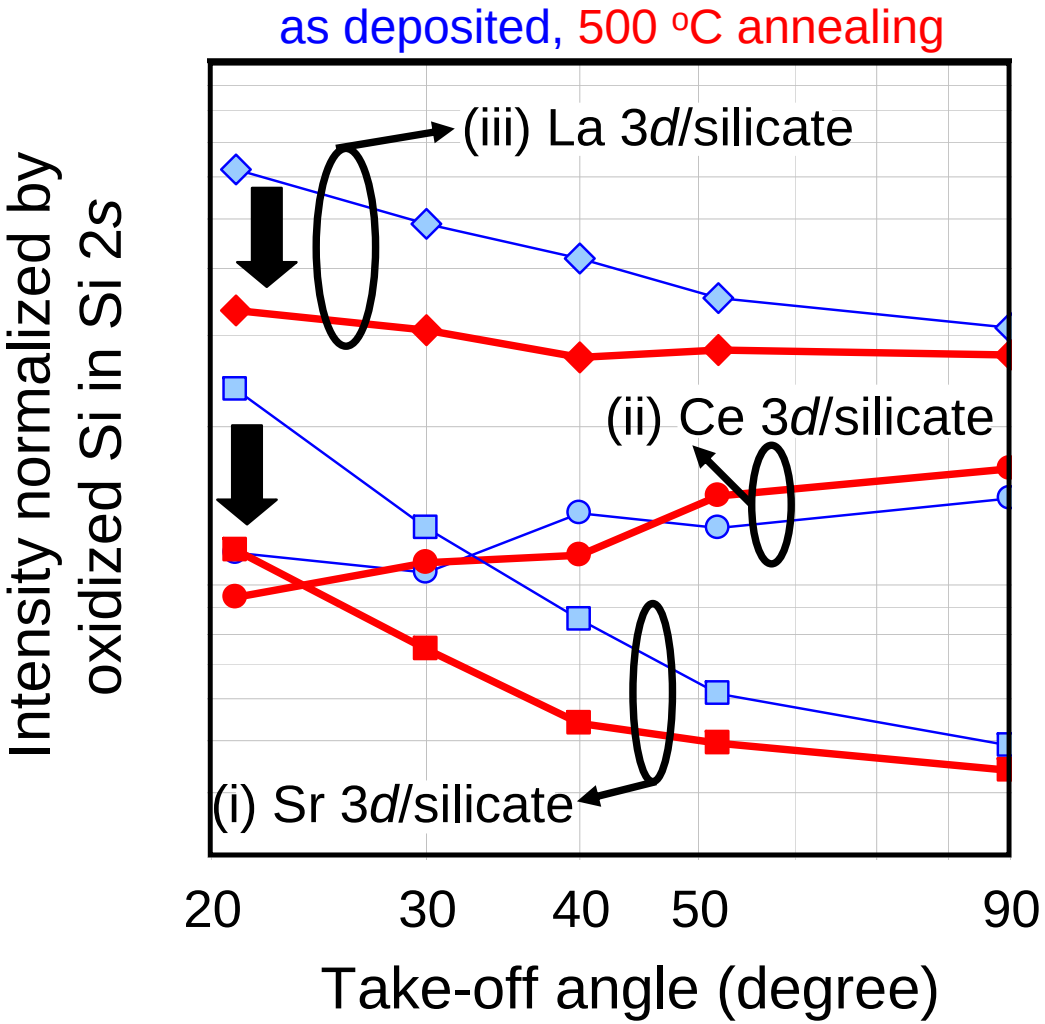


Further EOT reduction can be achieved with SrO capping

AR-XPS analysis of $SrO/La_2O_3/CeO_x/nSi$

analysis without metal layer



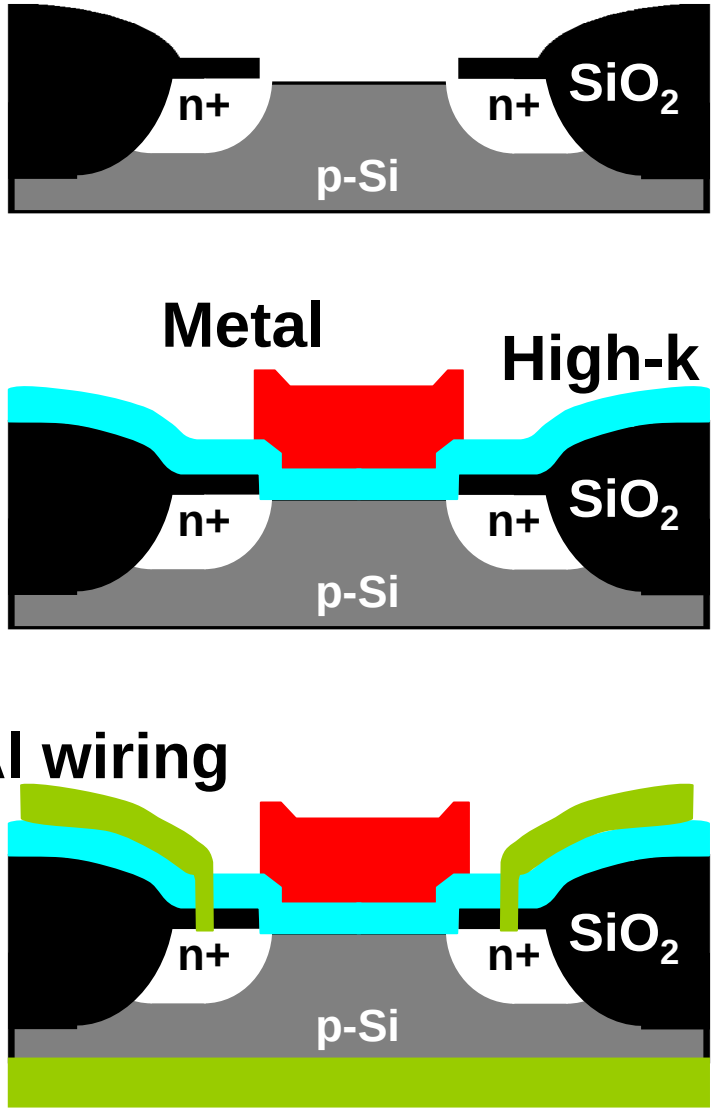


Sr atom diffusion to enhance the k-value of La-silicate

NFET characterization

La_2O_3/Ce-silicate nFET
SrO capped La_2O_3/Ce-silicate nFET

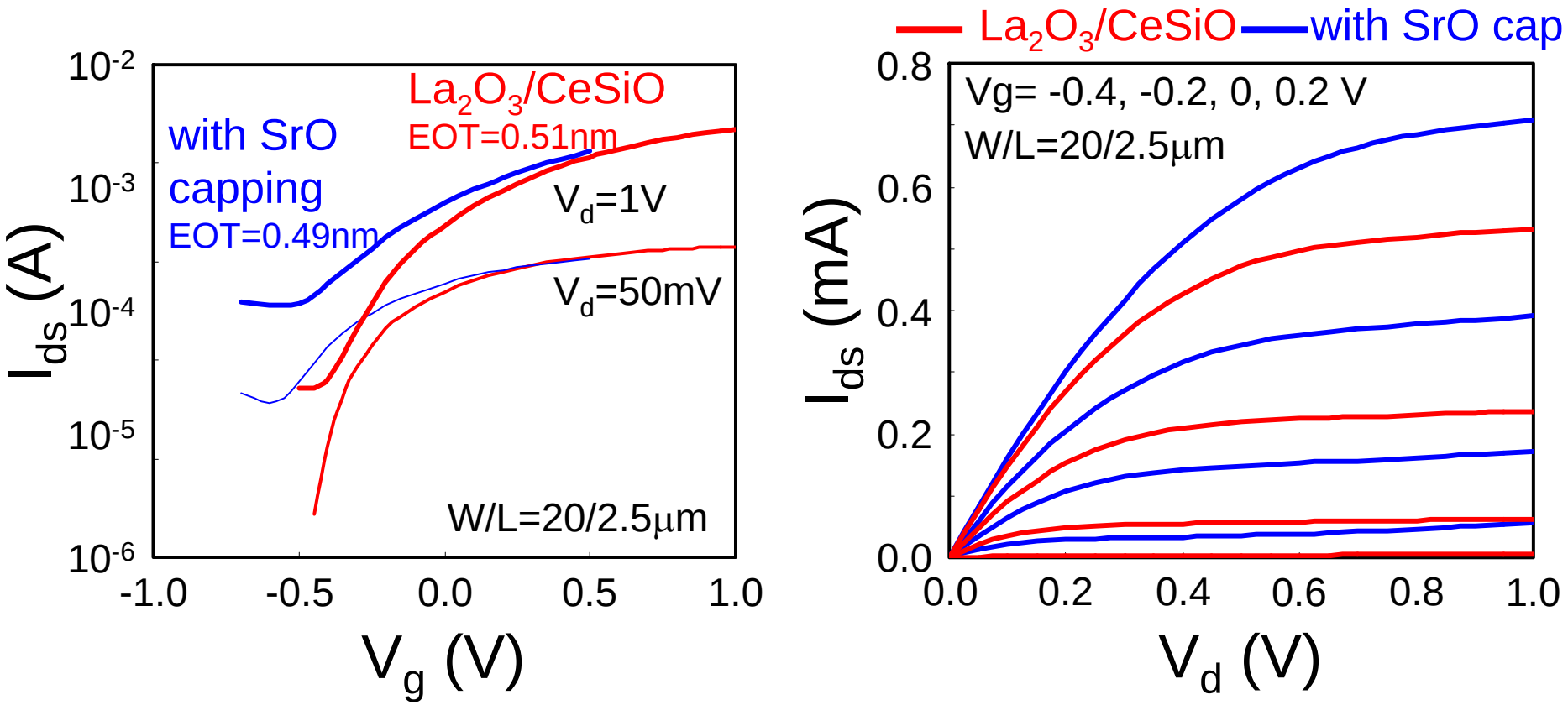
NFET fabrication process



Source/Drain pre-formed Substrate

- SPM, HF-last Treatment
- High-k e-beam evaporation HF-last Si @ 300°C under ~10^{-6} Pa
- Metal deposition by *in situ* RF-sputtering
- Metal dry etching
- Post Metallization Annealing (PMA)
- Contact hole formation
- Al wiring for S/D
- Back side contact formation (Al)

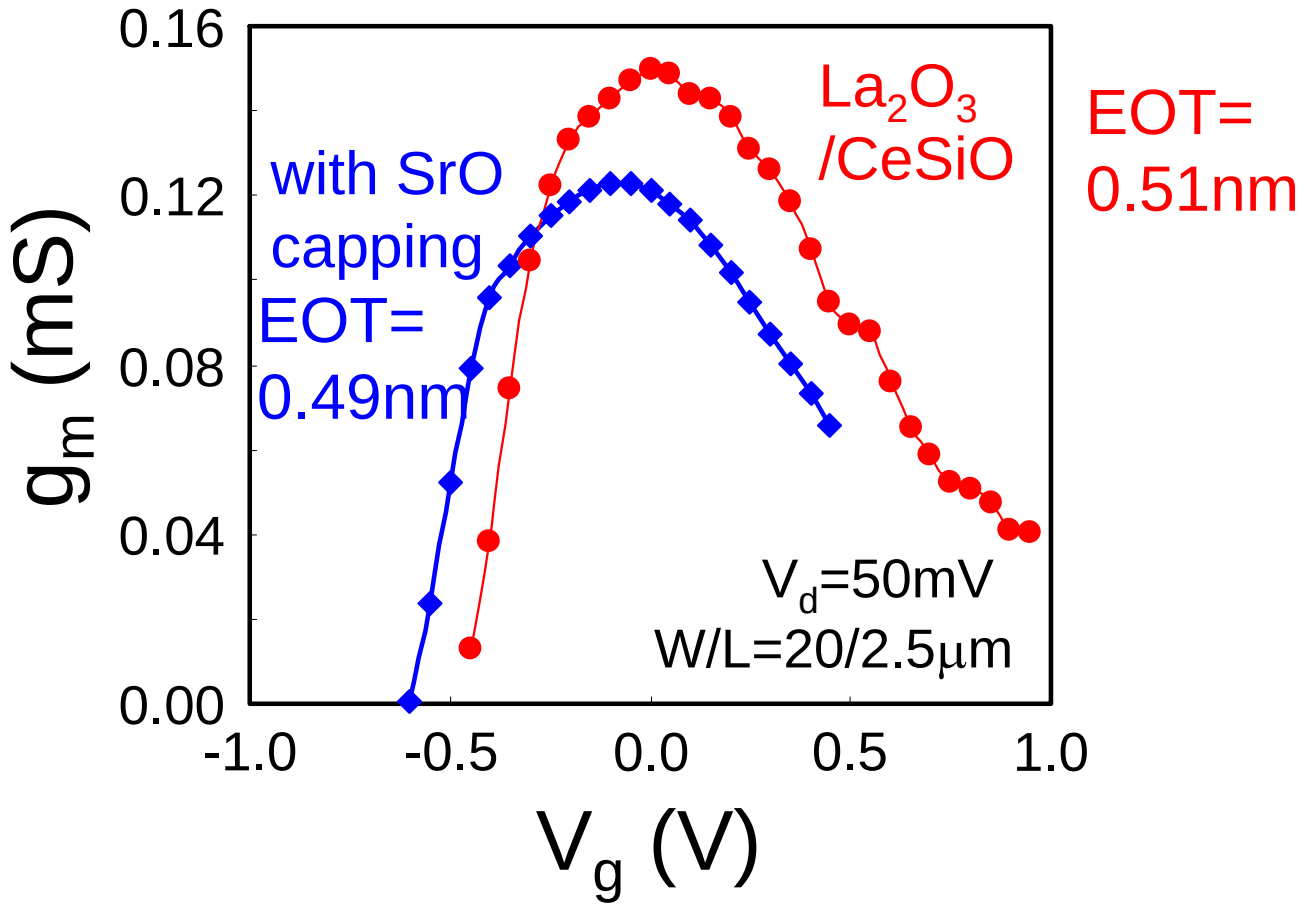
Output characteristics of nFET



Nice FET operations were confirmed with EOT<0.5nm

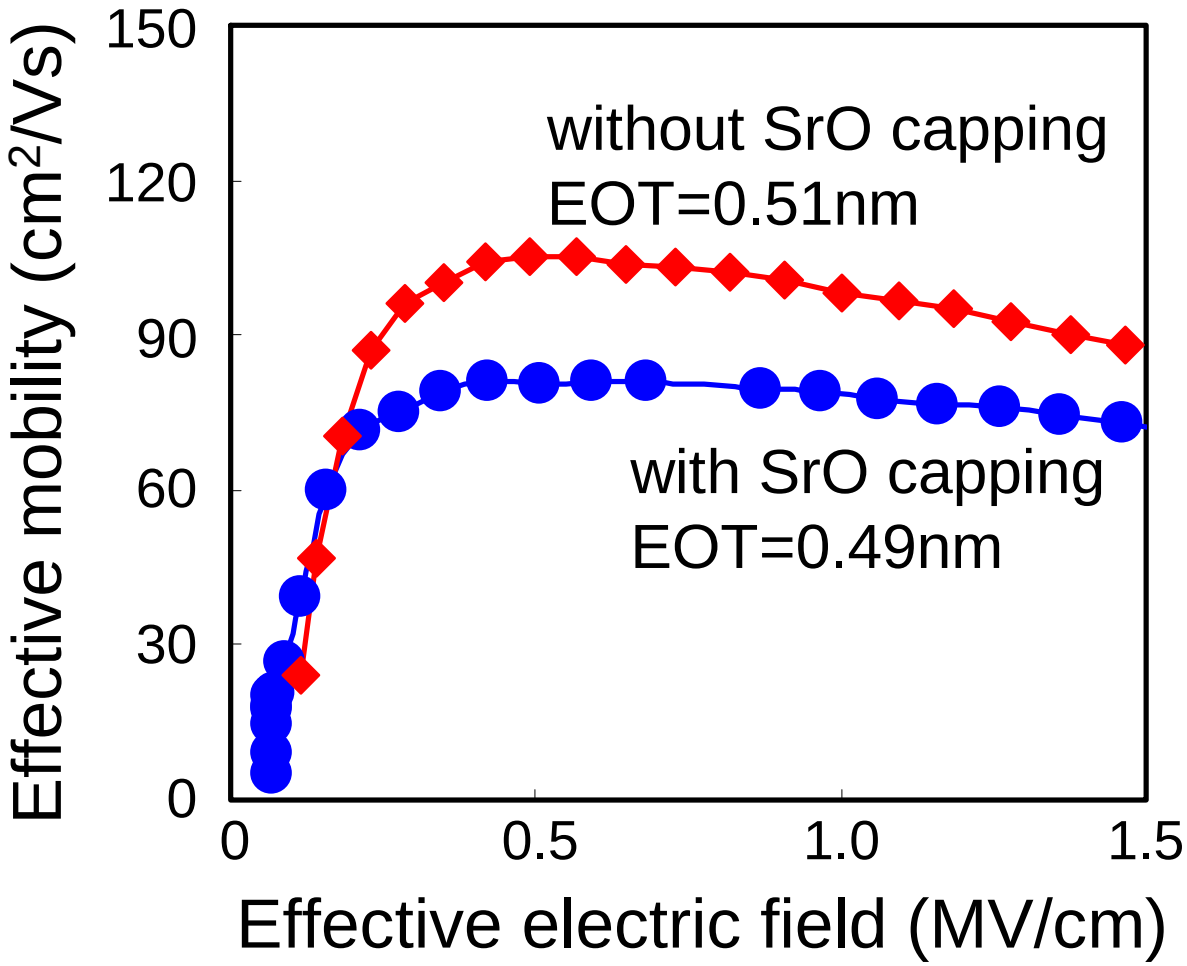
SrO capping shifts the V_{th} from -0.38 to -0.54 V

Transconductance of nFET



Reduction in g_m indicates the degradation in mobility

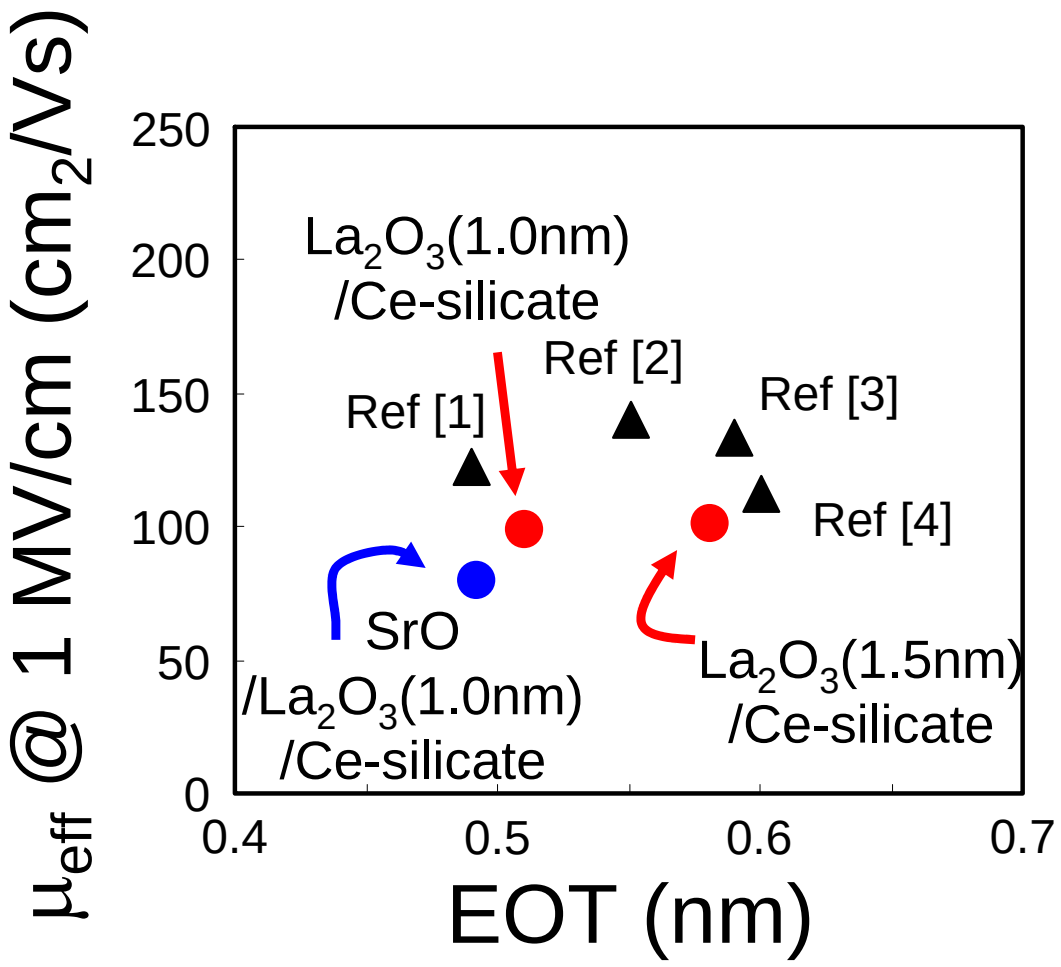
Effective mobility with SrO capping



Degraded mobility was observed with SrO capping

Possibly due to Sr atoms diffusion down to Si interface

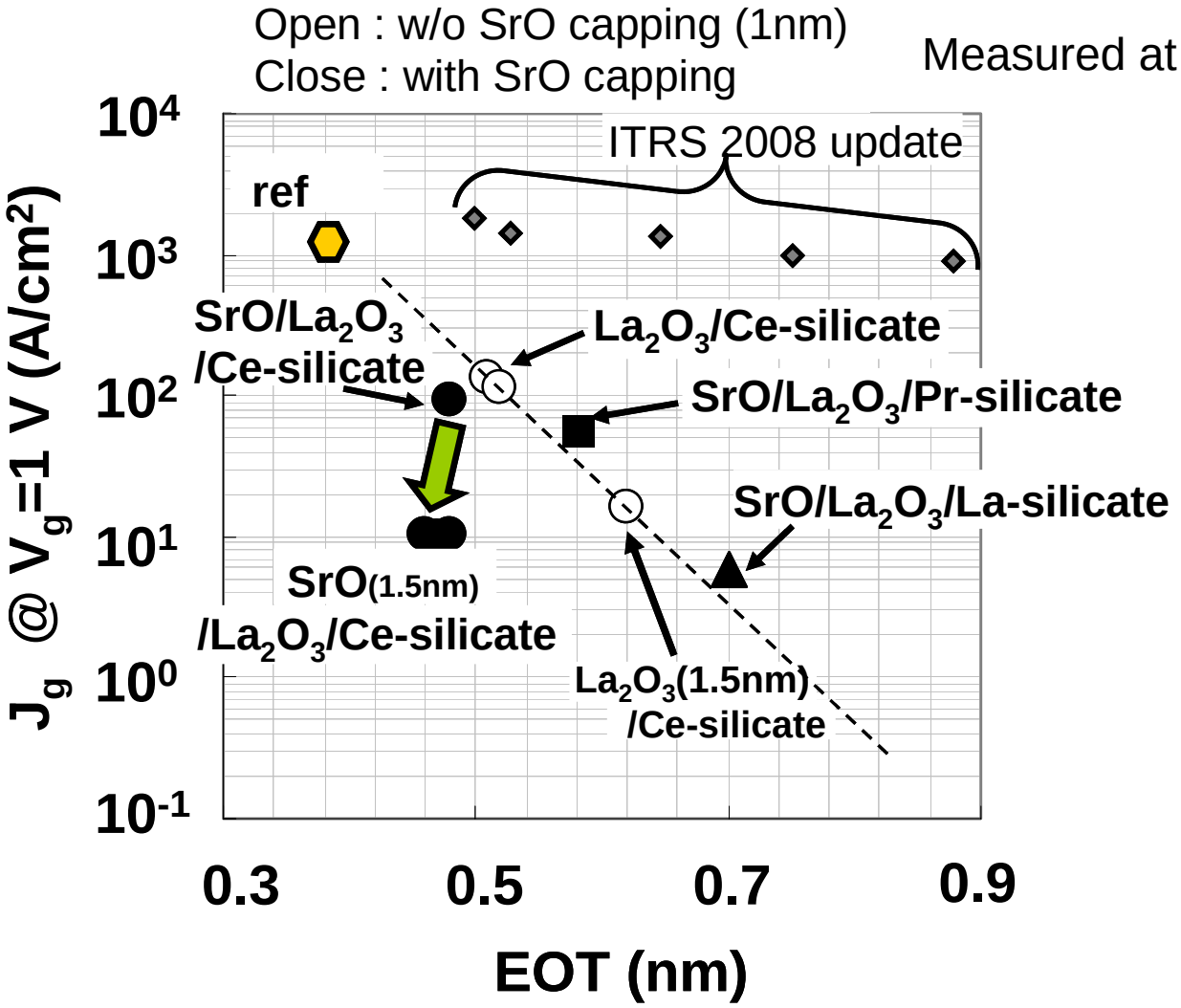
Summary of high field μ_{eff} on EOT



[1] M. Takahashi, IEDM 523 (2007)
[2] K. Choi, VLSI symp tech 138 (2009)
[3] J. Huang, VLSI symp tech 34 (2009)
[4] A. Ogawa, MEE 84 1861 (2007)

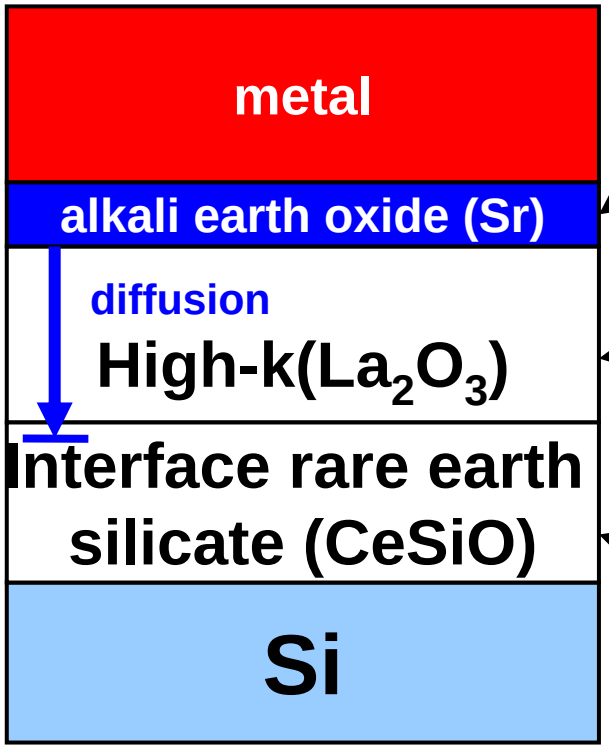
Our data follows the mobility trend in scaled EOT

Gate leakage current performance



SrO capping can reduce the gate leakage current

A proposed guideline for material selection in EOT=0.5nm



Suppression of fixed charge generation
Careful process control for diffusion

High k-value and wide E_g
Low fixed charge density by SrO

High dielectric constant with wide E_g
High diffusion barrier for Sr atoms
Low D_{it} should be achieved

Conclusions

- Ce-silicate interfacial layer is suitable for scaled gate dielectric

  $k\sim20$, E_g=6.1 eV, $D_{it}\sim10^{11}$ cm^{-2}/eV

- An EOT=0.51 nm can be obtained with by the combination of La_2O_3/Ce-silicate

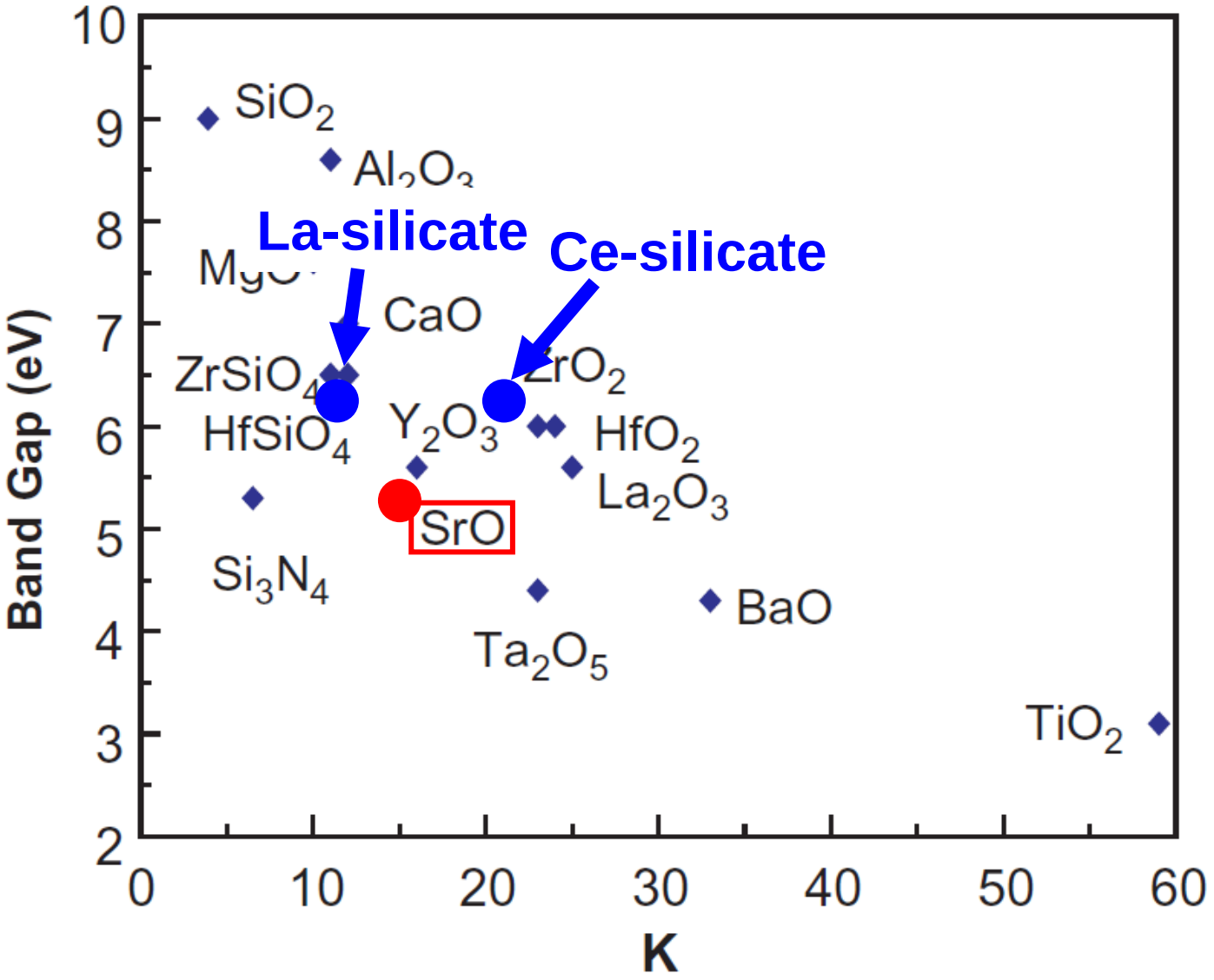
- SrO capping can further reduce the EOT at the cost of μ_{eff}

- A guideline for material selection for EOT scaling below 0.5nm is proposed

Acknowledgment

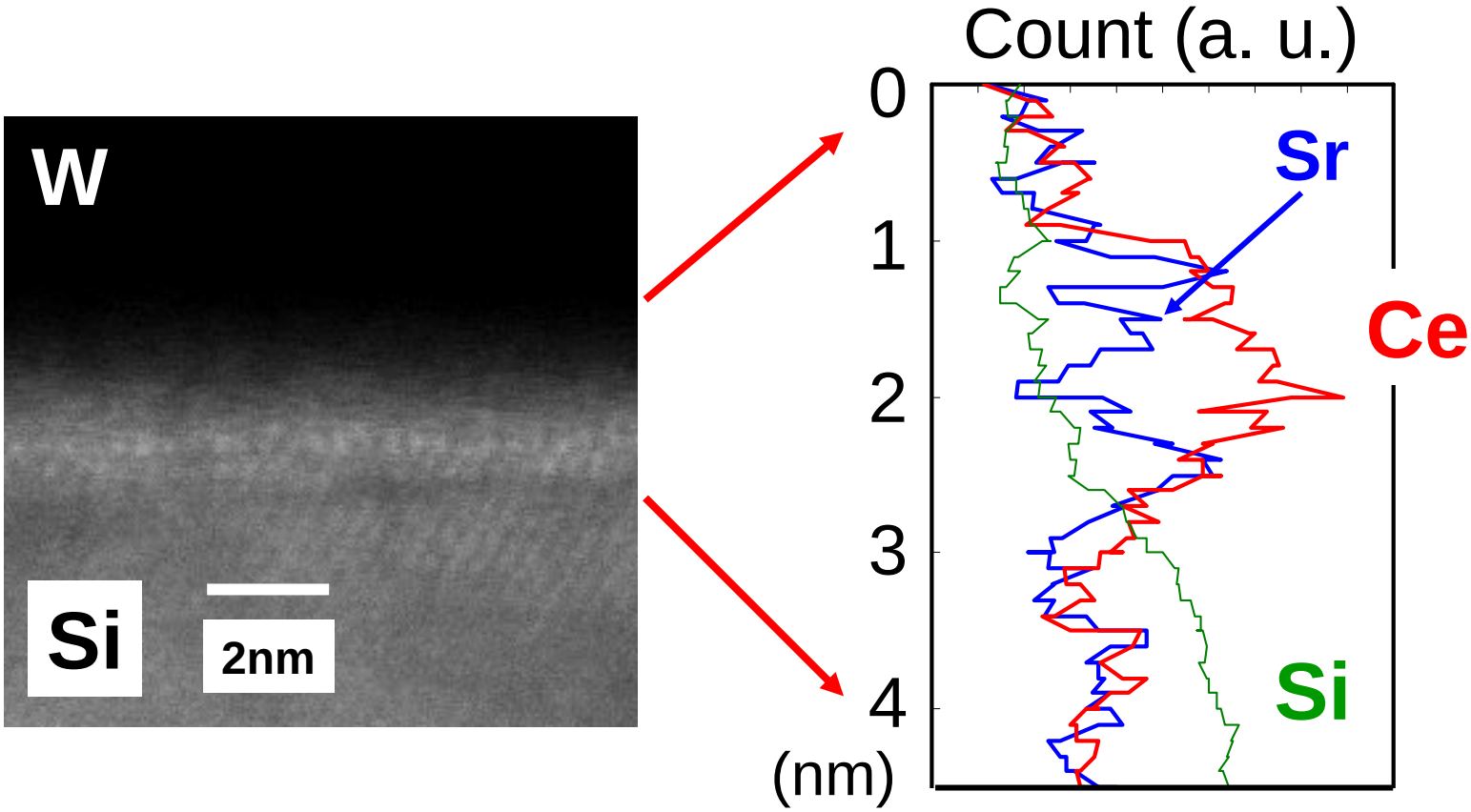
This work was supported by NEDO.

The synchrotron radiation experiments were performed at the BL47XU in the SPring-8 with the approval of the Japan Synchrotron Radiation Research Institute (JASRI) (Proposal No. 2007A0005).



J. Robertson, Solid-State Electronics 49 (2005) 283-293

TEM image of W/SrO(1nm)/CeO_x(1nm)/Si



The presence of Sr atoms are confirmed in Ce-silicate layer