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Towards Modeling the Effects of Lightning Injection on Power MOSFETs

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ABSTRACT

Power electronics are widely used in critical roles in modern day aircrafts and hence their health management is of great interest. An important part of prognostics and health management of these devices is understanding the effect of high-stress events such as lightning and how they affect their aging. In this paper we present our study and analysis of lightning injection experiments with power MOSFETs in their ON state. We show the different kind of damages that can be caused by such events and analyze their effects on device performance parameters. In addition, we present a simple yet effective modeling technique that can model the degradation in these devices. Such models will play a valuable role in understanding the behavior of these damaged devices when operated under normal conditions later and subsequently in prognosis of their remaining useful life.We present our results on the performance of this modeling and the scope within which they can be utilized for accurate estimation of device damage.

1. INTRODUCTION

Power electronics play a very important role in a wide range of applications varying from avionics to modern day cars. These devices are mainly used in high power switching circuits present in a wide array of electronic functions on board such as vehicle controls, communications, navigation, and radar systems as well as drives for electric motors that power systems ranging from actuatorsto electric vehicles. Understanding the behavior of these devices as they age is critical for ensuring operational safety and preventing catastrophic failures. In addition, most of these devices are prone to damage from high-stress events such as lightning and radiation. These events – though may not cause immediate failure – can significantly degrade the health of the device and hence its performance, ultimately resulting in reduced lifetime. Thus, it is imperative to study and understand the effects of these high stress events on power electronic components.

Study of the effects of radiation on these devices, are an active topic of research. However, lightning related events are of great concern in the aerospace domain. Commercial transport airplanes are typically struck by lightning once every 1000 to 20,000 flight hours (SAE, 2005; Clark, 2004) where voltage and current levels can reach as high as 30,000kV and 500kA respectively. Though, considerable shielding is provided to prevent catastrophic failures, in many instances significantly high surges can still reach individual components. In many cases, these surges may not cause the device to become completely non-functional, rather it may cause deviations in its ideal behavior. Such latent damage is of particular concern, since they may not be severe enough to be detected during normal operation, but would ultimatley lead to unexpected behavior and early failures. The effects of lightning events have gained even more prominence of late due to the gradual shift towards composite structures based body in modern aircrafts. Such structures are considered more prone to damage due to lightning and thunderstorm. Thus, understanding the effects of lightning surges on these devices is crucial for effective health management of them and their enclosing systems.

In this paper, we present our study and analysis of lightning injection on power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices which form an important subset of power semiconductor devices currently used in the industry. In a previous work, we had presented our studies on the effects of various lightning waveform injections on these devices when they were not turned ON (Celaya et al., 2009). In this paper, we extend this work to power MOSFETs in their conducting state, i.e., they are powered ON. In addition to presenting results and analysis of the effects of the lightning waveform injections, we also present an initial framework for modeling the effects of such high energy injections. Specifically, this paper makes the following contributions:

- An experimental framework for injection of lightning waveforms into power MOSFET devices in their powered ON state

- A framework for characterization of the effects on the devices after such high energy injections by performance parameter monitoring before and after injection
- Analysis of the effects on the devices, based on their performance parameters
- Development of initial simplified physical model for the degraded devices that include model parameter estimations

The remaining sections are arranged as follows. In section 2, we present a brief discussion of related work in this area. We then present the experimental setup and results of the lightning waveform injections in section 3. In section 4, we first present a brief overview of power MOSFETs and their models followed by modeling of damaged devices. In section 5, we present our modeling results followed by a concluding discussion in section 6.

2. BACKGROUND

Prognostics and health management for electronic components is a relatively new research field which is fast gaining in importance due to the omnipresence of these components. Most of the past as well as existing efforts approach the estimation of the component health from the perspective of reliability-based studies. However, of late, focus has been made on developing accelerated aging methodologies for these components by means of electrical, thermal or mechanical overstress (Lall et al., 2008; Saha et al., 2009; Sonnenfeld et al., 2008). Though, such aging methodologies would greatly aid in understanding the behavior of the device as they undergo regular operation, a critical aspect of their prognostics and health management is understanding the effects on electronic devices following single very-high stress events. Example of such events include lightning, electrostatic discharge, radiation and so on. Such events can cause catastrophic damage to the device rendering it inoperable. However, the issue of greater concern is if any latent damage is incurred by the device. Such damages would not be detected during normal maintenance or nominal operation – since they may have not affected the device characteristics significantly – but can lead to early failures of these devices. Thus, understanding the effects of such events as well as their influence on future aging is of vital importance for complete health management.

Effects of radiation on power electronics have been widely studied (Selva et al., 2003; Felix et al., 2005) which mainly focus on the device model undergoing radiation damage. Electro-static discharge (ESD) can cause significant damage to power electronics and are being currently analyzed (Wysocki, Vashchenko, Celaya, Saha, & Goebel, 2009). Most prior studies and analysis of lightning effects on semiconductors are devoted to the protection of equipment from lightning, including innovative surge protection circuitry for semiconductor devices (Satoh & Shimoda, 1996). Understanding lightning injection on passive devices (Tasca, 1976) and few semiconductor devices have been explored (Wunsch & Bell, 1968; Jeong, 2005). However, they are not comprehensive and do not conisder power semiconductors. Thus, research efforts on understanding the effects of lightning on power electronic devices, specially on their aging, are greatly lacking.

Lightning events are commonly encountered in aircrafts and the potential damage caused by their injection are of great concern; more so as we increasingly move towards composite aircrafts. In our previous analysis, we provided insight into the possible effects of lightning events on power MOSFET devices which have not been turned ON (Celaya et al., 2009). The current work, focuses on devices in their ON state. We also explore simple models that can capture the characteristics of lightning-affected device.

3. LIGHTNING INJECTION EXPERIMENTS

Power MOSFETs are a common semiconductor device used in high power switching applications. As mentioned earlier, they are susceptible to damage from lightning and an issue of great concern is the latent damage caused by such a high-stress event. In order to prevent unexpected failures, it is important to understand the effects of lightning injections on these devices; in particular which parameters and how they are affected. In this section, we present our experiments on injection of lightning waveforms followed by an analysis of their effects on the device. In order to estimate the extent of the damage caused by the injections, device parameter characterization tests both before and after the injection was performed. Analysis of these parameters, provide insight into the type and level of damage caused to the device which can be further used to create models for the damaged devices. These models can then be used for estimating the current and expected future health of the affected devices.

3.1 Experimental Setup

In a practical aircraft lightning strike event, an electronic component is not expected to be hit directly. The lightning waveform reaches an electronic component after passing through the various shielding provided in the aircraft. Thus, an appropriate propagation model is required to estimate the lightning waveforms that actually reach a given component. Standards that describe such waveforms are available for aircrafts which provide descriptions of waveform types representative of real situations along with their expected intensity levels. In our experiments, the lightning waveform reference standard described in RTCA/DO-160E (RTCA/DO-160E, 2004) was used. RTCA/DO-160E is intended for establishing flight worthiness tests of airborne equipment. However, the waveforms described in this standard apply to assembled electronic systems rather than individual components. Therefore, the test setup described in the standard was modified accordingly.

The DO-160E lightning- induced voltage Waveform 4 ($6.4\mu s$-Rise Double Exponential) was selected for these tests as shown in figure 1. DO-160E recommends Waveform 4 for airborne equipment that may be subjected to lightning-induced magnetic fields coupled onto their wiring. For a discussion on the various other waveforms and their suitability for such experiments please refer to (Celaya et al., 2009). Since in this experiment, pin injecting of lightning transients was performed on a MOSFET in its ON state, special considerations for the biasing circuit is required as listed below:

- Protection of biasing circuitry from the lightning transient.

Table 1: Applied lightning injection voltage levels

WF	Pin Config.	V_{GS}	H	M	L
WF4+	G-S	8V	65V	59V	52V
WF4-	G-S	8V	68V	61V	54V
WF4+	D-S	8V	265V	239V	212V
WF4-	D-S	8V	1360V	1292V	1224V
WF4+	G-S	16V	57V	51V	46V
WF4-	G-S	16V	80V	72V	64V
WF4+	D-S	16V	320V	288V	256V
WF4-	D-S	16V	1210V	1150V	1089V

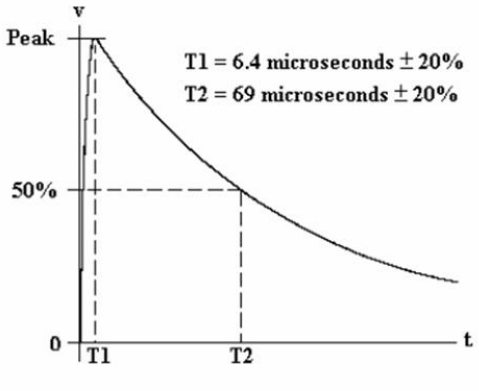

Figure 1: RTCA/DO-160E Section 22 Voltage Waveform 4 (modified from (RTCA/DO-160E, 2004))

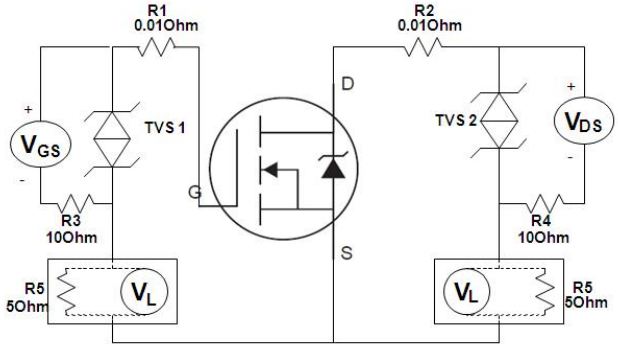

Figure 2: Lightning pin injection test setup circuit

- Protection of the MOSFET from excessive current applied by biasing circuitry.
- Protection of the Lightning Generator from excessive current applied by biasing circuitry.
- Assurance that biasing circuitry does not corrupt the MOSFET test results by modifying the lightning transient waveform.

The resulting circuit configuration that satisfies the above considerations and hence the one used in our experiments is shown in figure 2. In this circuit, V_{DS} and V_{GS} function to bias the MOSFET drain-source (D-S) and gate-source (G-S) junctions such that the device is in the ON state as the lightning pin injected transient is applied. A Fischer Custom Communications (FCC) Transient Voltage Suppressor (TVS) was installed in parallel to both voltage sources. The TVS devices function to bypass the voltage sources when the lightning transient is applied (thereby protecting the voltage sources). Current Sense Resistors ($R1$ and $R2$) are provided at the drain and gate inputs to facilitate measurement of direct current, using a differential probe. Current-limiting resistors ($R3$ and $R4$) are in-line with V_{GS} and V_{DS} to limit the direct current through the G-S and D-S junctions, so as not to cause unnecessary heating to the MOSFET or excessive direct current through the lightning waveform generator.

All testing was conducted in the High Intensity Radiated Field (HIRF) Laboratory at NASA Langley Research Center. The HIRF Laboratory is equipped with generators for indirect lighting effects testing. The lightning transient was applied to either the G-S junction or the D-S junction, but not both simultaneously. The G-D pin-injection configuration was not tested because such a test would require significant additional effort to protect the lightning generator and power supplies in the event of a G-D short-circuit MOSFET failure mode. The MOSFET Source is usually referenced to ground, so the G-S and D-S junctions are more likely to provide a lightning transient path than the G-D junction. In order to implement the MOSFET test circuit with safe, repeatable hookups, and test port access for oscilloscope and DC voltmeters, and to allow the use of interchangeable components (i.e. TVS devices), a component testing biasing/lightning injection interface board was designed and fabricated.

Experiments with injection configurations on G-S, S-G (source-gate), D-S and S-D (source-drain) were performed with two different G-S bias. Multiple levels of injection waveform namely high (H), medium (M) and low (L) and multiple strokes (5, 10 and 20) were used. The voltage levels corresponding to the three different levels are further elaborated in table 1. In this table WF refers to the waveform and WF- refers to the waveform applied after reversing the leads of the device corresponding to WF+.

After the injection, characterization tests were performed on the injected devices to obtain an approximate

measurement of the damage incurred by the devices using a source measurement unit (SMU). The SMU used was a Keithley 2410 series. Specifically, the parameters that were tested are described below:

- Breakdown voltage $V_{BR(DS)}$: This gives the voltage level at which the drain-source path of the device starts conducting drain current given that the gate is not biased, and essentially measures the breakdown rating of the body diode. Thus, under normal operation, this current should be very low (in the μA range) since the drain-source path behaves like an open circuit when the gate-bias is 0. As the applied voltage V_{DS} increases it approaches the breakdown rating of the diode and significantly large current starts flowing through the drain.
- Leakage Current I_{DSS}: This is the current flowing from drain to source as the gate is shorted with the source (no gate bias) and represents the leakage current characteristics of the body diode.
- Threshold Voltage $V_{DS(thr)}$: This voltage refers to the minimum voltage required to bias the gate in order for the device to switch ON and allow drain current to flow. The SMU equipment provides a voltage sweep and measures the corresponding drain current till V_{GS} reaches a value where the drain current starts growing exponentially.

3.2 Results and Analysis

It was generally observed from the SMU analysis that for the S-D and S-G configurations, extremely high voltages were required to produce any significant damage. Similarly for the D-S configuration, high levels of injection (lower than that for S-D and S-G configurations) was required to observe any damage; in most cases for such high levels of injections the devices were completely destroyed. However, significant damage could be observed in many cases with much lower injection voltage for the G-S configuration. Thus, it is of more interest to analyze these cases as they are more susceptible to damage. A complete analysis of all the configurations is beyond the scope of this paper and we focus on the injections using G-S configurations only.

Table 2 shows the damage levels observed using the SMU for the injection at the gate. The normalized change in parameter values for the affected devices was calculated in order to estimate the effect of the different configurations. The mean values of the normalized parameter changes are also shown in the table 2.

For the G-S configuration, it was observed that the threshold voltage decreased with increase in the voltage level, gate bias, number of strokes and a combination of these factors. It was also observed that in the injection configuration with highest intensity and 20 strokes, a very high deviation occurred in the device behavior. Not only was significant leakage (I_{DSS}) observed, in many cases the breakdown characteristic was completely altered. This was observed for both gate bias voltage values of 8V and 16V. Figures 3, 4 and 5 show these damages for one such case. As observed from these characteristics, the devices have incurred very high damages and in most cases may not be used for further normal operation. However, for lower levels of intensity, such high levels of damage was not observed and as seen in table 2 only the threshold voltage decreased. Figure 6 shows the decrease in threshold voltage for such a device.

The decrease in threshold voltage reflects that as the intensity of the injection applied at the gate is increased, the oxide and the underlying silicon started accumulating damage which starts modifying the turn-on behavior. As this injection is further intensified, the gate-oxide starts to breakdown which can then lead to conductive paths within the oxide. Such conduction paths would create various sources of leakage currents leading to significantly non-ideal behavior of the device. In addition, the body of the device also undergoes very high stress due to the presence of the high electric field. Damage to the body gets reflected in our characterization curves through the breakdown voltage and leakage current characteristics (figures 4 and 5).

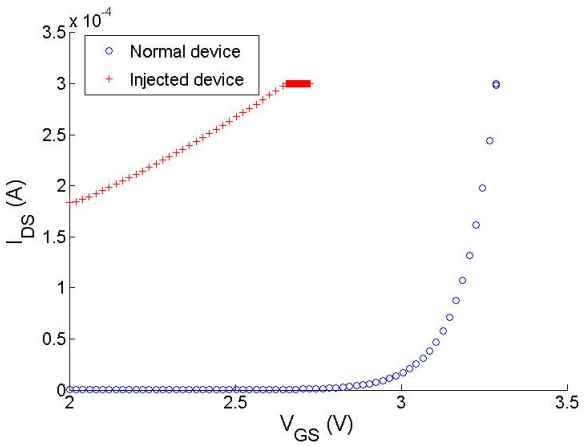

Figure 3: Turn-on characterization for lightning injected device in GS configuration, injection intensity H, strokes = 20 and gate bias = 8V

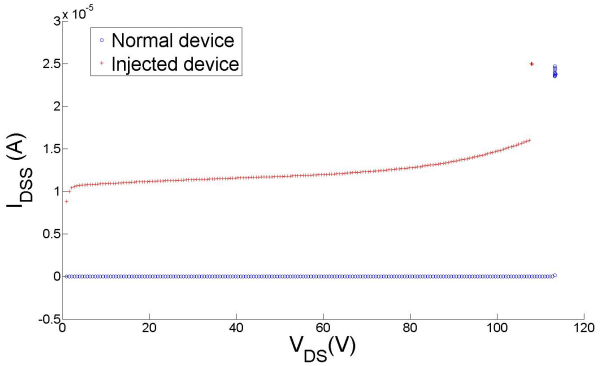

Figure 4: Leakage characterization for lightning injected device in GS configuration, injection intensity H, strokes = 20 and gate bias = 8V

4. DAMAGE MODELING

As observed in section 3.2, there was significant deviation in the turn-on characteristic after the devices were

Table 2: Summary of change in device characterization after lightning waveform injection

Pin Config	Injection Intensity Level	Gate bias	Strokes	Results
G-S	H	8V	5	Mean decrease in $V_{GS(thr)}$ by 0.0243V
G-S	H	8V	10	Mean decrease in $V_{GS(thr)}$ by 0.0647V
G-S	H	8V	20	Devices were significantly damaged with high leakage
G-S	M	16V	All	Mean decrease in $V_{GS(thr)}$ by 0.0095V
G-S	H	16V	5	Mean decrease in $V_{GS(thr)}$ by 0.0361V
G-S	H	16V	10	Mean decrease in $V_{GS(thr)}$ by 0.0847V
G-S	H	16V	20	Devices were significantly damaged with high leakage

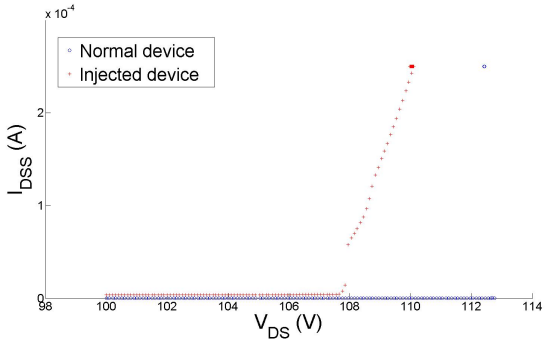

Figure 5: Breakdown characterization for lightning injected device in GS configuration, injection intensity H, strokes = 20 and gate bias = 8V

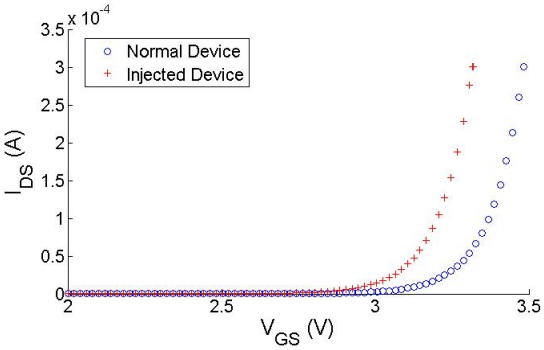

Figure 6: Turn characterization for lightning injected device in GS configuration, injection intensity M, strokes = 10 and gate bias = 8V

injected with lightning voltage pulses in the G-S configuration. Such changes are expected to affect the switching behavior of the device, since with a lower threshold voltage the device would take less gate voltage to turn ON and hence the device would switch ON much earlier. In order to understand how such an injected device may behave in operation in future i.e., predict the future switching behavior, it is important to model these changes. Our approach to capture these changes in performance is by creating a simplified model of the device and then modifying the various parameters of the model based on the change in characteristics after injection. In order to do this, we first create a simplified model of the normal device and then based on a set of experiments, determine the modified model for the injected device.

In the following subsections, we first provide a brief overview of the device structure followed by a discussion on their modeling. We next focus on the model parameter characterizing experiments and how they can be utilized to determine the modified model of the injected device. This model can then be used in conjunction with other model-based or data-driven prognostic techniques to predict the behavior and health of the device when in operation. Note, as mentioned in earlier section 3.2, we mainly focus on damage modeling for the G-S configuration for lightning injection. For the high-level intensity injection at the gate with 20 strokes, the device characteristics are significantly altered and hence would require a more complex model to capture all the parameter deviances and is beyond the scope of this paper. However, development of this model is an important direction for our future work.

4.1 Power MOSFET

A power MOSFET is a special MOSFET that is designed to handle large amounts of power. However, most power MOSFETs differ from normal MOSFETs in their structures, the main difference being in the fact that most power MOSFETs have a vertical structure as against the planar structure of normal MOSFETs. Thus, the main current flow is in the vertical direction in a power MOSFET. A typical power MOSFET structure is shown in figure 7. From this figure, it may be observed that the drain and source do not exist next to the gate, rather the drain lead is at the bottom of the structure. Such a structure provides much higher voltage rating.

All semiconductor devices contain parasitic components intrinsic to the physical design of the device. In power MOSFETs, the main components include resistors associated with material resistivity, a body diode formed at the junction of p+ body and the n- epitaxial layer, and an NPN BJT (bi-polar junction transistor) formed where the n+ source contact is diffused. Figure 8 shows the details of these parasitic components. The prominent parasitic capacitor components include the gate-source capacitance (C_{gs}), the drain-source capacitance (C_{ds}) and the gate-drain capacitance (C_{gd}) as shown in figure 9. C_{gs} is the capacitance due to the overlap of the source and the channel regions by the polysil-

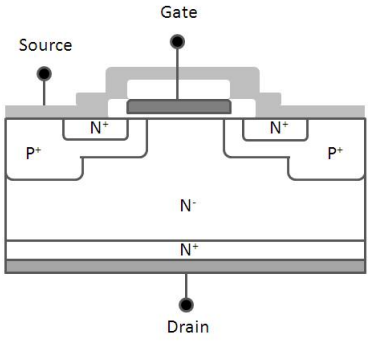

Figure 7: Structure of a typical power MOSFET

icon gate and varies insignificantly with applied voltage. It is considered to be a serial combination of the following capacitances:

- C_o: The capacitance between the gate and source metal
- C_{N+}: The capacitance between the gate and the n+ source diffusion region
- C_P: The capacitance between the gate and p-body. It is affected by the gate, the drain voltage and the channel length and is the only component that is influenced by the change of the drain voltage (V_{DS}) among other C_{gs} components. However, the change of C_{gs} due to $V_{DS}$is very small.

C_{gd} consists of two parts, the first (C_{gd1}) is the capacitance associated with the overlap of the polysilicon gate and the silicon underneath while the second part (C_{gd2}) is the capacitance associated with the depletion region immediately under the gate and varies as a nonlinear function of voltage and is also called the Miller capacitance. Finally, (C_{ds}), the capacitance associated with the body-drift diode, varies inversely with the square root of the drain-source bias. The total input capacitance C_{iss} is given by the following:

$$C_{iss} = C_{gs} + C_{gd1} \tag{1}$$

Other parasitic elements include the resistances that contribute to the ON resistance of the device or R_{DSon} which include the channel resistance, source diffusion resistance, substrate resistance and so on. However, as we shall see in the later sections, the only parasitic elements that are of interest to us for analysis purposes in this paper are the parasitic capacitances.

The turn-on of the BJT is undesirable since it leads to large current sinking in the device leading to its failure. Failure due to the parasitic BJT turn-on is a common mode of failure for the power MOSFET devices. The other parasitic component that plays a significant role in the functioning of this device is the body diode. This body diode may often lead to avalanche breakdown due to a sudden spike in voltage. However, most manufacturers provide specifications for this behavior which include characteristics of the device under single-shot as well as repetitive avalanche ruggedness tests.

From, the above discussion, one may observe that a complete model for the power MOSFET with multiple parasitic components would be complex to analyze.

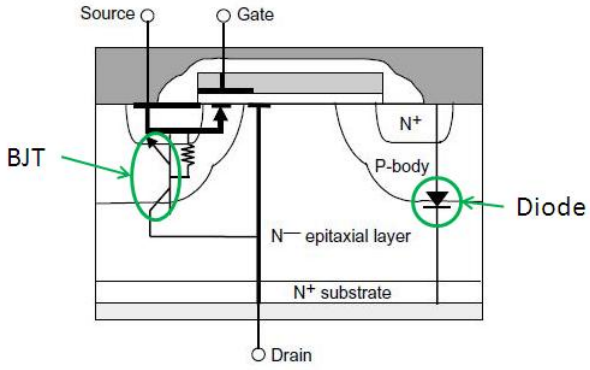

Figure 8: The power MOSFET vertical structure showing the parasitic BJT and Diode (modified from (Oh, n.d.))

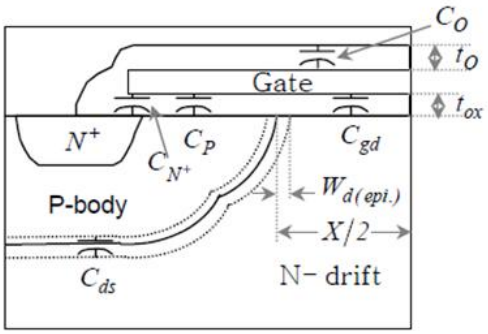

Figure 9: The power MOSFET vertical structure showing the parasitic capacitances (modified from (Oh, n.d.))

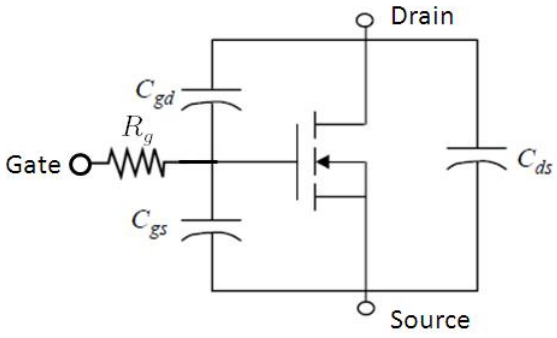

Figure 10: Simplified power MOSFET equivalent model (modified from (Oh, n.d.))

However, in order to analyze the effects of the lightning injection that we have observed in section 3.2, such a complex model is not required. Since, in this paper we focus more on modeling for the G-S damage, it allows us to ignore many of these parasitic components. Specifically, since threshold voltage was observed to be significantly affected, we focus on the gate switching behavior only i.e., the power MOSFET turn-on characteristic. The simplified model that captures the effects of the parasitic components on the switching is shown in figure 10, where the capacitances are as defined earlier and R_g is the line resistance seen at the gate. From this figure, it may be observed that before the device can turn ON, multiple capacitors need to be charged.

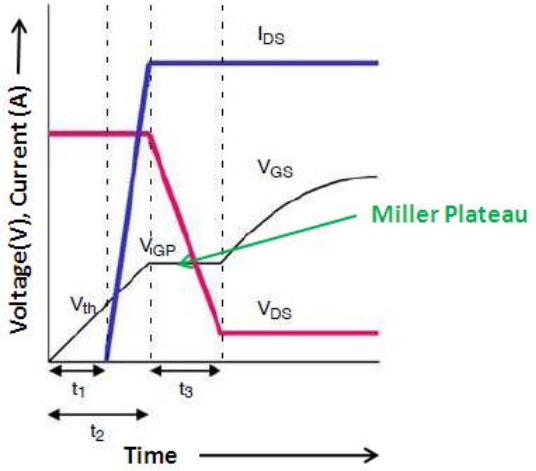

Figure 11: Simplified power MOSFET turn-on transient behavior (modified from (Brown, n.d.))

The idealized turn-on transient behavior corresponding to the simplified model in figure 10 is shown in figure 11. In this figure, the time period t_1 represents the time required for the gate voltage V_{GS} to reach the threshold voltage ($V_{GS(thr)}$). During this time, the gate current I_G charges the capacitors C_{gs} and C_{gd1}. Though, in figure 11, this charging is represented linearly, in practice this is an exponential rise with the following time constant:

$$\tau_1 = (C_{gs} + C_{gd1}) \times R_g \quad (2)$$

While the time period t_1 is given by the following equation:

$$t_1 = R_g \times (C_{gs} + C_{gd1}) \ln[1/(1 - V_{GS(thr)}/V_{GG})] \quad (3)$$

where V_{GG} is the applied voltage at the gate.

Till V_{GS} reaches $V_{GS(thr)}$, the device is still in its OFF state and V_{DS} is held at the supplied voltage at the drain (V_{DD}). The next time period between t_2 and t_1, represents the time when the threshold voltage has been crossed and hence the drain current I_{DS} has started to increase. However, V_{DS} does not change significantly and the device still charges the capacitors C_{gs} and C_{gd1}. Next in the time period t_3, the device is in the active region and as V_{DS} starts decreasing, the Miller capacitance C_{gd2} starts charging. This region is known as the Miller plateau and should show a slope of zero or near-zero. In many cases, the slope may be non-zero which reflects that fact that some the gate current I_G is being used to drive C_{gs} as well. The time constant is the same as shown in equation 2, while the value of the time period t_2 is given as follows:

$$t_2 = R_g \times (C_{gs} + C_{gd1}) \ln[1/(1 - V_{GP}/V_{GG})] \quad (4)$$

where V_{GP} is the value of the gate voltage at the Miller plateau region.

During the time period t_3, only the Miller capacitance is charged which varies with V_{DS} and is given by

$$t_3 = [(V_{DS(off)} - V_F) \times R_g \times C_{gd2}]/(V_{GG} - V_{GP}) \quad (5)$$

where V_F is the value of V_{DS} when the MOSFET is conducting full load current while $V_{DS(off)}$ is the value of V_{DS} when the MOSFET is off. In general, since C_{gd2} varies with the V_{DS} voltage it is difficult to approximate this value.

As seen from the above equations 3, 4, 5, only R_g, C_{gs} and C_{gd} play an important role in the rise time of the device. Using a similar analysis for the fall time of the device, it is observed that same components influence the fall time as well. In order, to solve for the values of these three parameters the above set of equations are not enough and more independent relations are required. To obtain that, we tie the gate and the drain and use the corresponding new relation for t_2. Since, in this case the gate and drain are shorted, it is expected that the gate-drain capacitance would not affect t_2 and the new time period $t_{2(new)}$ is given as follows:

$$t_2(new) = R_g \times C_{gs} \ln[1/(1 - V_{GP'}/V_{GG})] \quad (6)$$

where $V_{GP'}$ is the final gate voltage attained by the device when the gate and drain are shorted. The resistance at the gate R_g is mainly the source resistance emanating in the path before the gate which may be influenced by the gate driver circuit and/or the resistance of cables and hence is independent of the device characteristics damaged or otherwise. This resistance can be measured separately and used in conjunction with equations 3 and 6 to obtain the values of C_{gs} and C_{gd1}. Note that it is difficult to estimate the value of C_{gd2} since it varies with the applied voltage. However, an estimate of the static part of C_{gd} i.e., C_{gd1} should aid significantly in estimating damage or faults in a device if any is present.

4.2 Power MOSFET failure modes

Lightning surges can affect semiconductor devices in many ways. In some cases, it may lead to complete failure of the device, while in other cases the damage incurred allow the device to operate but not within expected performance measures.

For power MOSFETs, a few common modes of failures have generally been observed as summarized below:

- Parasitic BJT turn-on due to body diode reverse recovery: as mentioned in the earlier section 4.1, a parasitic BJT is present in the power MOSFET structure, which can get turned ON due to high rate of rise of drain-to-source voltage (dV/dt). Once this parasitic BJT is turned ON, the gate cannot be used to control the device anymore and hence the current flowing through the device cannot be turned

off leading to its failure. Though, in most of the current devices, the base and the emitter of the parasitic BJT are tied together by the source metalization, spurious turn-ons can still occur in particular during reverse recovery of the parasitic body diode. MOSFET parasitic body diode reverse recovery occurs during diode switching from the ON state to the OFF state due to the application of a negative voltage across it while in its ON state which leads to a high (dV/dt) (Dodge, 2006). Hence, peak commutating (body diode recovery) (dV/dt) limit are provided in the datasheet.

- Parasitic BJT turn-on due to high voltage at drain: An avalanche breakdown across the body diode may occur when a very high voltage is applied at the drain-source terminal as it increases the electric field at the body-epi junction (McDonald, Soldano, Murray, & Avram, 2000). All diodes have a specified limit for the electric field it can withstand in the reverse configuration. When, the electric field increases beyond this critical limit, avalanche breakdown of the diode occurs. This leads to avalanche multiplication of carriers leading to an abrupt increase in current. Though this avalanche multiplication does not destroy the device itself, the high current density may turn ON the parasitic BJT which finally leads to the device failure. In normal operations, such increases can occur due to sudden spikes which may occur due to inductive elements in the circuit. However, such spikes may appear due to lightning voltage injections, in particular when the lightning waveform is similar to the one shown in figure 1 used in our experiments.
- Gate oxide damage: The gate oxide region of MOSFETs are quite susceptible to damage leading to device failures. One of the most commonly documented damage inducing event is radiation and ESD (Electroststatic Discharge). However, as observed in our experiments, a single high-voltage pulse applied at the gate can also lead to significant damage to the device. Unfortunately, gate oxide damage is difficult to characterize and model since not much information is available that explains the phenomenon.

From the above discussion on the common modes of failure in power MOSFETs, it may be inferred that the lightning waveform injection with the D-S configuration may lead to avalanche breakdown of the body diode and lead to device damage. However, most modern power MOSFETs are made rugged against such avalanche multiplication. They are designed to avoid turning ON the parasitic BJT until very high temperature and/or very high avalanche current occurs. Thus, it is difficult to observe any damage due to diode breakdown as observed in our experiments with D-S injections.

From our experiments with injection using the G-S configuration, it was observed that for the high-level intensity of the injection voltage with 20 strokes, significant deviations occurred in all device performance characteristics. From our SMU characterization it was observed that the threshold voltage characteristics was significantly altered in these devices. The threshold voltage is affected by – amongst a set of multiple factors – substrate doping and oxide thickness. Excessive damage at the gate oxide could lead to the breakdown of the oxide which acts as a dielectric for the gate-oxide capacitor. Thus, though the dielectric provides a high impedance path under normal operations, such dielectric breakdown can provide conductive paths through it and lead to flow of current through the device even before the normal threshold voltage is provided at the gate. Under such damage conditions, the device would conduct current much earlier than the rated gate voltage for device turn-on is applied. Further, the I_{DS} variation with V_{GS} would also not follow the normal device characteristic since it depends on the gate-oxide capacitance. The high electric field causing damage at the gate can also propagate damages to the device silicon which may lead to various other spurious capacitative and/or resistive components. These new spurious elements may lead to alterations in other characteristics of the device such as reduced reverse breakdown voltage of the body diode which reflects damage in the body diode and various other leakage currents such as the drain-source leakage. All of these characteristics were observed for the highest intensity lightning voltage injections using the gate-source configurations. Modeling these damages in the device present a significant challenge and as mentioned earlier is one of our active directions for future research.

For the lower intensity lightning voltage injections, it was observed that the threshold voltage characteristic was affected without much change in other characteristics. Thus, these scenarios represent much less damage to the device as compared to the high-intensity injections and may be modeled using the modified values for the parasitic components. Both C_{gs} and C_{gd1} depend on the oxide capacitance and hence any minor damage to the oxide should reflect as a change in these capacitance values for the injected devices. These capacitances should also reflect any minor damage in the device body as well. These modified values can be obtained by analyzing the turn-on behavior of damaged devices as shown in section 4.1. Comparing these values to the ones for a normal device would provide an estimate of the extent of damage incurred by the device and hence would provide insights regarding the current state of health of the device.

5. MODELING EXPERIMENTS AND RESULTS

As shown in the previous section 4.1, an approximate model of a power MOSFET can be obtained by analyzing the switching characteristics of the device. In order to obtain these details of the switching characteristics, a finite voltage pulse was applied at the gate of the device under test (DUT) while providing required voltage at the drain. Specifically, a 1kHz voltage pulse of approximately 10V (9.5V) with a duration of 50μs was applied at the gate while a voltage of approximately $8V$ (7.9V) was applied at the drain terminal. The turn-on characteristic of the DUT was then recorded using the oscilloscope and used for further analysis.

As seen in figure 11, the turn-on characteristic has three distinct regions separated based on the change in characteristics of V_{GS}. By performing a slope analysis of V_{GS} these three different regions can be determined i.e., the delimiters for the separate regions can be obtained. In our experiments, we only use equation 4 i.e., equation for time period t_2. Time period t_2 can be easily

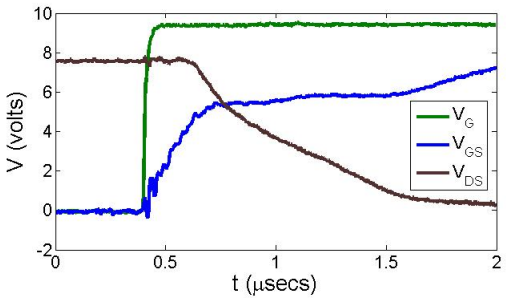

Figure 12: Turn-on characteristic for a normal MOSFET with a pulse input

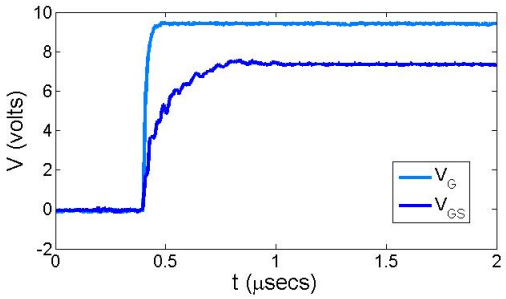

Figure 13: Turn-on characteristic for a normal MOSFET (gate and drain shorted) with a pulse input

detected by change in slope of V_{GS} only. However, we observed in our experiments that the Miller plateau region had a non-zero slope (figure 12). Thus, analysis of V_{DS} was used, in addition, to determine V_{GP} required to evaluate t_2.

A sample pulse response obtained from our experiments for a normal device is shown in figure 12. A similar slope analysis was performed for the pulse response of the devices with their gate and drain tied. Analysis of V_{GS} from this measurement yielded the value for $t_{2(new)}$. A sample pulse response obtained from our experiments for a normal device with gate and drain shorted is shown in figure 13.

This pulse response analysis was performed for both the normal devices and the lightning waveform injected devices. Since in our lightning injection experiments, the device was removed from normal operation and separately injected, it is expected that any of the biasing circuits used for pulse response measurement would not be affected. Thus, we assumed that the resistance R_g remained constant for the devices after injection. The value of R_g was measured separately ($1k\Omega$) and used in conjunction with equations 4 and 6 to determine the values of the capacitances C_{gs} and C_{gd1}. Note that the value of R_g used is quite high. This was done to ensure that the rise time during turn-on of the device was longer than normally used. At low-rise times, the signal at the gate was significantly distorted and hence could not be used for analysis.

These experiments were carried out using an in-house developed board and the pulse response was measured on an oscilloscope (Agilent Technologies DSO5034A).

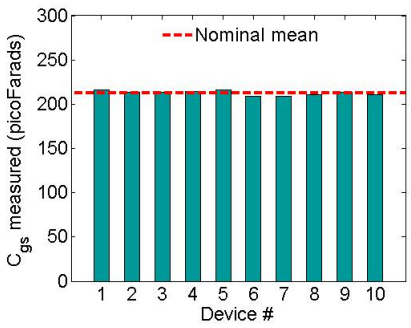

Figure 14: Gate source capacitance measured for normal device using pulse response

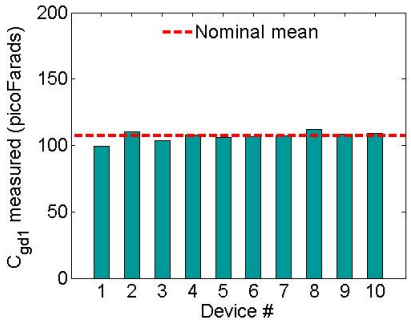

Figure 15: Gate drain capacitance measured for normal device using pulse response

Since, it is difficult to avoid extraneous spurious elements in a prototyping board such as parasitic inductances and capacitances, obtaining the actual values is quite challenging. Hence, all the values obtained from the experiments are only approximations for the actual values. Experiments with normal devices were first carried out in order to estimate the capacitance values for normal devices. We measured the values for multiple normal devices to observe the variation in the values. In figures 14 and 15 the values obtained for the gate-source capacitance for 10 normal devices is shown. The input capacitance (C_{iss}) value obtained was $319.61p$F which is very close to the value specified in the data sheet for this device ($330p$F). The average capacitance values for C_{gs} and C_{gd1} obtained from our measurements was found to be $212.59p$F (variance of $6.0322p$F) and $107.02p$F (variance of $12.2084p$F) respectively.

The C_{gs} and C_{gd1} values obtained from the damaged devices are shown in figures 16 and 17 respectively. The nominal mean represents the average capacitance value typically observed in a normal device. From figure 16, the capacitance value is seen to decrease from the nominal mean with an average mean of $9.579p$F. Note that C_{gs} represents a combination of capacitances and hence a decrease in the value could be due to damage in multiple locations including the gate as well as body. A significant increase in the C_{gd1} value is observed for the damaged device in figure 17 (average increase of $46.26p$F). Though, this capacitance is supposed to represent the static value of the C_{gd}, it is difficult to avoid the influ-

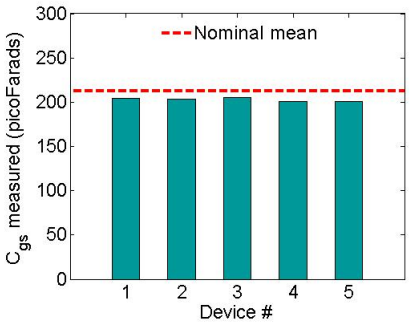

Figure 16: Gate source capacitance measured for damaged device using pulse response

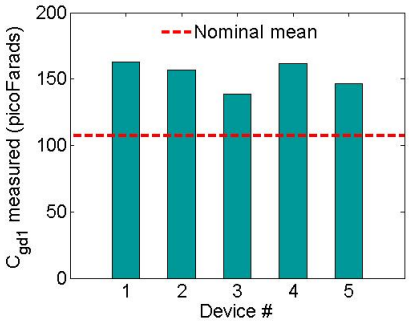

Figure 17: Gate drain capacitance measured for damaged device using pulse response

ence of the Miller capacitance C_{gd2} due to variations in V_{ds} (mainly due to noise) during experiments. The increase in this value, mainly represents damage incurred at the gate region. From these results, it may be concluded that with sufficient injection level of the lightning waveform at the gate of a power MOSFET, significant damage can be incurred by the gate as well as the body of the device just beneath the gate. As a result of these changes, it was observed that the input capacitance C_{iss} has decreased from the normal device value. This indicates a faster turn-on of the device which is also expected from the observation of reduced threshold voltage in the SMU measurements.

6. CONCLUSIONS

In this paper, a detailed study and analysis of a subset of lightning injection effects on power MOSFETs in their powered ON state has been presented. Our experiments showed that injections at the gate can lead to significant damage even at low injection intensities compared to injections using the D-S configurations where much higher levels of injection was required. In the G-S configuration, most of the damage observed was at the gate region, while for higher intensities significant damage was observed within the body as well.

In addition to our experiments and analysis, models for damaged devices with parameter estimation techniques were also developed. The model is simple yet sufficient in modeling the damage. The parameter estimation techniques used for the model are also simple yet efficient in representing the damage. From the modeling results for the damaged device, it was observed that the capacitances values C_{gs} and C_{gd1} in the model have significantly deviated from the normal device values which represents damage incurred both at the gate area as well as the body of the device. These deviations implied changes in the pulse response (faster turn-on) of the device and hence an abnormal state of health of the device.

Our future directions of work include further analysis of the device, in particular G-S injected devices with more damage i.e., significant leakage current (I_{DSS}) and so on, as seen in figures 3, 4 and 5. Modeling such damage for these devices is a complex problem involving various challenges. In addition further extension of the models in order to enable prognostics will be pursued which would include accelerated aging of the injected devices. In this effort we intend to verify the hypothesis that devices that are stressed by lightning will fail sooner than normal devices and that this time of failure can be predicted ahead of time. Detailed analysis of the other injection cases such as drain-source will be pursued as well.

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