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Research Article

An FPGA-Integrated Time-to-Digital Converter Based on a Ring Oscillator for Programmable Delay Line Resolution Measurement

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We describe the architecture of a time-to-digital converter (TDC), specially intended to measure the delay resolution of a programmable delay line (PDL). The configuration, which consists of a ring oscillator, a frequency divider (FD), and a period measurement circuit (PMC), is implemented in a field programmable gate array (FPGA) device. The ring oscillator realized in loop containing a PDL and a look-up table (LUT) generates periodic oscillatory pulses. The FD amplifies the oscillatory period from nanosecond range to microsecond range. The time-to-digital conversion is based on counting the number of clock cycles between two consecutive pulses of the FD by the PMC. Experiments have been conducted to verify the performance of the TDC. The achieved relative errors for four PDLs are within 0.50%–1.21% and the TDC has an equivalent resolution of about 0.4 ps.

1. Introduction

Many radar systems such as pulsed radar [1], ultra-wideband (UWB) radar [2, 3], random noise radar [4], and multiple input multiple output (MIMO) radar [5] require timing generator circuits to make timing adjustment. Programmable delay line (PDL) is often being applied as a high precision timing circuitry to introduce both coarse and fine delays. The performance of these radar systems depends a lot on the delay resolution of the PDL. However, the actual delay resolution of a PDL may differ slightly from its nominal delay resolution due to changes in temperature, power voltage, and other factors. To ensure correct timing, high resolution measurement of a PDL is essential before design begins. Since there is no direct way to realize the measurement of the delay resolution, it can be converted into time interval measurement by injecting two synchronized rising edges into two PDLs with different delays and connecting the two outputs of two PDLs to an XOR gate. Thus, the XOR gate yields a pulse signal with a pulse width related to the delay resolution. Then we can measure the pulse width to indirectly get the resolution. Time-to-digital converter (TDC) is being widely used for time interval measurement and TDC can be easily implemented by a digital device, such as a field programmable gate array (FPGA) or an application-specific integrated circuit (ASIC). Most available TDCs with picosecond resolution are implemented in ASIC technology as the technology allows precise control of the internal propagation times for signal. Seo et al. introduced a cyclic TDC with 1.25 ps resolution [6], whereas Kim et al. presented a pipelined TDC with 1.12 ps resolution [7]. Xu et al. described a TDC providing 0.84 ps resolution [8]. However, these TDCs have a very high cost of development and are not easily adaptable to new applications. In comparison with ASIC-based TDCs, FPGA-integrated designs [9–12] lack competitiveness in terms of resolution, although they are easily adaptable to a new application and have shorter development cycle and lower development cost. Therefore, an FPGA-integrated TDC with picosecond resolution is of great importance. This paper describes a TDC implemented in a

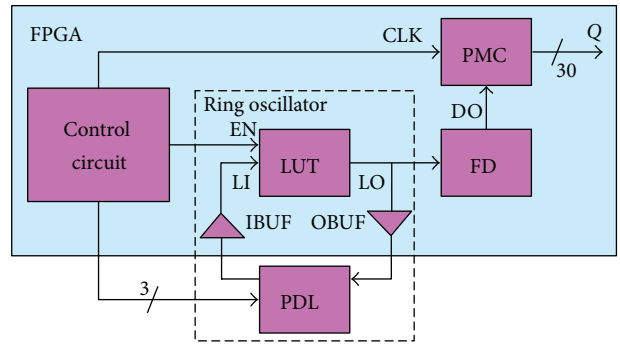


Figure 1: Block diagram of the proposed FPGA-integrated TDC.

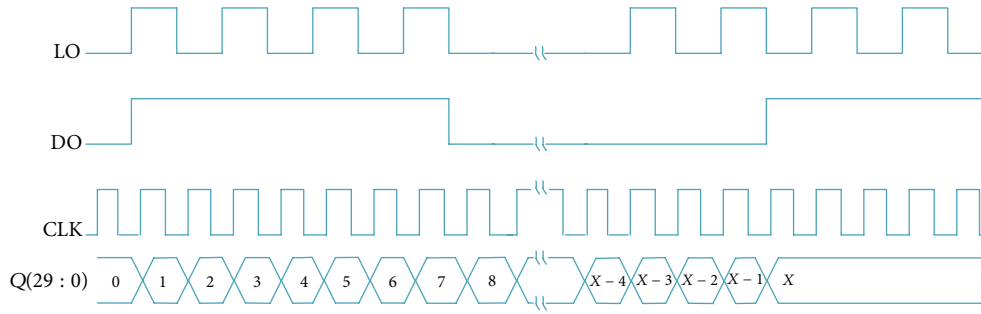


Figure 2: Timing diagram of the proposed FPGA-integrated TDC.

Table 1: Logic table of LUT.

Input		Output
EN	LI	LO
0	0	1
0	1	1
1	0	1
1	1	0

Xilinx FPGA device to measure the actual delay resolution of a PDL and it achieves an equivalent resolution of about 0.4 ps.

2. Operation Principles

A block diagram of the proposed FPGA-integrated TDC is illustrated in Figure 1. It is composed of three blocks, namely, the ring oscillator, the frequency divider (FD), and the period measurement circuit (PMC). The ring oscillator consists of a PDL, an input buffer (IBUF), an output buffer (OBUF), and a look-up table (LUT) with two inputs and one output. The logic table of the LUT is presented in Table 1.

The signal with a period of nanosecond range from the output of the ring oscillator needs to be amplified to microsecond range by the FD before it enters into the PMC. The FD has a divide ratio of D and the PMC involves the use of a counter driven by a reference clock CLK of period T_{CLK}. The time-to-digital conversion is based on counting the number of clock cycles between two consecutive pulses of the FD by the PMC. Timing diagram of the FPGA-integrated TDC is shown in Figure 2.

The oscillation period of the ring oscillator derived using the most common way is given as follows:

$$T = 2\left(t_0 + t_1 + t_2\right), \tag{1}$$

where t_0 is the variable time delay PDL yields, t_1 is the constant time delay PDL yields, and t_2 is the time required by the signal to propagate from the output of the PDL to the input of the PDL. Delays t_1 and t_2 are constants, while t_0 is programmable to be modified. The period of the FD's output signal is given by

$$T_0 = D \times T. \tag{2}$$

The PMC measures the period T_0 to obtain the result $X = T_0/T_{\mathrm{CLK}}$, where X is an unsigned decimal integer at the PMC output.

In the proposed FPGA-integrated TDC, when the variable time delay of the PDL is modified, the outputs of the three blocks would change. When the variable time delay of the PDL is programmed to t_{01}, the signal period of the ring oscillator is recalculated using

$$T_1 = 2\left(t_{01} + t_1 + t_2\right), \tag{3}$$

where $t_{01} = Y_1 \times \Delta T$, Y_1 is a control word generated by FPGA and ΔT is the actual delay resolution of the PDL. The PMC output can be written as $X_1 = D \times T_1/T_{\mathrm{CLK}}$.

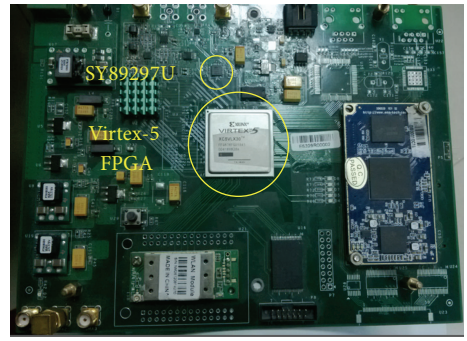
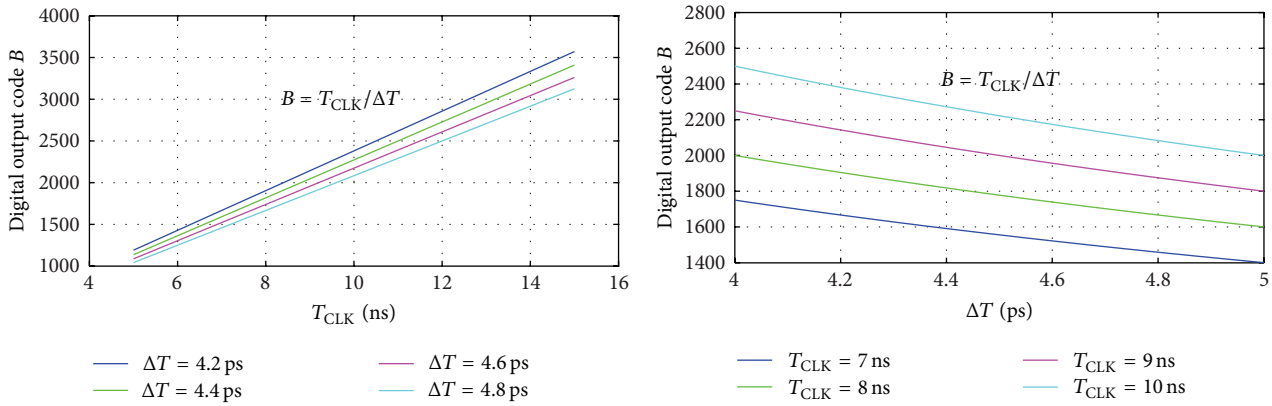


Figure 3: Photograph of the radar board.



(a) Different ΔT (b) Different T_{CLK}

Figure 4: Simulated characteristic curves of the proposed TDC.

When the variable time delay of the PDL is programmed to t_{02}, the signal period of the ring oscillator is then recalculated using

$$T_2 = 2\left(t_{02} + t_1 + t_2\right), \tag{4}$$

where $t_{02} = Y_2 \times \Delta T$ and Y_2 is a control word generated by FPGA. The PMC output can be written as $X_2 = D \times T_2 / T_{CLK}$.

By combining (3) and (4), the actual delay resolution ΔT can be calculated using

$$\begin{aligned} \Delta T &= \frac{\left(T_1 - T_2\right)}{2\left(Y_1 - Y_2\right)} \\ &= \frac{\left(X_1 - X_2\right) \times T_{CLK}}{\left(2\left(Y_1 - Y_2\right) \times D\right)} \\ &= \frac{T_{CLK}}{B}, \end{aligned} \tag{5}$$

where $B = 2(Y_1 - Y_2) \times D/(X_1 - X_2)$.

By combining (1) and (2), we can get

$$\left(t_0 + t_1 + t_2\right) = \frac{X \cdot T_{CLK}}{2D}. \tag{6}$$

Thus, we give an equivalent TDC resolution of $T_{CLK}/2D$, since the TDC is intended to measure the delay resolution instead of the time interval.

Table 2: Brief comparison of the four PDLs.

PDL number	1	2	3	4
System clock period T_{CLK} (ns)	7.532	7.940	7.890	7.782
Clock uncertainty ΔT_{CLK} (ns)	0.087	0.035	0.035	0.087
Digital output code B	1650	1773	1786	1726
Absolute error ΔB	1	1	1	1
Relative error (%)	1.21	0.50	0.50	1.18
Actual delay resolution Δt (ps)	4.56	4.48	4.42	4.51
Nominal delay resolution ΔT (ps)	5	5	5	5

3. Experimental Results

To evaluate the performance of the proposed converter, we implemented its structure on a radar board equipped with a Virtex-5 FPGA device (Xilinx) and a programmable, two-channel delay line SY89297U (Micrel) as shown in Figure 3. Simulated characteristic curves of the proposed TDC are illustrated in Figure 4. Experiments were performed on four different radar boards at an ambient temperature of about 22°C with the use of Xilinx Integrated Software Environment (ISE) 13.2 written in Verilog. We set $Y_1 = 1000$, $Y_2 = 500$, $D = 10000$. The digital output code B was collected using Xilinx ChipScope Pro Analyzer which was also used to verify

Table 3: Brief comparison with previous works.

	[6]	[7]	[8]	[12]	This work
Structure	Cyclic	True pipeline	SAR-ADC	Vernier	Ring oscillator
Process (nm)	130	65	65	65	65
Device	ASIC	ASIC	ASIC	FPGA	FPGA
DNL (LSB)	±0.7	0.6	−0.7/1.0	N/A	N/A
INL (LSB)	−3~+1	1.7	−2.7/1.7	−0.93~0.75	N/A
Resolution (ps)	1.25	1.12	0.84	1.58	Equivalent to 0.4

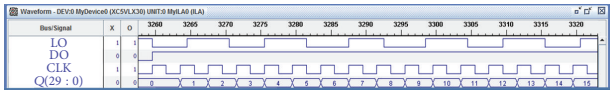


Figure 5: Measured timing diagram of the proposed TDC.

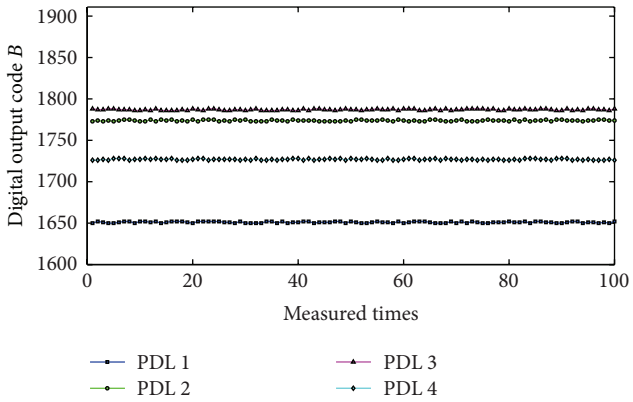


Figure 6: Measurement results of the proposed converter for four PDLs.

the actual timing of the TDC as depicted in Figure 5. Measurements were repeated 100 times during each experiment. The measurement results of the proposed converter for four PDLs are shown in Figure 6. Furthermore, a relative error can be determined. Assume that the clock uncertainty of the system clock is ΔT_{CLK} and that the absolute error of the digital output code is ΔB; then the relative error can be calculated as $(\Delta T_{\mathrm{CLK}}/T_{\mathrm{CLK}} + \Delta B/B)$. Figure 7 shows that the relative errors were measured to be within 0.50%–1.21%, which were in a reasonable range for programmable delay line resolution measurement.

Table 2 gives a brief comparison of the four PDLs. As the four PDLs are not measured by the same TDC but separately measured by its corresponding TDC, the reference clocks of the TDCs would demonstrate difference in clock period and clock uncertainty. Furthermore, the FPGAs where the TDCs are implemented also have influence on clock period and clock uncertainty. Thus, the four PDLs show different relative errors. As the system clock period T_{CLK} is about 8 ns and the divide ratio D equals 10000, then the equivalent TDC resolution $T_{\mathrm{CLK}}/2D$ equals about 0.4 ps.

Table 3 summarizes the performance comparison of several TDCs. Compared with [6–8, 12], the proposed TDC achieves the highest resolution. Hence, this TDC is more competitive than other TDCs for programmable delay line resolution measurement.

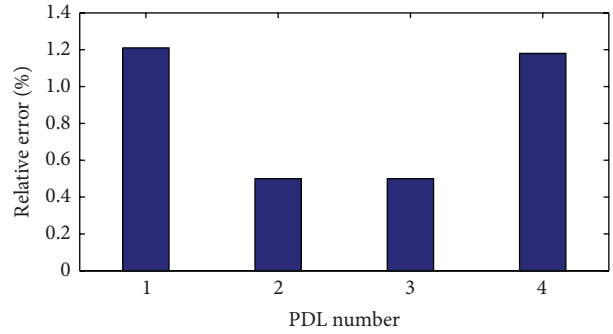


Figure 7: Relative error variation for four PDLs.

4. Conclusion

We realized an FPGA-integrated TDC with 0.4 ps equivalent resolution using an architecture based on a ring oscillator. It measures the delay resolution of the PDL used in radar systems to ensure correct timing generation. It also provides great operating flexibility as FPGA can allow for an easy configuration to support both delay resolution measurement and radar control. The TDC that we proposed is very promising and well suited for use in radar applications.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgment

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