Printed organic TFTs on flexible substrate for complementary circuits

ECS Transactions, 54 (1) 153-163 (2013)
10.1149/05401.0153ecst ©The Electrochemical Society

PRINTED ORGANIC TFTs ON FLEXIBLE SUBSTRATE FOR COMPLEMTARY CIRCUITS

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Organic Thin film Transistors (OTFT) have been widely investigated in these last years as potential candidate for the development of low cost, flexible and lightweight active-matrix backplanes for display applications. Indeed the organic semiconductors provide both promising electrical performances tunable by chemistry and the ability to be processed at low temperature with innovative printing technics on various large scale substrates. Thanks to the recent developments on both n-type and p-type solution-processed organic semiconductors, we have developed a printable organic complementary technology compatible with flexible PEN substrates. By combining state of the art materials exhibiting mobility in the range of 1 $cm^2/V.s$ and silicon inspired compact modeling and simulation approach, we were able to design and fabricate circuit's building blocks that provide the switching, digital and analog functions required for the fabrication of printed systems on foil.

Introduction

Organic thin Film Transistors (OTFT) have been widely investigated for their interest as switching elements in active matrix backplanes for display [1]. Indeed, solution based organic semiconductors (OSC) offers nowadays both N-type and P-Type materials with mobility performances similar to those in conventional a-Si:H[2]. Moreover processing materials through solution enables printing techniques that could bring strong advantages for their integration on flexible plastic substrate: low temperature deposition on Large Area with high throughputs offering a potential cost-effective alternative to amorphous silicon. However, organic based technologies still suffer from the lack of visibility in terms of process and tooling risk to be competitive in the replacement of a-Si:H technology for displays. Indeed, MCO (Multi Component Oxide) could provide promising performance (μ~10-20 cm^2/Vs) as well as better compatibility with the current display fabrication model [2]. Nevertheless thanks to the ability to be processed by printing techniques at low temperature, the Organic TFT technology keep a strong and direct interest in the development of printed electronics. With large area and high throughputs on flexible substrate, printed OTFT could be integrated with large pixel displays (Electrophoretic or Electrochromic) for signage applications or with printed sensors for environmental mapping (Temperature, Mechanical stress, Photo-detectors, Smart bandage …). In this context printed OTFT circuits with switching, digital and

analog functions could provide interfacing circuits (Active Matrix, Decoder, Multiplexer, Counter, Comparator, Digital-to-Analog Converter …) for displays or sensors.

Printed Organic TFTs & Resistances Technologies

In this paper we are presenting circuits made of three different technologies developed for the fabrication of printed system on foil: Complementary OTFT technology [3] and its compatible printed resistors for digital and analog circuits as well as standalone P-type OTFT technology optimized for switching applications.

Device fabrication

Complementary Process Flow - Gold is first sputtered to a thickness of 30 nm on a 125-µm thick polyethylene-naphtalate (PEN) foil. Source and drain electrodes are patterned either by photolithography or directly by laser ablation. Then, a Self-Assembled Monolayer (SAM) is deposited to optimize electron injection in the Lowest Unoccupied Molecular Orbital (LUMO) of the N-type organic semiconductor [4]. The N-type OSC (Polyera ActivInk®) is first formed by screen-printing, leading to a final thickness in the range of 50-200nm. Then, the source/drain electrodes and the PEN in P-type areas are cleaned with an O2 UV-free plasma prepare the surface for the SAM and P-type OSC deposition (TIPS-pentacene). The thickness of P-type OSC patterns is also in the 50-200nm range. A common fluoropolymer dielectric (CYTOP®) is then screen-printed on top of both semiconductors with a final thickness of 750nm and annealed, leaving open areas for via holes. A silver-ink conductor is finally screen-printed on the top of the dielectric and annealed at 100°C, forming in the same step the gate electrodes for devices and the 2nd level for interconnection. For analog requirements we have also developed within the FP7 COSMIC project [5] printed resistors compatible with the complementary flow. The resistors, processed by screen-printing and annealed at 100°C, have a sheet resistance value of approx. 75 kOhm/sq. (Fig. 2).

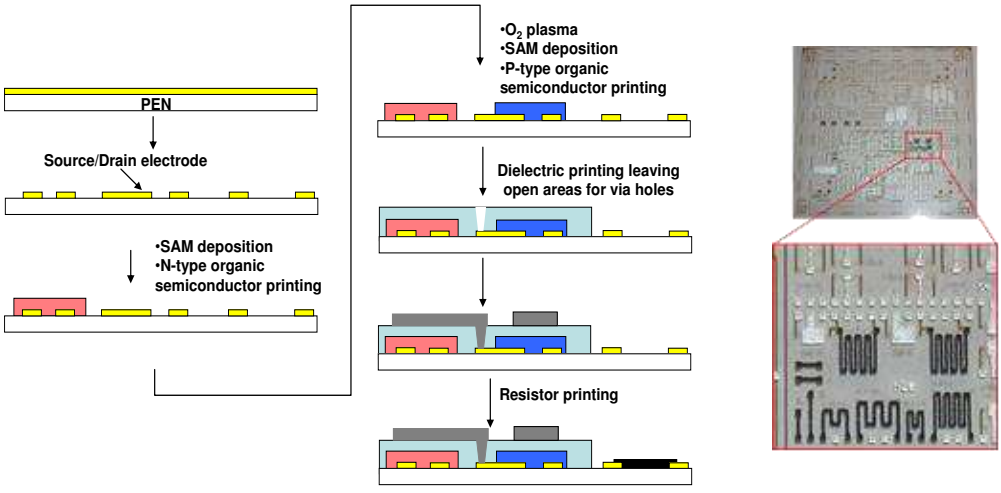


Figure 1: Left-Schematic view of the complementary process flow. Right – Picture of printed Complementary foil with resistors.

Stand-alone P-OTFT Process-flow – A specific process flow has been developed in order to optimize the performance of the Top-Gate Organic P-type OTFT with a focus on the voltage reduction and improvements in variability and yield at fixed geometry. Figure 2 shows schematic process-flow of the fabricated device. In order to be independent from

substrate's roughness and its electrical properties, a buffer layer is first deposited on the PEN substrate. This blanket deposition in the range of 1µm in thickness is processed either with spin-coating or Slot-Die coating for larger substrates. This layer, which is optimized for the matching with subsequent P-type semiconductor, is then exposed to UV in order to become resistant to the solvents later used during the fabrication process. The first metallization level employed for drain and source electrode is made of PVD sputtered gold with a thickness of 30 nm and patterned either by photo-lithography or laser ablation. Following a soft cleaning with O_2 UV-free plasma, the P-type organic semiconductor (TIPS-pentacene derivative) is patterned with a thickness in the range of 50 to 150nm by printing. The subsequent processes are similar to the Complementary technology with screen-printed Fluoropolymer as dielectric (Cytop) and Ag-ink as gate electrode.

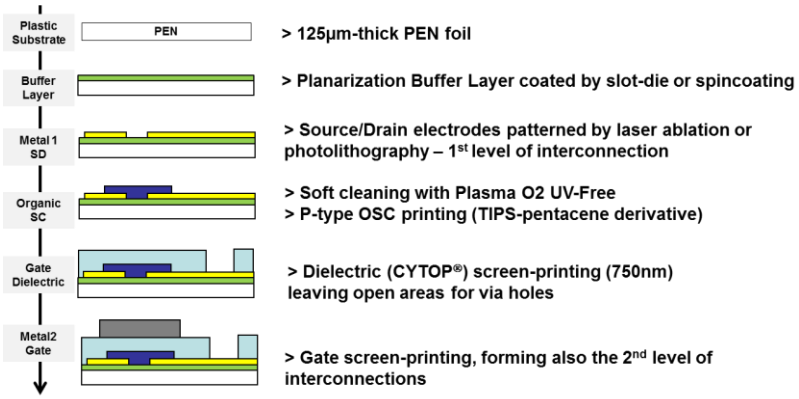


Figure 2: P-OTFT process flow optimized for switching applications.

Electrical Performances of printed devices

For all of the printed devices presented here, electrical characterizations of devices have been performed in air. The electrical performances of the printed devices are summarized further in table I.

Electrical characteristics for Complementary Technology – Transfer curves of N- and P-type devices with L=100µm and W=2000µm processed with our complementary technology are plotted on Fig. 2, exhibiting mobilities of 1.5 cm².V-1.s-1 for P-OTFTs and 0.55 cm².V-1.s-1 for N-OTFTs [3]. The typical electrical characteristics of transistors are listed in table I. In addition to high mobility, both P and N-type transistors present high ratio between the On and Off currents as well as steep subthreshold slopes.

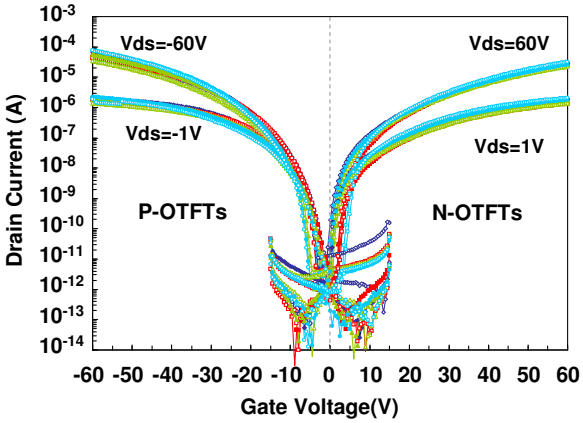


Figure 3: Transfer characteristics in linear (|Vd|=1V) and saturated (|Vd|=60V) regime of 8 P-OTFTs and 8 N-OTFTs of the complementary process flow. L=100µm W=2000µm.

Electrical characteristics for Stand-alone P-OTFT – The transfer and output characteristics for a P-type transistor designed with a channel of 500µm in width (multi-finger 4x125µm) and 20µm in length are presented on the figure 4. On the (I_D-V_{GS}) characteristic we can observe very low off current and improved sub-threshold swing with respect to similar dielectric thickness (750nm). The extraction for this P-OTFT technology is in the range of S~0.5-1 V/decade. Regarding threshold voltage, the preliminary extractions from the (I_D/V_{DS}-V_{GS}) and (√IDd-V_{GS}) characteristics conclude in low threshold voltages V_{th} in the range of [0-2V]. These performances could enable functional operation with voltage as low as 20V. The mobilities extracted for such devices are in the range 0.5-1 $cm^2.V^{-1}.s^{-1}$. Moreover from the (I_D-V_{DS}) characteristics we do not observe any S-shape at low V_{DS} suggesting no specific contact resistance distortion.

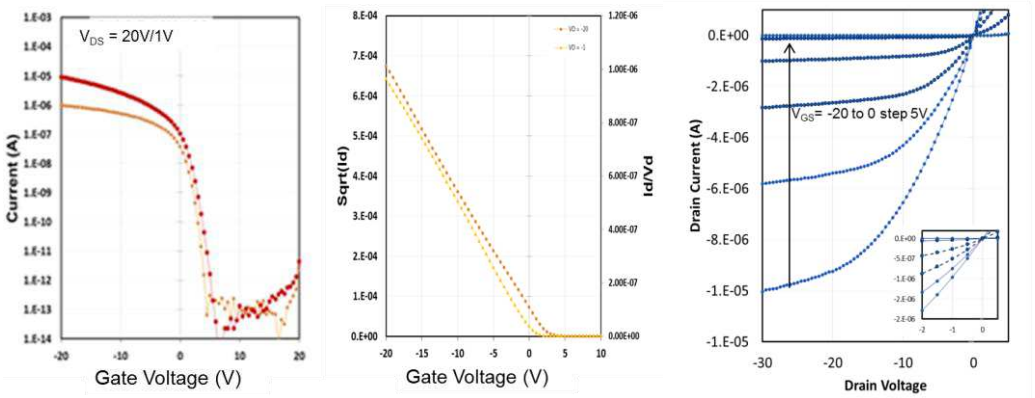


Figure 4: Electrical characteristics for Standalone P-OTFT: Left- Transfer Characteristics (I_D-V_{GS}) in log scale; Center- (I_D/V_{DS}-V_{GS}) and (√IDd-V_{GS}) characteristics in linear scale; Right- Output characteristics (I_D-V_{DS}).

TABLE I. Technology Performance for the presented printed devices

Electrical performances	**Complementary P-OTFT** (W=2000;L=100)	**Complementary N-OTFT** (W=2000;L=100)	**RESISTOR** (L=20)	**Standalone P-OTFT** (W=500;L=20,Vdd=20V)
Cox (pF/mm^2)	20	20	-	20
μ_{sat}($cm^2.V^{-1}.S^{-1}$)	1.5	0.55	-	0.8
Ion_{sat} L/W (A)	~2.10^{-6}	>10^{-6}	-	~6.10^{-5}
$Ioff_{sat}$ L/W (A)	~2.10^{-13}	~2.10^{-14}	-	~1.10^{-13}
Ion/Ioff	~10^7	>2.10^7	-	~5.10^7
Vt_{sat} (V)	-20	18	-	~2.5
V_{onset}(V)	-0.2	1	-	5
Sub-threshold Swing (V/dec)	2.4	1.2	-	0.5-1.0
Resistance	-	-	75kΩ/□	-

Compact Modeling and Technology Design Kit

In order to make this technology available for academic and industrial partners, it has to be supported by a complete technology design kit (TDK) based on standard silicon electronic design automation (EDA) flows. The main components of a TDK are the design rules manual (DRM), the Spice [6] simulation models for the various devices, and

the verification tools, DRC (design rules check) and LVS (Layout Vs Schematic). With this information, a designer is able to design, simulation, lay out and verify an IP.

The compact models for the transistors are based on the RPI amorphous Silicon TFT model [7], which demonstrates a very close behavior when compared to the characterization results of our transistors. In addition to the DC current computed by the aTFT model, a network of access components has been added to reproduce accurately the characteristics of the transistors. Gate to drain and source access resistors (RGD, RGS) have been added to model the gate leakage effects. A drain to source resistance (RBC) emulates the ohmic part of the conduction (involuntary doping of the channel). Finally, two gate-voltage dependent capacitances (CGD, CGS) between gate and source/drain account for Gate-to-Channel capacitance and allow an accurate transient simulation of the device. The complete schematic for the transistor model is shown in fig 5:

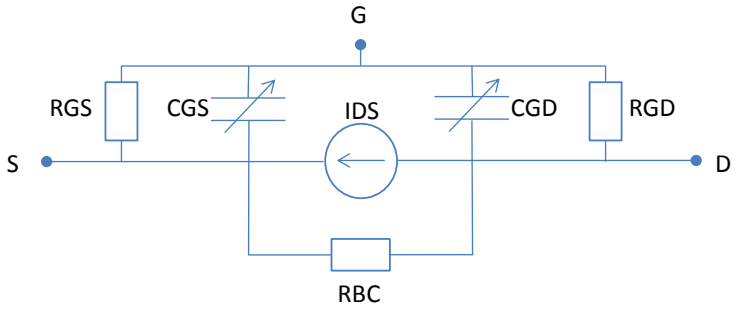


Figure 5: Structure of the transistor simulation model

The models for the CMOS N-OTFT and P-OTFT have been developed, as well as the model for the stand alone P- OTFT. The results of this modeling are shown in fig 6:

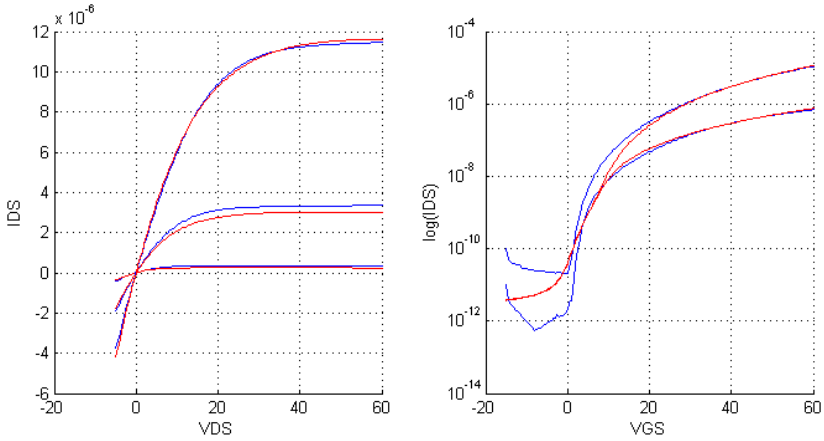
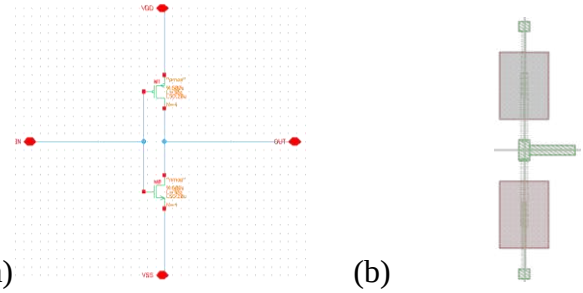


Figure 6: Comparison between characterization results (blue) and model (red)

The available technological layers and the corresponding design rules have been included in a complete TDK available in Cadence Virtuoso 6.1 format [8], and Eldo spice simulator [9]. The design rules can be checked using the DRC Calibre software from Mentor Graphics, and the LVS can be verified also with Calibre [10]. These various tools are the most widely used software for designing analog and mixed-signals IPs in silicon technologies.

Using this TDK, several IPs have been designed, simulated, and the simulation results were compared to the actual characterization results of the fabricated devices. The example of a simple inverter gate is shown below on figure 7. As it can be seen, the simulation is accurate and the characterization results fit well with the simulation.



(a) (b)

Figure 7: Schematic (a) and layout (b) of an inverter gate in Virtuoso format.

Using this inverter gate, a complete 7 stage ring oscillator can be created:

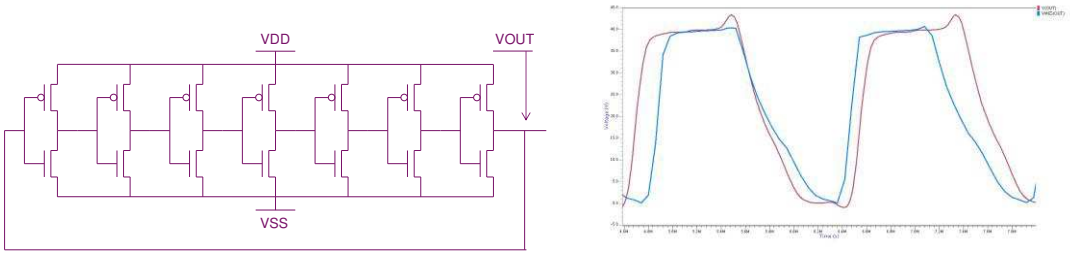


Figure 8: Schematic (Left) and simulation results (Right) of ring oscillator

Printed Circuits Building Blocks

Based on the design-kit environment (DTK) developed, circuits library have been designed and several mask sets including different analog and digital circuits have been processed on 11cm x 11cm foils. The circuits were measured in air and over several weeks showing there that without specific encapsulation the operational and shelf-life times are not critical.

Digital Building Blocks

In order to demonstrate and study the stability of typical digital building blocks a 7-stage ring oscillator made of inverter have been fabricated and characterized. Fabricated device and electrical measurements are presented on the figure 9. The extraction of oscillation frequencies varying from 1.2 kHz @ 40V to 200Hz @ 20V corresponds to a delay per gate of 60µs and 350µs, respectively. Despite the lack of encapsulation, after 6 months in ambient air, the oscillation frequency, reported on figure 10, remains basically unchanged (1.4kHz@40V). However we can observe a modification of the pull down behaviour, which may derive from the progressive degradation of channel conductivity from plastic substrate.

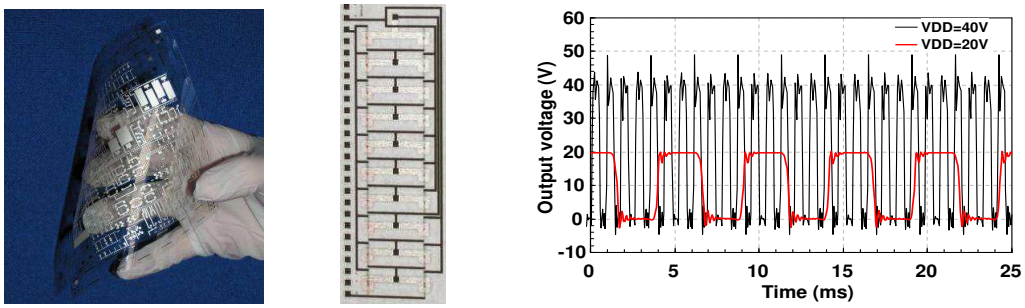


Figure 9: Left - Pictures of an 11cm x 11cm plastic foil with printed single devices and complementary digital and analog circuits. Center – detailed view of a 7-stage ring

oscillator. Right - Transient response of a 7-stage complementary ring oscillator with equally sized P-and N-type OTFTs for VDD=40V and 20V. L=20µm W=1000µm.

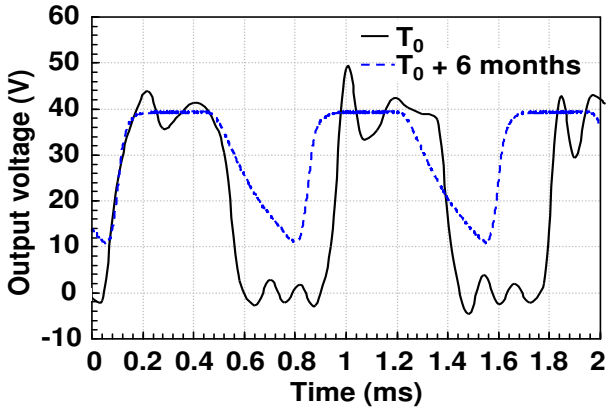


Figure 10: Shelf-lifetime of the ring oscillator kept for 6 months in ambient air without passivation. VDD=40V.

Analog Building Blocks.

Simple analog circuits have been also processed and tested on plastic foils. The figure 11 presents the schematic and measurements of three different Operational Trans-conductance Amplifiers (OTAs) [11]. The circuit was measured statically with one of the inputs (In+) kept to 25V DC, while the other input (In-) was swept. Figure 11(b) shows that the three OTAs are functional, with an output offset varying from 1.5 to 4V, which is due to the fact that there is still some dispersion on OTFTs characteristics.

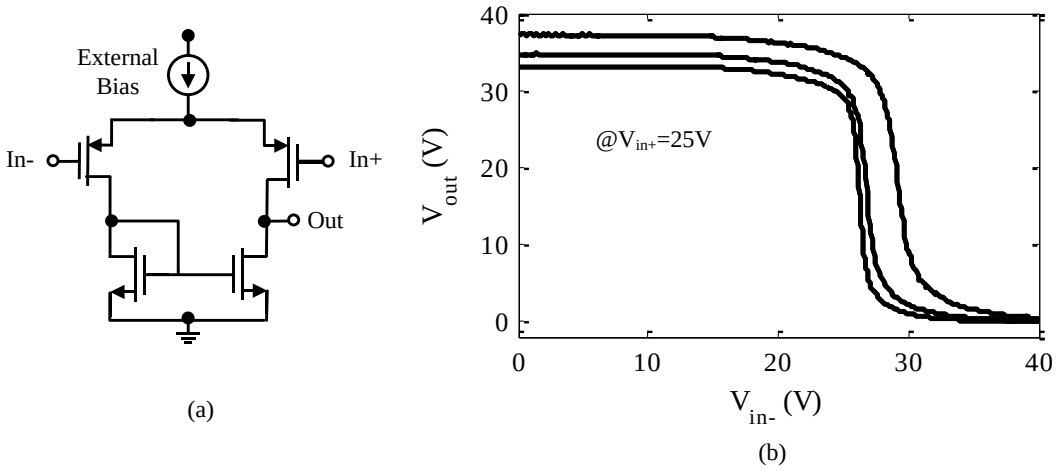


Figure 11: (a) Schematic of the OTA, (b) Experimental results of static measurements on 3 samples of the OTA on two different foils. The output is measured when In+ is set at 25V and In- is swept.

Thanks to the resistors technology, we have fabricated a 4-bit printed R-2R Digital to Analog Converter (DAC) [12]. The circuits and electrical characterization are presented on figure 12 and 13. The In-Out measured characteristic of the DAC is very closed to ideal one, demonstrating a good matching of the printed resistors.

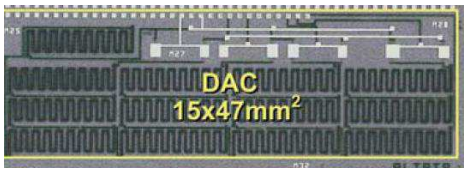


Figure 12: Picture of the R-2R Digital to Analog Converter (DAC)

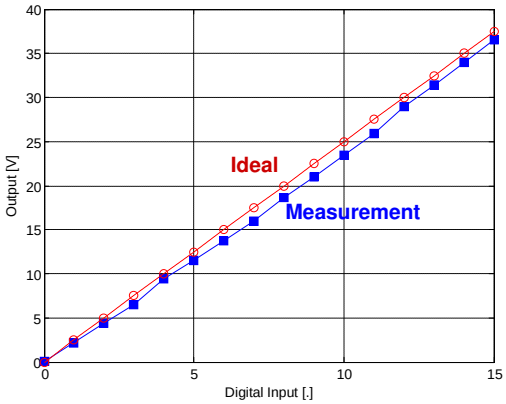
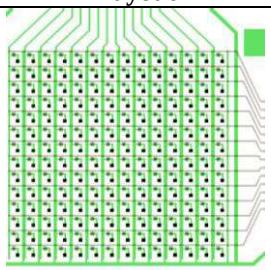


Figure 13: In-Out measurement of the Digital to Analog Converter (DAC).

Active Matrix Circuits

The Stand-alone P-OTFT technology has been employed for the fabrication of 5x5 cm² large pixel active matrix circuits. Made of 14x14 columns and lines, individual matrixes are composed by 196 transistors with channel width of 500µm and length of 20µm. This matrix developed for engineering has a large pitch for side by side integration of 3mm² devices thus providing an aperture ratio in the range of 60%. Details on matrix configuration are summarized in the Table II.

TABLE II. Large pixel Active Matrix Circuit

Parameters	Details	Layout
Number of Transistors (NA)	196	
Transistor Width (µm)	500	
Transistor Length (µm)	20	
Pixel Pitch (µm)	2300	
Aperture Ratio (%)	~60%	
Total Area (mm²)	50x50	

For switching applications the static criteria are the voltage amplitude required to drive the selector, the switching ratio of current (on-off ratio) and uniformity in currents for both selection states. The matrix configuration with 196 devices enables here a statistical analysis of these performances. The transfer characteristics in linear regime with a gate voltage of +-20V are reported on the figure 14 for each individual switch. In the set of devices presented here we can observe that all transistors are functional with a ratio of current superior to six decades. As observed on the figure 14 reporting the mobility in saturation regime (μ_{SAT}), the on-current dispersion wich could be critical for

device driving in on-state is linked to variation in mobilities originating from crystallization inhomogeneity on the foil (see mapping on figure 14-c).

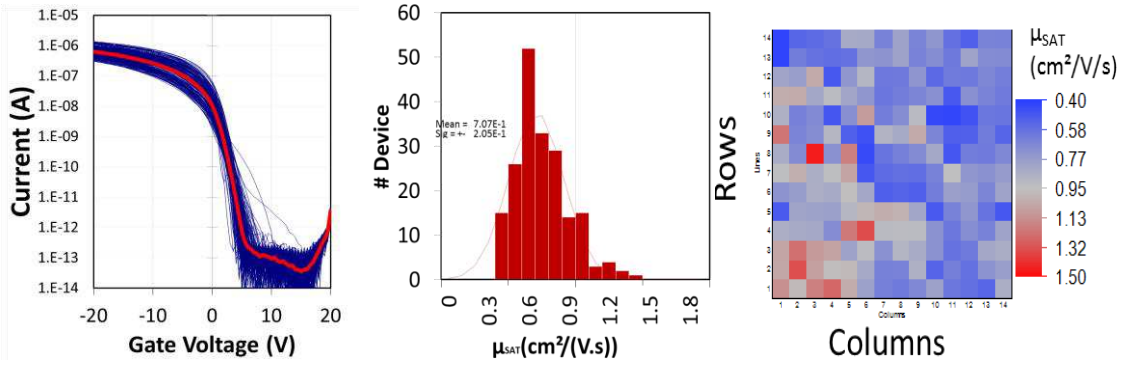


Figure 14: Left- Transfer characteristic in linear regime for 196 devices in a matrix. Center- Distribution of mobility in saturation regime for 196 devices. Right – Mapping of mobility in the matrix

On the transfer characteristics figure 14, we can notice the degradation of the sub-threshold behavior for a few devices related to defects in the printing of OSC patterns. This unexpected behavior has direct impact on the switching dynamics (on to off current range) reported on figure 15 in saturation regime (V_{DS}=20V). Such defect could be damaging for sensing system where a high off current transistor would increase the global line leakage current and thus decrease the sensibility of whole line.

Therefore crystallization uniformity and defect in OSC printing would be the major challenges for active matrix in driving or sensing applications.

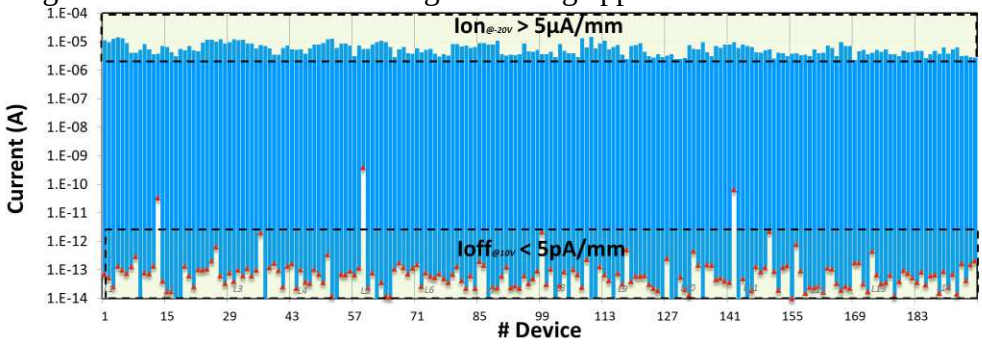


Figure 15: Switching dynamics in saturation ($Ion_{@-20V}$; $Ioff_{@10V}$) for the 196 device of the matrix

Mixed Circuits for printed systems on foil

In the frame of the COSMIC project, fully-static logic gates, flip-flops and comparators have been processed and characterized. Small-sized envelope detectors have also been measured at the HF RFID frequency (13.56MHz), to demonstrate the high frequency performance of the OTFTs [11]. All these circuits are the building blocks for the realization of a RFID tag. The second lead application of the project is a 4-bit Analog to Digital Converter (ADC) which can enable applications exploiting sensors that do not require high-speed or high-resolution, like coarse ambient temperature monitoring. The simplified structure of the ADC is shown on figure 16. It consists of three blocks: a counter, the 4-bit R-2R DAC presented in the previous section, and a comparator. Each block was separately measured, and all of them showed correct functionality [12].

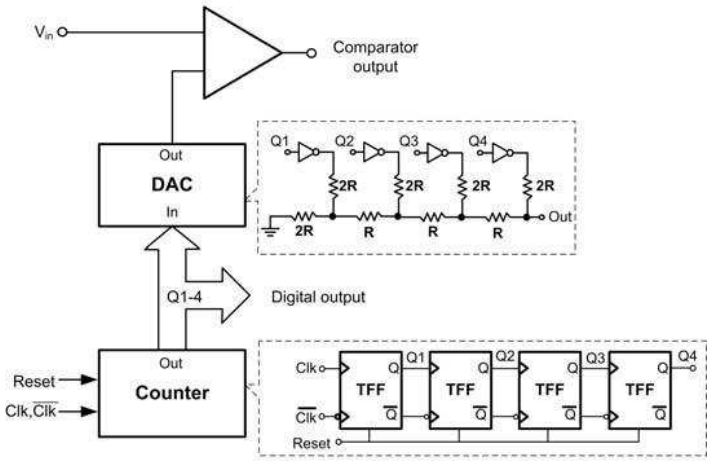


Figure 16: Simplified ADC architecture. The comparator output determines at which clock the digital output corresponds to the analog input (Vin).

Conclusions

Thanks to the ability to be processed through printing technics, Organic Thin Film Transistors (OTFT) could play a role in the fabrication of large area flexible system on foil. In this context we have developed complementary OTFT technologies including P-type OTFT, N-type OTFT and compatible printed resistors in order to provide digital and analog functionalities. A p-type OTFT technology has been also optimized for switching applications. Integrated in a Design Tool-kit, these technologies have been employed in the fabrication of different functional organic based circuits including inverter, ring oscillators, Operational Trans-conductance Amplifiers, Resistor based Digital to Analog Converter and Active matrix.

Acknowledgments

This work was funded in the frame of the European FP7 project COSMIC (grant agreement n° 247681). The authors want to thanks Polyera Corp. for supplying N-type semiconductor ActivInk® material.

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