Low-Voltage Low-Power Fast-Settling CMOS Operational Transconductance Amplifiers for Switched-Capacitor Applications

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ABSTRACT
This paper presents a new fully differential operational transconductance amplifier (OTA) for low-voltage and fast-settling switched-capacitor circuits in digital CMOS technology. The proposed two-stage OTA is a hybrid class A/AB that combines a folded cascode as the first stage with active current mirrors as the second stage. It employs a hybrid cascode compensation scheme, merged Ahuja and improved Ahuja style compensations, for fast settling.

Categories and Subject Descriptors
B.7.1 [**Hardware**]: Integrated Circuits

General Terms
Design

Keywords
Cascode compensation, Class AB, Switched-capacitor circuits, Operational transconductance amplifiers.

1. INTRODUCTION
The realization of a CMOS operational amplifier that combines high dc gain with high unity gain bandwidth has been a difficult problem especially in low voltage circuits. The high dc gain requirement leads to multistage designs or cascoding of transistors with long channel devices biased at low current levels, whereas the high unity gain frequency requirement calls for a single stage design with short channel devices biased at high bias current levels. Cascoding is a well-known means to enhance the dc gain of an amplifier without degrading the high frequency performance. But cascoding is not possible in the low voltage circuits. Another technique to achieve both high DC gain and unity gain bandwidth is to employ gain boosting [1], [2]. But in this technique at least four transistors should be cascoded at the output. Two-stage OTAs can be used to achieve the high dc gain. But the major concern is the speed of this type of amplifiers due to their additional pole and zeros in their signal transfer functions, where without any frequency compensation, they can be unstable.

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Fortunately, some frequency compensation methods have been proposed to design a stable two-stage OTA such as miller and cascode compensation schemes [3].

In this paper a two-stage OTA with a new compensation technique is proposed to satisfy the high dc gain requirement for high-speed applications. The proposed two-stage OTA has a class A/AB structure with a new hybrid cascode compensation scheme. The class AB structure of the second stage reduces the OTA's power consumption and the proposed hybrid cascode compensation enhances its speed.

In section (2) the new merged OTA structure is introduced and analyzed. Design procedure for this OTA is described in section (3). Section (4) presents simulation results. Finally, conclusions are summarized in section (5).

2. PROPOSED OTA
Figure 1 shows the proposed OTA structure. The first stage is a folded cascode amplifier with PMOS input transistors. PMOS input differential pair allows the use of near ground as the opamp input common mode voltage, *Vcmi*. This, in turn, allows the use of relatively small NMOS transistors to design the switches that are connected to *Vcmi.* The second stage is a class AB amplifier with active current mirrors similar to [4]. Due to class AB operation of this stage, slew limiting only occurs in the first stage. The second stage currents are chosen in order to the non-dominant poles are adequately high in frequency to guarantee the stability. Because of push-pull operation, the lowest non-dominant pole in the class A/AB design is governed by the time constant formed by approximately twice the transconductance of the output PMOS transistors, M_4 and the load capacitance. Thus the output branch current can be about half that used in the two-stage class A circuit for the same non-dominant pole frequency. When this fact is exploited together with the use of gain in the second stage current mirrors, a significant reduction in power dissipation can be achieved relative to the two-stage class A topology. The mirror pole and zero will eventually degrade the phase margin of the circuit and finally its settling performance. To increase the mirror pole and zero frequencies in the active current mirrors, NMOS transistors are used in this design.

It uses two simple switched-capacitor common mode feedback circuits to define the voltage of first and second stage outputs.

Frequency compensation is needed to maintain stability in a two-stage amplifier. The standard miller compensation has a pole splitting effect, which moves one pole to a lower frequency and the other to a higher frequency. The two-stage amplifier shown in Figure 1 employs the hybrid cascode compensation scheme,

merged Ahuja [3] and improved Ahuja style [5] compensation methods, which creates two real poles, two complex poles at a higher frequency, and three zeros. This scheme of compensation yields a higher amplifier bandwidth compared to the standard miller and conventional cascode compensation techniques at the cost of more complex design procedure for the settling behavior of the amplifier. This implies that for practical designs some form of computer optimizations constrained by the tradeoffs in the design equations will be necessary.

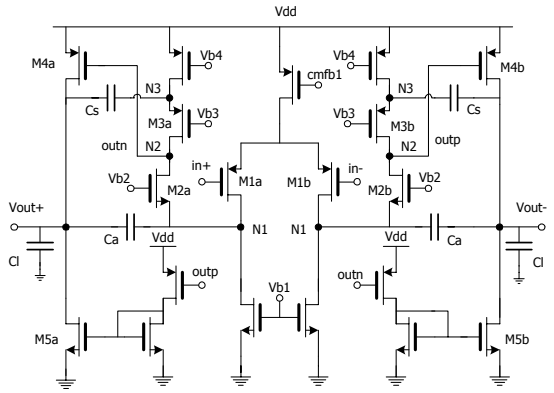

Figure 1. Proposed OTA Structure.

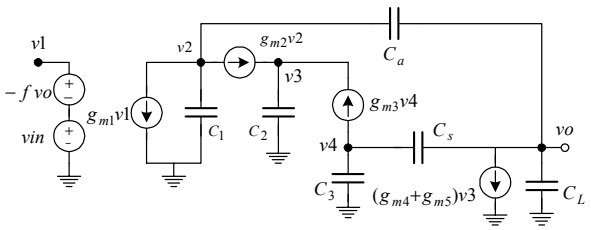

Figure 2. Closed-loop small-signal equivalent circuit.

Figure 2 shows the closed-loop small-signal equivalent circuit for pole and zero analysis of the proposed OTA shown in Figure 1, where C_1, C_2, C_3, and C_L represent the parasitic capacitances of nodes N_1, N_2, N_3, and the output node of the circuit shown in Figure 1, respectively. f is the feedback factor. To simplify the analysis, device output resistances are assumed to be infinite. It should be noted that the effect of finite device resistance is to move the amplifier poles slightly to the left, which will slightly increase the bandwidth of the amplifier [6]. The node equations of this circuit are as follows:

$$g_{m1}v1+(sC_1+g_{m2})v2+sC_a(v2-vo)=0 \quad (1)$$

$$sC_2v3-g_{m2}v2-g_{m3}v4=0 \quad (2)$$

$$(sC_3+g_{m3}+sC_s)v4-sC_svo=0 \quad (3)$$

$$(sC_L+sC_a+sC_s)vo-sC_av2+(g_{m4}+g_{m5})v3-sC_sv4=0 \quad (4)$$

$$v1=vin-fvo. \quad (5)$$

The transfer function will be as follows:

$$\frac{vo}{vin}=\frac{g_{m1}(s^2C_aC_2-g_{m2}g_m)(g_{m3}+sC_3+sC_s)}{s^4d4+s^3d3+s^2d2+sd1+d0} \quad (6)$$

where

$$g_m=g_{m4}+g_{m5} \quad (7)$$

$$d4=C_a^2C_2(C_3+C_s)+C_s^2C_2(C_1+C_a) -C_2(C_L+C_a+C_s)(C_1+C_a)(C_3+C_s) \quad (8)$$

$$d3=C_aC_2fg_{m1}(C_3+C_s)+C_a^2C_2g_{m3}+C_2C_s^2g_{m2} -g_{m2}C_2(C_L+C_a+C_s)(C_s+C_3) -g_{m3}C_2(C_L+C_a+C_s)(C_1+C_a) \quad (9)$$

$$d2=fg_{m1}g_{m3}C_aC_2-g_{m2}g_mC_a(C_3+C_s) -g_{m3}g_mC_s(C_1+C_a)-g_{m2}g_{m3}C_2(C_L+C_a+C_s) \quad (10)$$

$$d1=-fg_{m1}g_{m2}g_m(C_3+C_s)-g_{m2}g_{m3}g_mC_a -g_{m2}g_{m3}g_mC_s \quad (11)$$

$$d0=-fg_{m1}g_{m2}g_{m3}g_m. \quad (12)$$

In order to verify the usefulness of the proposed compensation technique, the settling time of Ahuja style, improved Ahuja style, and the proposed compensation techniques are shown as a function of the total compensation capacitance in Figure 3. In these simulations the small signal parameters as shown in Table 1 have been used. According to Figure 3, the proposed compensation technique can give a smaller settling time compared to the other alternatives.

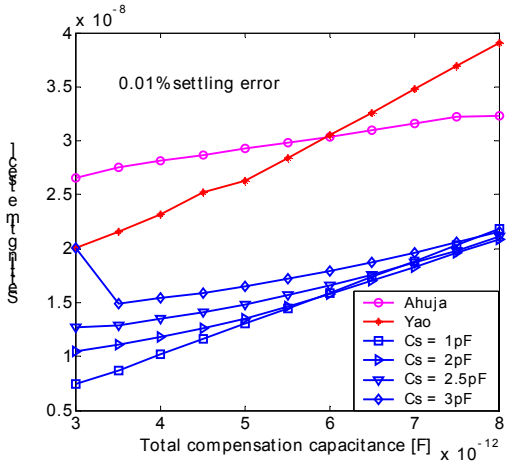

Figure 3. Settling time with different compensation techniques.

Table 1. Small-signal parameters.

Parameter	Value	Parameter	Value
g_{m1}	4 mA/V	C_1 [pF]	0.206
g_{m2}	4.7 mA/V	C_2 [pF]	0.627
g_{m3}	4.2 mA/V	C_3 [pF]	0.267
g_{m4}	5.7 mA/V	C_L [pF]	4
g_{m5}	7.4 mA/V	f	0.8

3. DESIGN PROCEDURE

In order to investigate the settling behavior of the proposed compensation technique a standard fourth order system with the following transfer function is considered

$$H(s)=\frac{k(\gamma^2\zeta^2\omega_n^2-s^2)(s+z\zeta\omega_n)}{(s+\alpha\zeta\omega_n)(s+\beta\zeta\omega_n)(s^2+2\zeta\omega_ns+\omega_n^2)}. \quad (13)$$

There are six system parameters, α, β, γ, ω_n, ζ and z in the transfer function. ω_n and ζ are called natural frequency and damping factor, respectively. Figure 4 shows the description of these six

system parameters by the location of poles and zeros of the proposed compensation technique in a practical implementation.

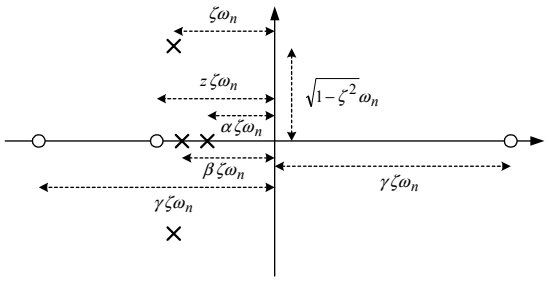

Figure 4. Closed-loop pole and zero locations.

In switched-capacitor circuits, the step response determines the amplifier settling performance in the time domain. It can be shown that the step response of the above-mentioned fourth order system is as follows:

$$s(t)=A_{cl}\{1-a1\times e^{-\alpha\zeta\omega_n t}-a2\times e^{-\beta\zeta\omega_n t} + a3\times e^{-\zeta\omega_n t}\left(a4\times\cos(\omega_n t\sqrt{1-\zeta^2})\right) - a3\times e^{-\zeta\omega_n t}\left(a5\times\sin(\omega_n t\sqrt{1-\zeta^2})\right)\} \quad (14)$$

where A_{cl} is the closed-loop gain and

$$a1=\frac{\beta(z-\alpha)}{z(\beta-\alpha)(1-2\alpha\zeta^2+\alpha^2\zeta^2)} \quad (15)$$

$$a2=\frac{\alpha(z-\beta)}{z(\alpha-\beta)(1-2\beta\zeta^2+\beta^2\zeta^2)} \quad (16)$$

$$a3=\frac{\alpha\beta\zeta}{z(1-2\alpha\zeta^2+\alpha^2\zeta^2)(1-2\beta\zeta^2+\beta^2\zeta^2)} \quad (17)$$

$$a4=-z\zeta\left((\alpha-1)(\beta-1)\zeta^2-1+\zeta^2\right)+(\alpha\zeta^2-1)(\alpha+\beta-2)\zeta \quad (18)$$

$$a5=\left\{\left(z\zeta^2-1\right)\left((\alpha-1)(\beta-1)\zeta^2-1+\zeta^2\right) + z\zeta^2(1-\zeta^2)(\alpha+\beta-2)\right\}\frac{1}{\sqrt{1-\zeta^2}}. \quad (19)$$

In the calculation of the step response it is assumed that γ goes to infinity since in the practical cases the right and left-plane z_p zero pair in the closed loop transfer function will be at much higher frequencies than the poles.

The settling error as defined $\varepsilon_s=\frac{s(\infty)-s(t_s)}{s(\infty)}$ is obtained by:

$$\varepsilon_s = a1\times e^{-\alpha\zeta\omega_n t_s}+a2\times e^{-\beta\zeta\omega_n t_s} - a3\times e^{-\zeta\omega_n t_s}\left(a4\times\cos(\omega_n t_s\sqrt{1-\zeta^2})\right) + a3\times e^{-\zeta\omega_n t_s}\left(a5\times\sin(\omega_n t_s\sqrt{1-\zeta^2})\right). \quad (20)$$

This equation is very complex to intuitively explain how to choose the system parameters to optimize the settling error. Therefore, numerical calculations are used. Figure 5(a), (b), (c), (d) show the settling error of the proposed compensation technique for different values of the system parameters. For example, the obtained system parameters for –120 dB settling error are $\alpha=0.95$, $\zeta=0.9$, $z=0.9$, $\beta=0.95$ and $\omega_n t_s=17$.

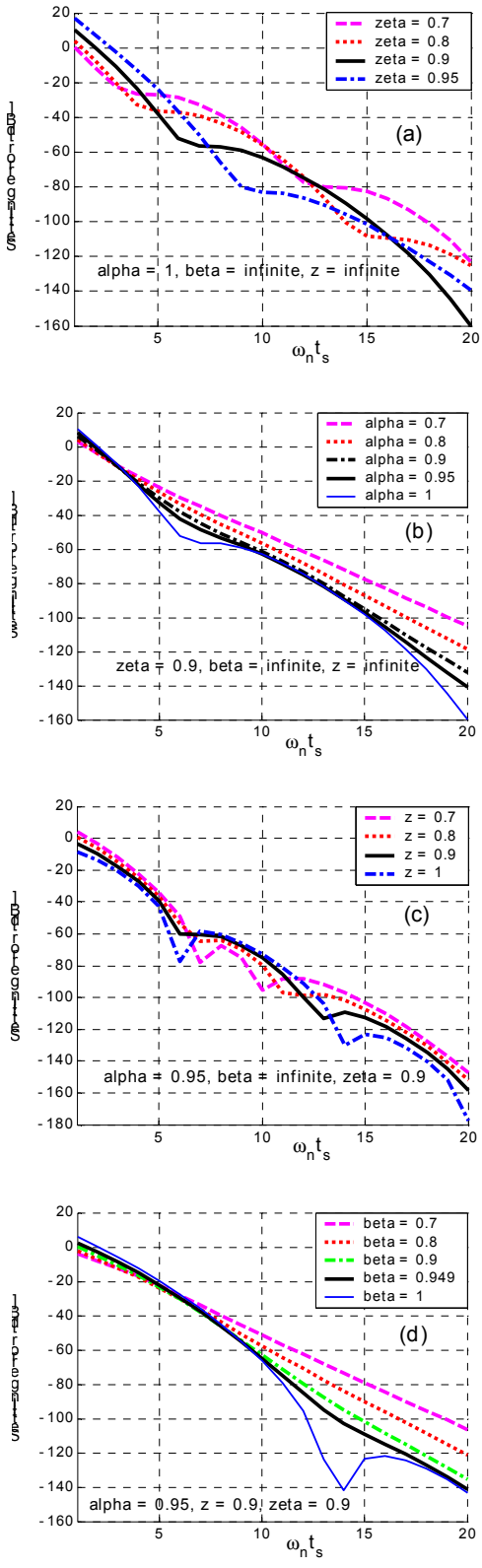

Figure 5. Settling errors as a function of $\omega_n t_s$ for different values of (a) ζ, (b) α, (c) z, and (d) β.

The obtained system parameters for a specific settling error in a defined time can be used to determine the device parameters with the following equations:

$$(\alpha+\beta+2)\omega_n\zeta=\frac{d3}{d4} \quad (21)$$

$$\left(2(\alpha+\beta)\zeta^2+\alpha\beta\zeta^2+1\right)\omega_n^2=\frac{d2}{d4} \quad (22)$$

$$\left((\alpha+\beta)\zeta+2\zeta^3\alpha\beta\right)\omega_n^3=\frac{d1}{d4} \quad (23)$$

$$\alpha\beta\zeta^2\omega_n^4=\frac{d0}{d4} \quad (24)$$

$$z\zeta\omega_n=\frac{g_{m3}}{C_s+C_3}. \quad (25)$$

In these equations, the system parameters, α, β, z, ζ, and ω_n are known. The load and compensation capacitances, C_L, C_a, and C_s are determined due to circuit noise considerations. The parasitic capacitances, C_1, C_2, and C_3 are related to the device sizes. Also all of device transconductances can be expressed by transistor sizes. So, these equations can be solved to determine the device sizes using numerical calculations. Then one can run circuit level simulations to fine the obtained gate dimensions from system level calculations.

4. SIMULATION RESULTS

In order to demonstrate the usefulness of the proposed OTA and its compensation technique, three different design examples with Ahuja style, improved Ahuja style, and the proposed compensation techniques were considered in the circuit level. At first, the system parameters of these design examples were obtained using their settling error equations with numerical calculations. Then, their circuits were simulated in a 0.25-µm CMOS technology with HSPICE. In these simulations, the OTAs were designed for a switched-capacitor integrator where sampling, integrating, and load capacitances were 2.5pF, 10pF, and 2pF, respectively. The bootstrapped switches have been used in these designs. In Figure 6 the settling behavior of the proposed OTA with three different compensation methods is shown. Simulation results are given in Table 2.

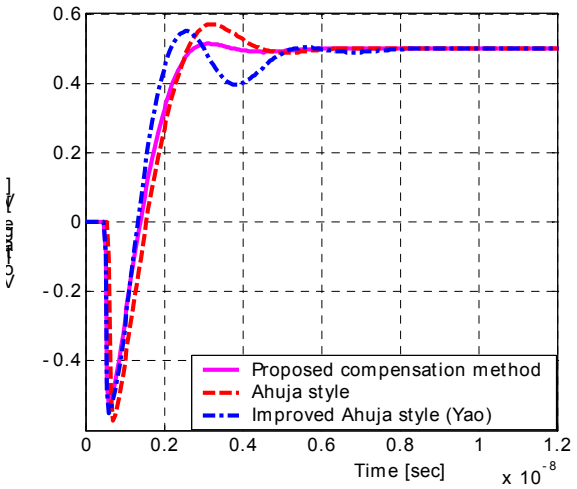

Figure 6. Settling simulation results.

Table 2. Simulation results.

Parameter	Ahuja	Improved Ahuja	Proposed method
Power supply voltage	1.5-V	1.5-V	1.5-V
DC gain [dB]	80.3	79	80
Unity gain bandwidth [MHz]	137	151	167
Phase margin [degree]	75.5	89	73.5
Compensation cap.	3 pF	3 pF	3 pF
Load capacitance	4 pF	4 pF	4 pF
Settling time (0.01%)	10.1 ns	12.4 ns	7.1 ns
Output swing [V_{pp}]	1.13	1.13	1.13
Input referred thermal noise [V^2/Hz]	1.6×10^{-16}	1.5×10^{-16}	1.2×10^{-16}
Power consumption	8.9 mW	8.9 mW	8.9 mW

5. CONCLUSIONS

In this paper a new merged two-stage class A/AB OTA has been proposed. Because of the class AB operation of the second stage, the currents in this stage are determined so that the non-dominant poles and zeros are sufficiently large in frequency to maintain stability. So, the second-stage currents are not constrained by the slew rate limiting of the OTA. To move the mirror pole and zero to a high frequency, NMOS transistors are used in the active current mirrors. It employs merged cascode compensation technique, which results in fast settling compared to conventional miller, Ahuja style, and improved Ahuja style compensation techniques at the cost of more complex design procedure. A design procedure is also considered for the proposed OTA.

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