Comparison of CHARM-2 and Surface Potential Measurement to Monitor Plasma Induced Gate Oxide Damage

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Abstract

Plasma process induced gate oxide damage was found in early process development stages. Device data showed unacceptable burn-in failure. By utilizing multiple test vehicles, the underlying cause of oxide damage was identified. This study showed that no single methodology is adequate for controlling the damage. A combination of the monitoring techniques is required to understand root cause of damage and how to optimize the process or equipment. The plasma process was optimized and verified with CHARM-2 monitor response. Further device data verification indicated no gate oxide damage was found with new improved process. The fast turn around time of plasma monitors were essential to understand and determine the plasma damage source. Understanding the relationship between plasma monitor response and plasma process is a key point to identify the source of damage. A fingerprint of plasma process is very useful for process control and defect reduction.

I. Introduction

Plasma induced gate oxide damage has been an increasly important issue for integrated circuits process technology. The damage usually causes device performance degradation, yield loss, or unacceptable reliability failure. Using fully processed device wafers to analyze charging problems is time consuming and very expensive. Since device wafers have to be processed through multiple plasma process steps, the electrical data always has a lot of noise and needs to be carefully analyzed to isolate and understand the charging source. Several techniques have been used to study the damage mechanism and charging potential of plasma process [1, 2, 3]. This study shows that use of multiple test vehicles significantly improved the ability of identifying and understanding root cause of the plasma induced gate oxide charging problem. By utilizing CHARM-2 charging monitor wafer, a new improved process has been developed and proved to have no impact on the device wafers

II. Charging Source Investigation

The device data showed unacceptable burn-in results in the early development stages. Gate oxide pin hole was found in failed devices. Device wafers were partitioned at different process steps to isolate the charging source. Surface Potential Measurement (SPM) and CHARM-2 charging monitor wafers were used to investigate the possible charging source and understand the cause of the damage.

1. Surface Potential Measurement (SPM)

1000A thermal oxide wafers were used for Surface Potential Measurement. The SPM indicated the photoresist strip process has highest positive voltage, as shown in Figure 1, compared with other plasma processes. The wafer map shows a center circle (bulls-eye) pattern which is similar to the device burn-in failure wafer map. The oxide deposition process showed a negative potential with a gradient voltage drop across the wafer, as shown in Figure 2. The SPM results indicated the source of damage is likely to be the photoresist plasma ashing process.

2. CHARM-2 charging monitor wafer

CHARM-2 wafers were also used to evaluate the individual plasma process step and to understand the cause of gate oxide damage. The CHARM-2 wafers are equipped with EEPROM based sensors to record the voltage, current flux, and UV intensity during the process [4,5]. The photo-resist ashing process showed very high positive potential in the center of wafer as shown in Figure 3, but the plasma J-V current was low. It may not necessarily cause the damage. The positive potential map from oxide deposition also showed high potentials in the center, as shown in Figure 4. Further examined, the plasma J-V current of oxide deposition process has much higher current than the resist ashing process, as shown in Figure 5. This surprising result indicated that the oxide deposition process may be the source of the damage. A further device lot experiment was performed to isolate these two possible processes. It revealed that the damage was caused by plasma oxide deposition processes at the inter-metal dielectric deposition. The gate leakage current was increasing on wafers processed through oxide deposition with center dies failure. The gate leakage current increased as the device wafer went through more IMD oxide deposition process, while the other split without oxide deposition showed no gate leakage failure or

threshold voltage shift. This indicated the damage was caused by the back end oxide deposition process.

III. Comparison of SPM and CHARM-2 data

The relaitonship between SPM and CHAMR-2 data for resist ashing process was studied. The correlation between SPM and CHARM-2 data is shown in Table 1. It showed the same trend for the process condition changes. Process condition 2 has higher voltage reading in SPM measuremtn also shows a higher positive potential in CHAMR-2 data. Since resist ashing has only one plasma charging step, the response from both SPM and CHARM-2 are correlated to each other.

Process conditi	SPM Voltage (V)	CHARM-2 positive potential (V)
Process 1	3	12
Process 2	7	19

Table 1. SPM and CHAMR-2 correlation, resist ashing.

Further analysis of CHARM-2 data of oxide deposiiton process showed that positive J-V plots from unipolar charge flux sensors in center dies showed shift to lower potentials, as shown in Figure 6, indicating that positive charging occurred at elevated temperatures. (CHARM-2 unipolar charge flux sensors use diode in parallel with current-sensing resistor, as shown in Figure 7. At elevated temperature, leakage current through the diode reduces current throught the current-sensing resistor. This lowers the voltage across the resistor, causing lower voltage and current readings. This shifts the J-V plots toward the origin.)

This information is very useful in this case. Since resist ashing is at relatively low temperature compared with oxide deposition process, whose temperature is about 350°C to 400°C. The response of the negative potential and charge-flux sensors showed a gradient similar to the response obtained with the SPM measurement, as shown in Figure 8. However, the peak negative current density at the gate oxide breakdown voltage was negligibly small (compared to the positive current density), and would not have been capable of causing damage to the gate oxide. Moreover, a comparison of responses obtained with simple potential and charge-flux sensors vs. unipolar potential and charge-flux sensors indicate that negative charging did not occur at the oxide deposition temperature, but at a much lower temperature, when gate oxide would have been significantly less susceptible to damage. (The charge-to-breakdown oxide, Qbd, is function of temperature [6]. The higher process temperature the lower Qbd. At elevated temperature, the amount of charge needed to cause gate oxide damage is much less than at lower temperature.

From CHARM-2 data, it is clear that damage happened at the deposition process step. The SPM method reveals the last event of the wafer process history. It may not correlate to the source of damage. To investigate the source of negative potential, the wafer was intentionally rotated before being loaded into the chamber. Figure 9 shows the SPM response also correlated to the rotation. It was concluded that negative potential is coming from the wafer moving out of chamber while plasma is still on. This was confirmed by turning the plasma OFF before moving the wafer, which resulted in SPM bulls-eye pattern.

Process optimization was done on oxide deposition process to prevent the gate oxide damage. CHARM-2 wafer was used to monitor the plasma process of the new optimal process. It has reduced the positive plasma J-V current siginificantly, as shown in Figure 10. CHARM-2 data in Figure 10 predicted that damage should not occured with new optimal process. The device wafer results proved the new process condition is free of plasma induced gate oxide damage. No more gate leakage current was observed.

IV. Conclusions

Several conclusions are obtained from this experiment.

1. SPM and CHARM-2 data can be correlated for single plasma charging step process such as resist ashing. For multiple plasma charging process, SPM reveals the last event of the wafer surface, it may not correlate to device damage results. In our case, the device damage happened during the oxide deposition step. The negative voltage SPM reading was the wafer from the plasma chamber after deposition.

2. The device damage is caused by accumulated charge. CHARM-2 is able to record the charging current passing through gate oxide to identify the charging source and evaluate the potential damage process.

3. Fully processed device wafers are the ultimate test vehicle to evaluate and verify the plasma process effect on the gate oxide, while CHARM-2 wafers were used to identify the charging source and fingerprint the process and equipment.

4. No single test methodology is adequate for controlling the damage. A combination of the monitoring techniques is required to understand root cause of damage and how to optimized the process or equipment.

5. This study shows use of multiple test vehicle significantly improved the ability of identifying and understanding root cause of the plasma induced gate oxide

charging problem. By utilizing CHARM-2 charging monitor wafer, a new improved process has been developed and proved to have no impact on the device wafers.

V. References

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VI. Acknowledgements

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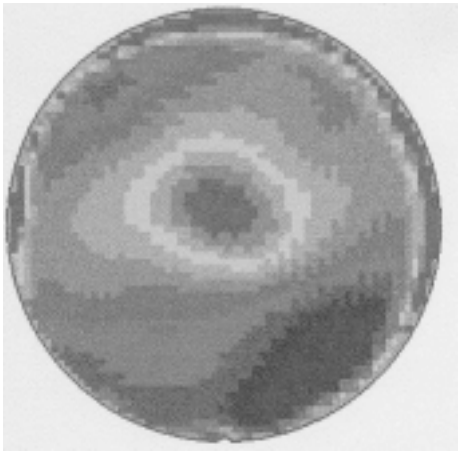

Figure 1. SPM positive potentials; resist asher. Center high (bulls-eye) pattern.

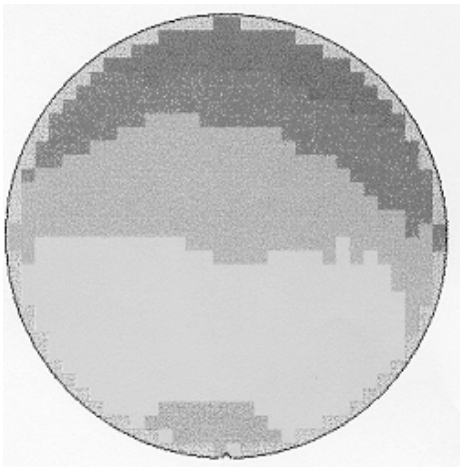

Figure 2. SPM negative potentials; oxide deposition. Directional voltage drops from top to bottom.

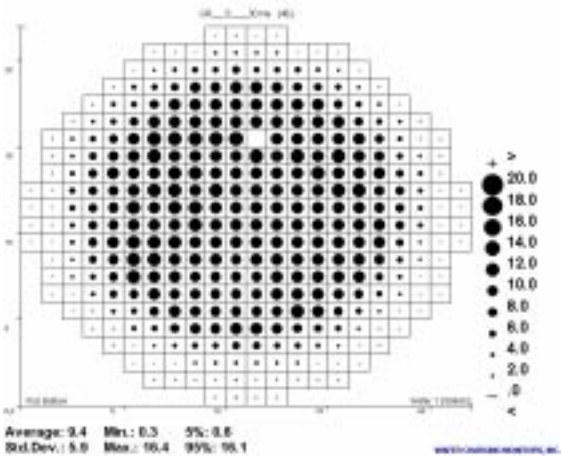

Figure 3. CHARM-2 positive potentials; resist asher. The potential sensors are saturated at 16 V.

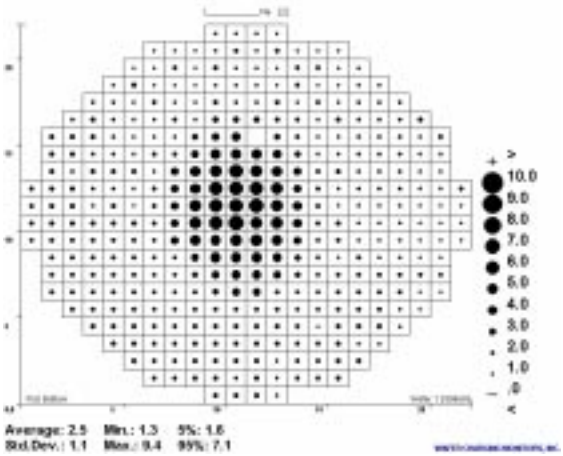

Figure 4. CHARM-2 positive potentials, oxide deposition.

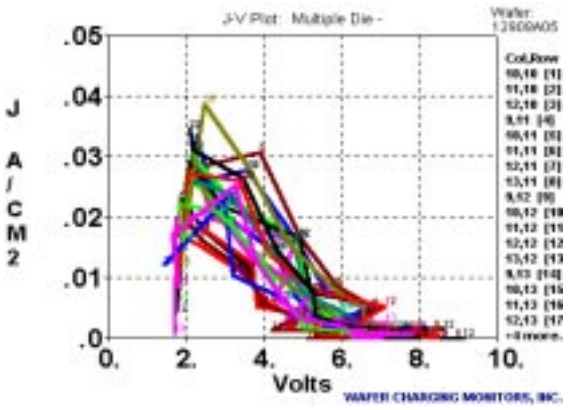

Figure 5. CHARM-2 positive J-V plots from die in the center of the wafer,oxide deposiiton process.

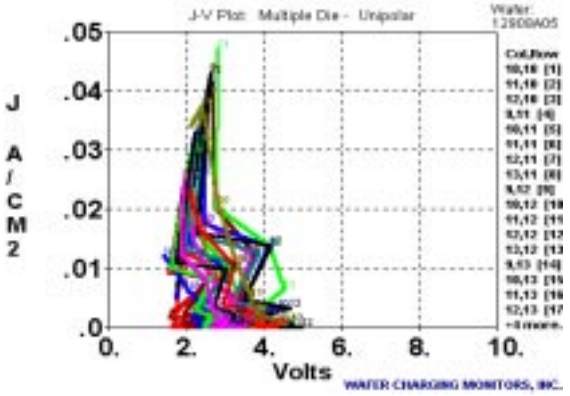

Figure 6. CHARM-2 positive J-V plots from die in the center of the wafer; unipolar charge-flux sensors; J-V plots shift to lower potentials, indicating that positive charging occurred at elevated temperature.

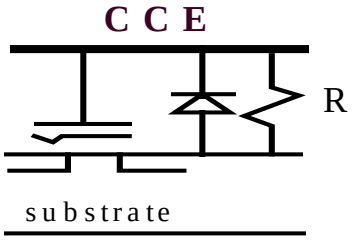

Figure 7. CHARM-2 unipolar positive charge-flux sensor: CCE = charge collection electrode; R = current sensing resistor.

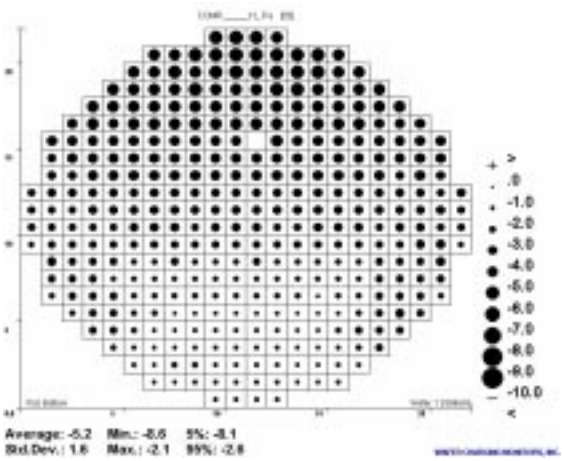

Figure 8. CHARM-2 negative potentials; oxide deposition.

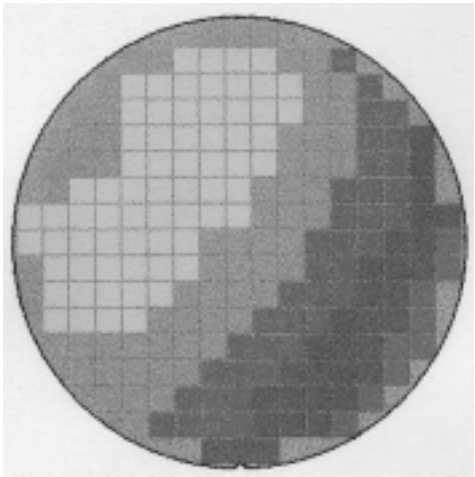

Figure 9. SPM negative potentials; oxide deposition with wafer rotated.

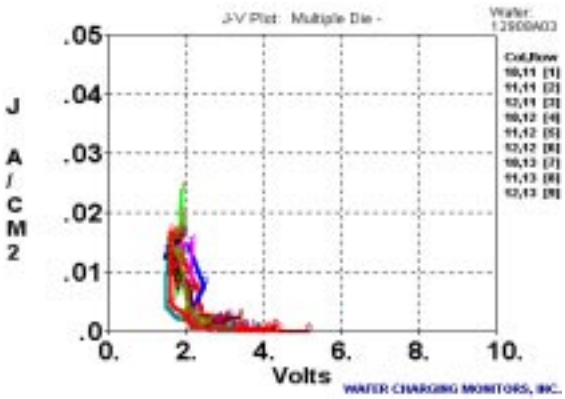

Figure 10. CHARM-2 positive J-V plots from die in the center of the wafer.