Research Journal of Recent Sciences _____ ISSN 2277-2502
Vol. **4(2),** 48-54, February **(2015)** *Res.J.Recent Sci.*

A Novel Hybrid Continuous Time / Discrete Time Multi Stage Noise Shaping Structure Dedicated to MEMS Based Accelerometer

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Available online at: www.isca.in, www.isca.me
Received 8th January 2014, revised 21st April 2014, accepted 25th June 2014

Abstract

A novel hybrid CT/DT delta sigma interface for micro electro mechanical accelerometer, which is located in the negative feedback, is presented in this article. The accelerometer with natural continuous time property is considered as the first stage of the modulator while a discrete time integrator is considered as the second stage of hybrid delta sigma to take the advantages of CT and DT delta sigma, simultaneously. The continuous time delta sigma modulator makes the use of inherent anti-aliasing filter and increased sampling frequency. While the discreet time delta sigma modulator benefits from the high accuracy of implementation. MATLAB simulation of the proposed hybrid delta sigma indicates the Signal to Noise plus Distortion Ratio (SNDR) of 114 dB over 1 KHz bandwidth when Over Sampling Ratio (OSR) is 256.

Keywords: Delta sigma modulator, mems, accelerometer, multi stage noise shaping (mash), hybrid continuous time /discreet time.

Introduction

Many applications such as inertial navigation, microgravity measurements in space, GPS-aided navigators etc. need high precision accelerometers with microgravity resolution, high sensitivity and high linearity[1]. Linearity in the inertial accelerometer can be defined as a small deflection of the proof of mass[2]. Displacement of the proof of mass can be reduced by placing the sensor in the close loop and as a result the performance of the sensor can be increased[3]. Since the sensing element presents a second order transfer function, it tempts the designer to utilize such an element as a loop filter in the delta sigma modulator structure to provide a digital output in high density CMOS technologies. Moreover, the problem of nonlinear electrostatic forces can be solved by placing in the feedback structure. However, the in-band quantization noise would be an important limitation and it dominates over the electronic noise due to this fact that micromechanical integrator works in very low dc gain at low frequencies.

Delta Sigma Modulator (DSM) is a widely used approach to implement high resolution analog to digital converter, which is able to increase the resolution of a low accuracy quantizer by applying two signal processing techniques, namely over sampling and noise shaping[4]. The quantization noise can be spread over a wide range of frequency by hiring the over sampling technique. Therefore, the in-band noise is diminished. Noise shaping technique can push the noise in the desired bandwidth to out of band of interest. The transparent consequence of these techniques is the reducing the noise and increasing the Effective Number of Bits (ENOB)[5]. It is worth mentioning that DSMs present unique advantages such as a compromise between dynamic range and bandwidth, insensitivity to circuit imperfections and programmability in digital domain[6]. DSMs suitable for micro electro mechanical systems (MEMs) have already been published in the literature. A systematic method to design of a feed forward (FF) delta sigma interface has been reported in which it was shown that the FF and feedback (FB) architectures have the same performance in terms SNDR when a pole and a zero is added to the feed forward path[7]. A single loop 4th order delta sigma interface circuit for closed loop micro machined accelerometer is presented by Dong Y et.al[8]. Micro machined sensing element accompanies with two electronic integrators make a 4th order low pass DSM. To reduce the input referred noise a switched capacitor (SC) charge integrator and correlated double sampling (CDS) were hired. The modulator presented the SNDR of 86.5 dB with over sampling ratio of 128. However this architecture suffers from low SNDR.A higher order noise shaping structure has been employed in Ref 1 to achieve higher SNDR. Although the fifth order modulator proposed by *Kauffman J. G. and et al.*, shows 100 dB SNDR, this topology is more susceptible to instability[2].

To overcome the aforementioned problems (low SNDR and instability problem) a hybrid CT/DT multi stage noise shaping (MASH) structure delta sigma modulator will be proposed in this article. The novelty of the proposed system lies in the fact that accelerometer located in the first stage as a 2nd order CT filter while, the second stage is implemented in Z domain. A compensation approach is applied to get the optimal noise transfer function. This paper is organized as follow. Section 2 introduces the design procedure. CT and DT design of the modulator will be explained in this section, as well. Main non-idealities in the second stage of the modulator will be investigated in the section 3. Section 4 dedicates to the

simulation results and finally conclusion is drawn in section 5.

Material and Methods

From the stand point of loop filter structure, DSMs are split into two categories: continuous time (CT) and discrete time (DT)[9]. Noise Transfer Function (NTF) is implemented in S-domain in CT-DSM while DT-DSM uses the Z-domain properties. CT and DT DSM have their pros and cons. For example CT-DSM benefits from inherent anti-aliasing filter characteristic as well as relaxed power consumption. However CT-DSMs suffer from clock jitter and Excess Loop Delay (ELD) severely[10]. DT-DSMs offer several advantages such as implementation of the analog coefficients just by the ration of two capacitors with good matching property and low sensitivity to clock jitter. Unfortunately, this kind of DSM suffers from higher bandwidth and slew rate requirements rather than CT counterpart.

There are two popular structures for the implementation of whole DSMs. Single stage and Multi Stage Noise Shaping (MASH) structure[4]. Although single loop structures present insensitivity to analog blocks and gain mismatch, they suffer from the stability problem so that the single loop structures with the order of 4 and more are susceptible to instability. To overcome this problem MASH structure DSM has been proposed in which it is possible to achieve higher order noise shaping by cascading many stages, as shown in figure-2. Although it is possible to cascade more than two stages, the quantization noise leakage caused by circuit imperfections can degrade the performance of the entire system.

Considering figure-2 the digital filters and modulator output can be expressed as follow:

$$H_1(z)=z^{-2}, H_2(z)=\frac{-1}{\hat{g}}(1-z^{-1})^2$$
$$Y(z)=z^{-4}X(z)+z^{-2}(1-z^{-1})^2(1-\frac{g}{\hat{g}})E_1(z)-\frac{1}{\hat{g}}(1-z^{-1})^4E_2(z) \quad (1)$$

Transparently, elimination of the first stage quantization noise can be achieved by proper matching of analog and digital coefficients i.e. g and $\hat{g}$. By taking the advantages of CT-DSM and DT-DSM, hybrid CT/DT DSM has been proposed to benefit from inherent anti-aliasing filter (the advantage of CT-DSM) and implementation with high accuracy (benefit of DT-DSM) simultaneously. The proposed micro electromechanical MASH structure illustrated in figure-1 is designed and simulated. To preserve the linearity as well as increasing the dynamic range of the system 1 and 3 bit quantizers are utilized in the first and second stages, respectively. For the first stage, the discrete time noise transfer function (DT-NTF) is opted as:

$$NTF_{first-stage}(z) = (1-z^{-1})^2 \quad (2)$$

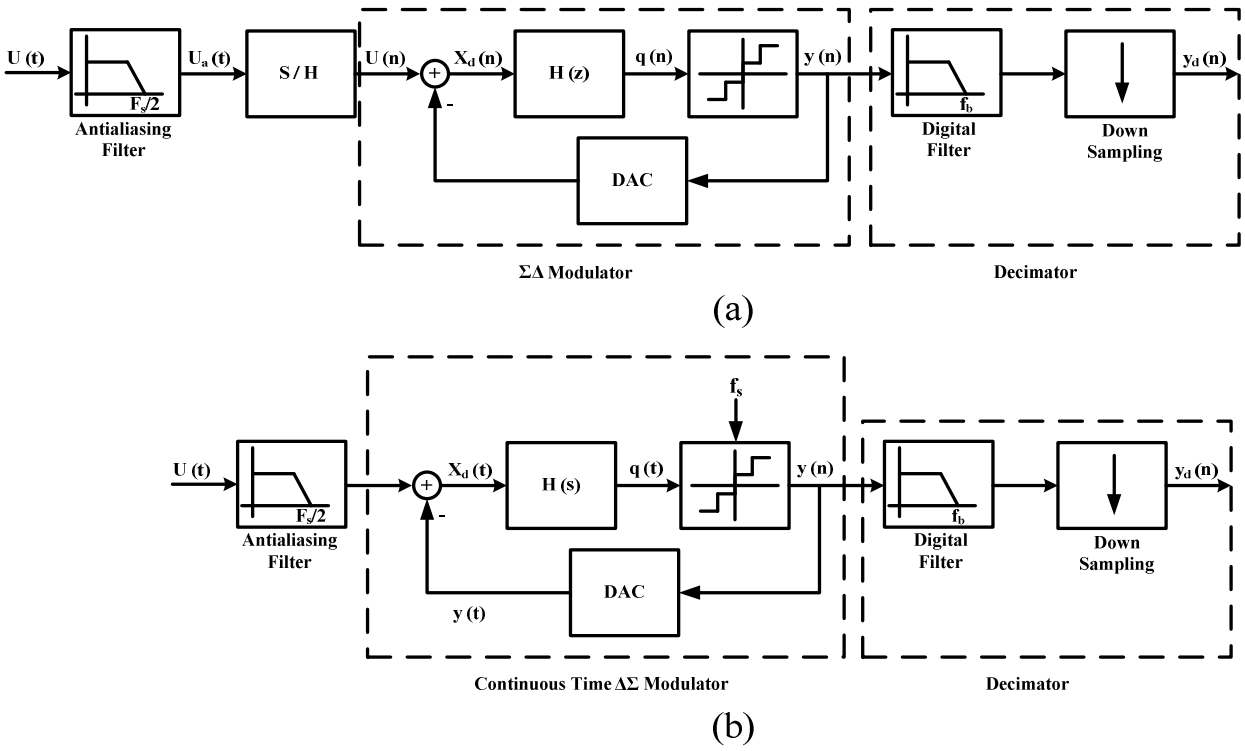


Figure-1
Delta sigma modulator topology (a) DT (b) CT

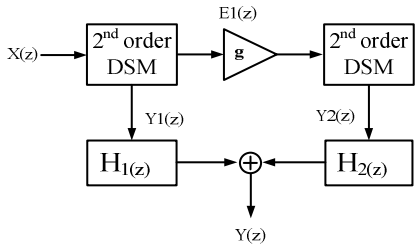


Figure-2
Multi stage noise shaping (MASH) structure DSM

However, it is necessary to map this discrete time transfer function to the Continuous time (CT) counterpart. The method used by Schreier R[11] is hired to do this transformation. The idea is that to convert discrete time transfer function to CT counterpart so that the modulator presents the same performance in terms of output spectrum as well as dynamic range. Another matter, which must be considered in DT to CT conversion procedure, is proper selecting of feedback DAC pulse shape to preserve the modulator against jitter error. Although, the use of a decaying waveform minimizes the jitter influences, the power consumption of the whole system will increase severely. Therefore, the non-return-to-zero (NRZ) DAC shape is utilized to have a low power design and reasonable jitter tolerance, as well[12-13]. Although, increasing the number of quantizer bit can reduce the clock jitter sensitivity, 1 bit quantizer is preferred to preserve the linearity in the first stage[11].

$$IBN_{\sigma_t} = \frac{V_{FS}^2}{(2^{B_{\text{int}}}-1)^2}\left(\frac{\sigma_t}{T_s}\right)^2 \frac{A_{NRZ,MB}}{OSR} \quad (3)$$

A second order feedback from (FB) structure is selected for implementation of the second stage of micro electromechanical MASH structure. Feedback structure is proffered due to two main reasons. First, controlling the signal transfer function (STF) is easier than the feed forward (FF) structure. Second, feed forward structure suffers from a big adder before the quantizer, unlike the Feedback structure. Moreover, a local feedback is considered to create a zero in the NTF and as a result increasing the performance in terms of Signal to Noise + distortion Ratio (SNDR). Regarding the $NTF_{2nd\text{-}stage}$ (z) as follow:

$$NTF_{2nd-stage} = 1-(2-g)z^{-1}+z^{-2} \quad (4)$$

Regarding the linear model for the quantizer, the z-domain output transfer function can be expressed as shown in Equation-5:

$$\begin{aligned} Y(z) &= X(z) - E2(z)\frac{NTF_{2nd-stage}(z) - NTF_{1st-stage}(z)}{d} \\ &= X(z) - E2(z)\frac{(1-z^{-1})^2 - 1 - (2-g)z^{-1}+z^{-2}}{d} \end{aligned} \quad (5)$$

In which, X (z) is the input signal and E_2 (z) is the quantization noise of the second stage of the modulator. The local feedback parameter, g presents a pair of complex conjugate zero in the overall NTF by maximizing the SNDR through the following equation:

$$g_{optimum} = \arg \min_{g} \int_0^{\frac{f_s}{2OSR}} \left|(1-z^{-1})^2 - 1 - (2-g)z^{-1}+z^{-2}\right|^2 df \quad (6)$$

Regarding $z = e^{j\theta}$ and $\theta = \frac{2\pi f}{f_s}$ the optimal value for local feedback coefficient can be extracted as shown in Equation-7:

$$g_{optimum} = \frac{2\sin(\frac{3\pi}{OSR}) - 18\sin(\frac{2\pi}{OSR}) + 90\sin(\frac{\pi}{OSR}) - (\frac{60\pi}{OSR})}{24\sin(\frac{\pi}{OSR}) - 3\sin(\frac{2\pi}{OSR}) - (\frac{18\pi}{OSR})} \quad (7)$$

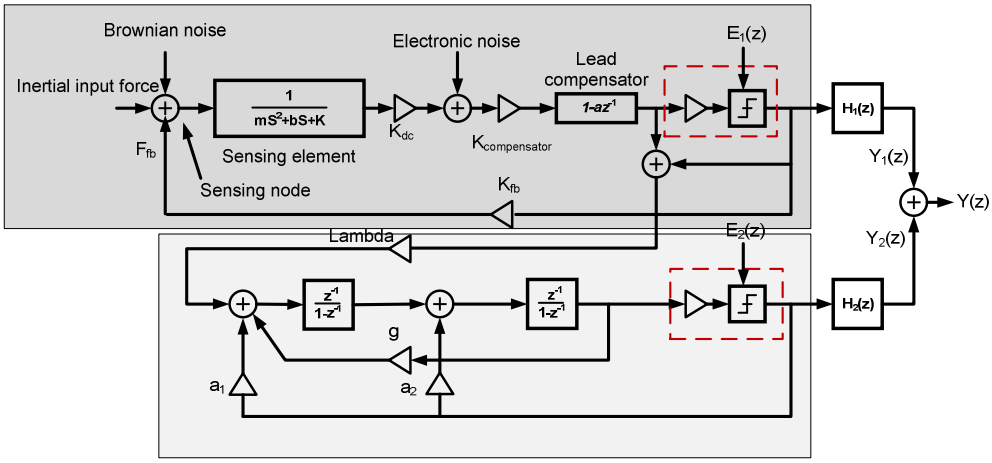


Figure-3
Proposed hybrid CT/DT MASH structure DSM

Results and Discussion

To prove the effectiveness of the proposed delta sigma modulator, several behavioral simulations in MATLAB/SIMULIK environment are provided. The over sampling ratio was assumed 256 in all simulation. The input signal band width is 1 kHz and as a result the sampling frequency would be 512 KHz. Investigating the main non-idealities in the second stage of the proposed modulator plays a crucial role in the performance of entire system. Practically, the modulator suffers from finite DC gain of integrators due to circuit constrains. In other words, the finite DC-gain of the integrators can move the poles of the noise transfer function outside the unit circle. As a consequence, the modulator tends to be instable. The SNDR of the modulator as a function of finite DC-gain is depicted in figure-4.According to this figure, the op-amp used in the second stage must handle the minimum gain of 40 dB to avoid the SNDR degradation.

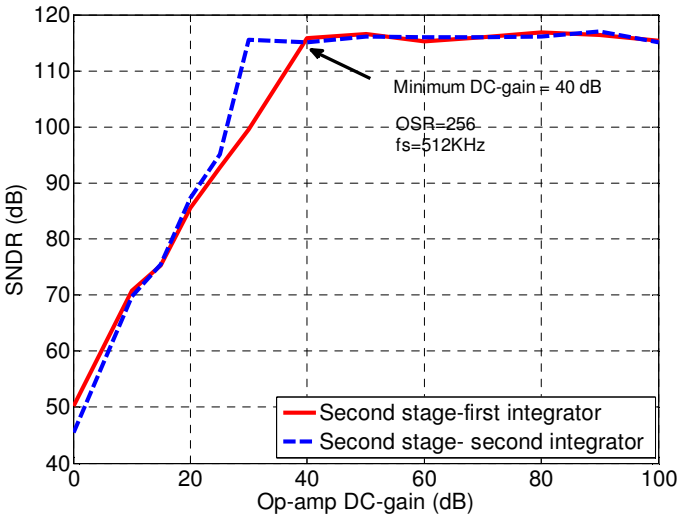


Figure-4

SNDR as a function of op-amp DC-gain for the second stage of the modulator

Incomplete charge transfer to the output of the integrator at the end of the integration period produces a non-ideality which is called the finite Gain Bandwidth (GBW) of the op-amp. The main drawback of this effect is reducing the performance of the modulator in terms of SNDR. On the other hand, Rate (SR) has the same effects on the performance of the DSM. To investigate how theses imperfections reduce the performance of the modulator, a user defined function is utilized as expressed inEq. (8). Simulation results show that the operational trance-conductance amplifier with 2.2 MHz GBW and at least 35 V/µs must be used to preserve the SNDR requirement.

To avoid the saturation of the integrators a coefficients scaling must be performed. By this scaling, preserving a high dynamic range can be guaranteed.

$$|\varepsilon| = \begin{cases} |V_{in}| - SR * \frac{T_s}{2} & t_{SL} \geq \frac{T_s}{2} \quad \left|\frac{\partial V_{in}}{\partial t}\right| t=0 > SR \\ (|V_{in}| - SR * t_{SL}) * e^{\frac{-t}{\tau}} & t_{SL} < \frac{T_s}{2} \\ |V_{in}| * e^{\frac{-t}{\tau}} & \left|\frac{\partial V_{in}}{\partial t}\right| t=0 < SR \end{cases} \quad (8)$$

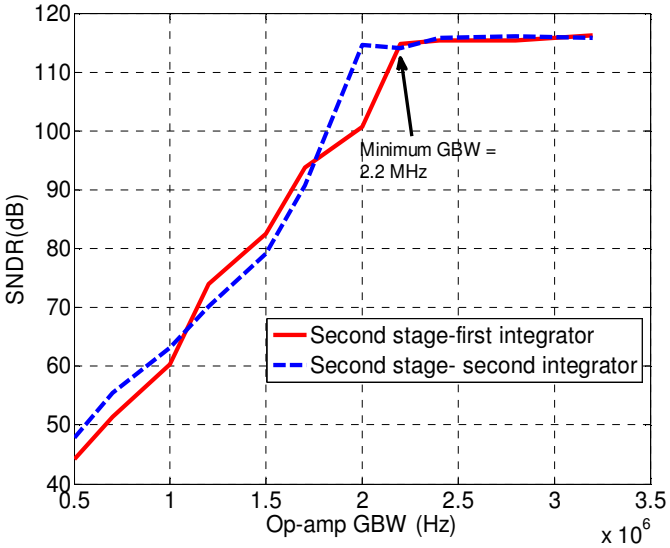


Figure-5

SNDR as a function of op-amp GBW for the second stage of the modulator

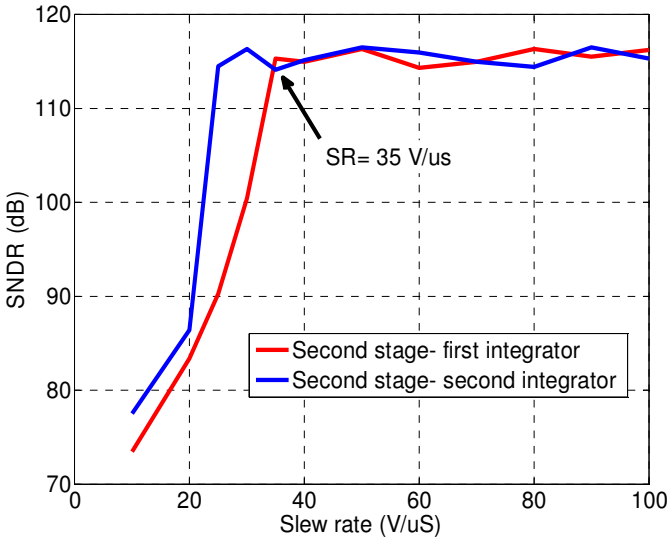


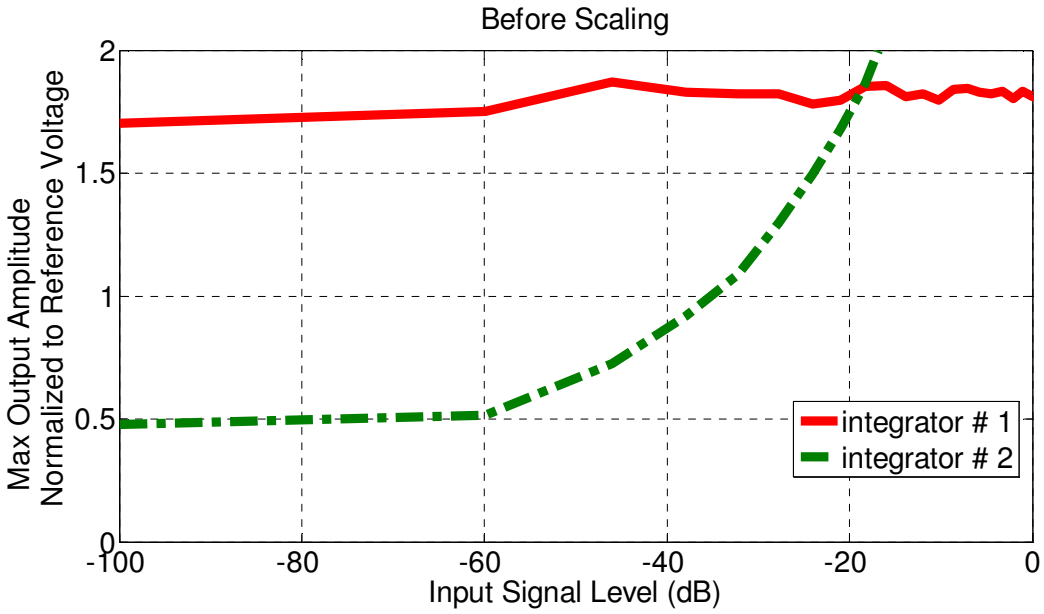
Figure-6

SNDR as a function of op-amp slew rate for the second stage of the modulator

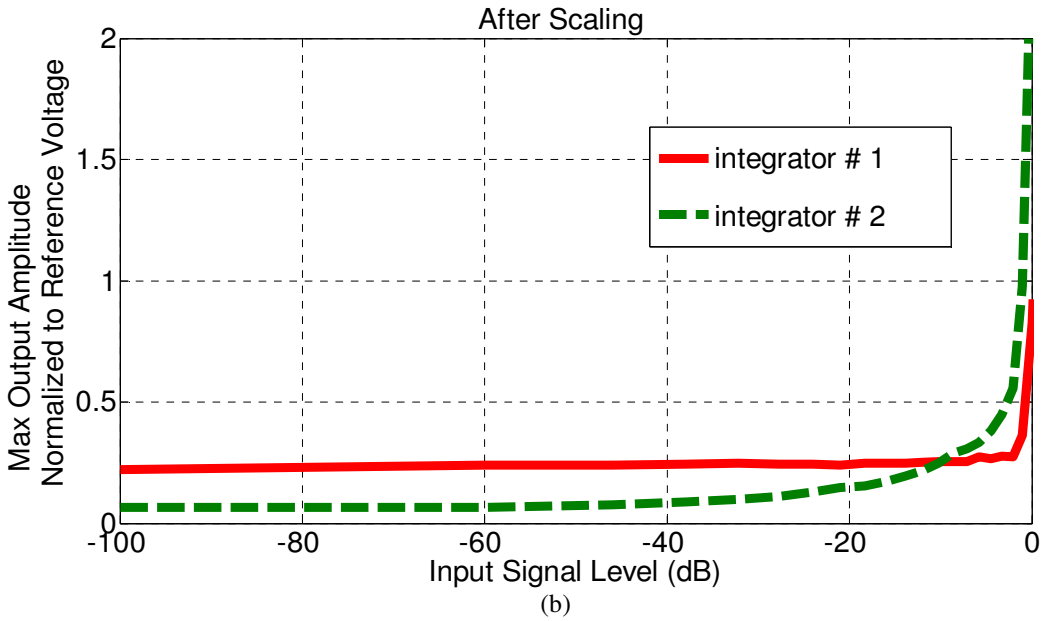
Figure-7 shows the integrators output of the second stage before

and after coefficient scaling. As can be seen from figure-7(a) the first integrator has a high output which is not tolerable for current technology and second integrator is saturated for -40 dB input signal. This results the degradation in dynamic range of the modulator. While figure-7(b) illustrates that the first and second integrators have a reasonable output swing as well as reasonable saturation level.

The proposed hybrid MEMS-DSM is simulated in MATLAB/SIMULINK environment. The simulation results indicate that the hybrid MEMS-DSM SNDR is 115 dB when the OSR is 256, which is utterly comparable with state of the art MEMS-DSM. Figure-8 depicts the power spectral density of the proposed modulator when the input frequency is 496.09 Hz for 2^{16} FFT point[14]. Figure-9 presents the simulated SNDR versus input signal amplitude. Simulation results show a peak SNDR of 115.23 dB@-3dBFS. The overall performance of the proposed hybrid CT/DT-DSM is summarized in table-1.



(a)



(b)

Figure-7

Maximum output amplitude of the integrators versus input level signal

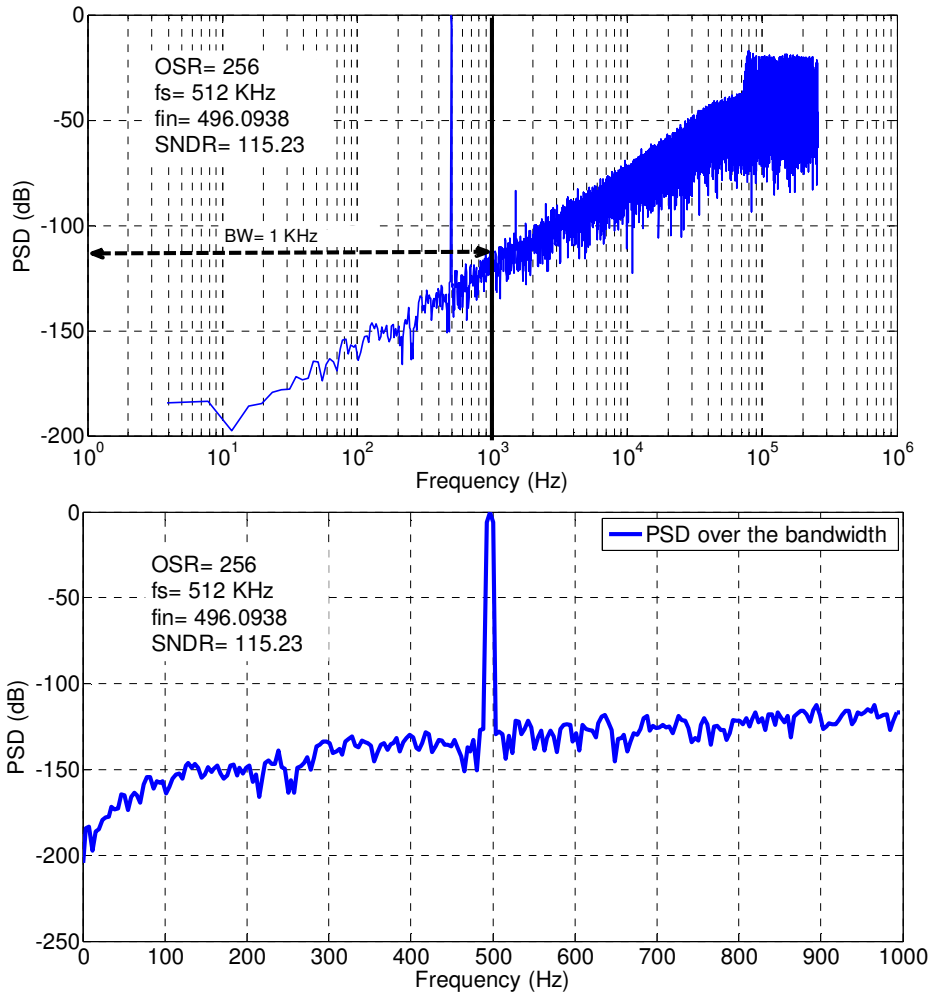


Figure-8
Power spectral density of the proposed modulator

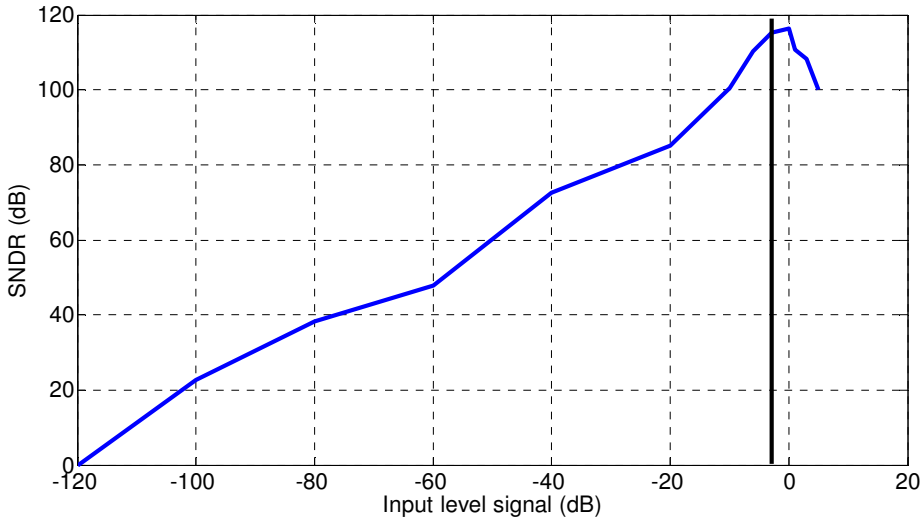


Figure-9
Dynamic range of the modulator

Table-1
Overall performance of the proposed hybrid CT/DT-DSM comparison with state of the art

Reference	2	7	8	This work
Structure	Feedback form 4^{th} order	Feed forward form3^{rd} order	Feedback form 4^{th} order	MASH structure
OSR	256	128	128	256
Signal bandwidth (kHz)	1	1.024	1	1
Sampling frequency (KHz)	512	262.144	256	512
SNDR (dB)	105	89.2	86.5	115.23
DR (dB)	LPDSM : 80 BPDSM : 100	-	-	117

Conclusion

A novel hybrid CT/DT MASH structure suitable for closed-loop micro machined accelerometer has been proposed in this article. The first stage makes use of the CT version of delta sigma modulator and the second stage is implemented as a 2^{nd} order DT-DSM. One bit quantizer is used in the first stage to preserve the linearity while 3-bit internal ADC is used in the second stage to increase the SNDR of the modulator as well as DR. A local feedback is applied to the modulator to increase the SNDR without wasting more power. Based on simulation results the modulator has a high DR while the stability is preserved without using higher order modulator.

Acknowledgement

The authors would like to thank Ahar Branch, Islamic Azad University for the financial support of this research.

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