Self-Repairing SRAM for Reducing Parametric Failures in Nanoscaled Memory

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Abstract- *We present a self-repairing SRAM to reduce parametric failures using an on-chip leakage sensor and application of proper body bias. Simulations in a predictive 70nm technology show 5-40% (depending on inter-die Vt variation) improvement in SRAM yield. A test-chip is fabricated and measured in 0.13µm CMOS to demonstrate operation of the self-repair system.*

Introduction

Large inter-die and intra-die variations in process parameters can result in large number of parametric failures in nanoscaled SRAM, thereby, degrading yield [1-2]. In this paper, we present a self-repairing SRAM to reduce parametric failures in memory. In the proposed technique, a self-repair system detects the inter-die process corner of an SRAM die using an on-chip leakage sensor and selects the proper body bias to reduce parametric failures. A test-chip is implemented in IBM 0.13µm CMOS technology to demonstrate the self-repair operation.

Parametric Failures and Self-Repair of SRAM

Within-die Vt variation due to random dopant fluctuations results in parametric failures (access, read, write and hold failures) in SRAM cells [2]. Inter-die shift in Vt can amplify the effect of random variation. At low inter-die Vt corners read (lower static noise margin) and hold (higher leakage) failures are more probable. At high inter-die Vt corners more write and access failures (reduction in the current of access transistors) are expected [2] (Fig. 1a, simulations using predictive 70nm devices [3]). At nominal Vt corner (region B, Fig, 1a), low cell failure probability makes memory failure very unlikely as most of the faulty cells can be replaced using redundancy. However, SRAM dies with negative and positive inter-die Vt shifts larger than a certain level are very likely to fail (high memory failure probability, Fig. 1a). Reducing read/hold failures in the dies at low-Vt corners (region A) and access/write failures in the dies at high-Vt corners (region C) can improve yield (shifts the dies from region A and C to region B). This can be achieved by applying Forward Body Bias (FBB) to high-Vt dies in region C and Reverse Body Bias (RBB) to low-Vt dies in region A. Fig. 1b shows that FBB reduces access/write failures and RBB reduces read/hold failures [2]. Based on above observations, we propose a self-repair technique for SRAM (Fig. 2). Inter-die Vt corner of an SRAM die is detected by monitoring (using an on-chip leakage sensor) the entire array (composed of a large number of cells) leakage and proper body bias is applied to reduce failures. The changes in the leakage of individual cells due to random within-die Vt variation tend to cancels each other. Hence, array leakage is a reliable indicator of the inter-die Vt corner even under intra-die Vt variation [2]. The proposed self-repair scheme reduces inter-die Vt shift of a die (not intra-die variation) using body bias. This greatly decreases dominant types of failure mechanisms in that die, resulting in less number of total parametric failures.

Implementation and Measurements of Test-Chip

The proposed self-repairing SRAM is implemented in IBM 0.13µm CMOS (dual-Vt & triple-well) technology (Fig. 2). Two 64KB SRAMs are implemented to emulate inter-die variations: one using low-Vt (representing extreme negative inter-die Vt shift) and the other using high-Vt (representing extreme positive inter-die Vt shift) devices. The on-chip leakage sensor (current mirror with active load, Fig. 3) is designed in series with the cell supply (not with pre-charge circuit) to monitor the array leakage. Large and distributed PMOS diodes are used in the current mirror to reduce the effect of within-die variability (~0.01% area overhead). The sensor output increases with array leakage and is compared against on-chip (or off-chip) reference voltages (representing low, nominal and high inter-die Vt corners) to apply proper body-bias (generated on/off chip). Level converters in the body-bias selection circuit (Fig. 4) convert logic "0" to the RBB value to prevent conduction through the 'off' NMOS transistors of pass gates connected to RBB voltage. The pass-gate devices are designed with thicker T_{ox} to prevent oxide breakdown when Vg='1' and Vs=RBB. The leakage monitors are bypassed (by switching "Calibrate" high-to-low) during regular operation using large PMOS devices (Fig. 2, ~5% area overhead). Access time is not impacted by the bypass PMOS as it is determined by the discharging current through access/pull-down NMOS.

The leakage sensor output (Vout) in the proposed scheme needs to have low sensitivity to (a) inter-die Vt shift in the sensor transistors, and (b) change in temperature (T). With a diode connected NMOS load (Fig. 3a) positive inter-die Vt shift of the diode at the high-Vt corner increases Vout. This reduces the difference in Vout between low and high-Vt corners ('Conv. Design' in Fig. 5). Also, due to exponential dependence of array leakage on T, Vout for a high-Vt die at high T can be comparable to that of a low-Vt die at low-T (Fig. 5). To solve this problem we used active NMOS load with variable bias (Fig. 3b). The bias generator circuit is designed such that, the bias increases with T and inter-die Vt shift of sensor transistors (with M_{T1}, M_{T2} and M_D in Fig. 3b, $V_{BIAS} \sim kT\ln(W_{T1}/W_{T2}) + Vt_{MD}$). This reduces the resistance of the NMOS load at higher T (lower sensitivity of Vout to T) and higher inter-die Vt (compensates the Vt increase of NMOS load). The transistors M1-M9 are designed to ensure a larger current through M_{T1}-M_{T2}-M_D at low-Vt corner compared to high-Vt corner. This increases V_{BIAS} at a faster rate with T for low-Vt cases to compensate the higher temperature sensitivity of array leakage at low-Vt corner. Simulations in 0.13µm technology show that, the proposed sensor reduces the output sensitivity to temperature, inter-die and intra-die Vt variation of sensor transistors (Fig. 5). The leakage sensor is designed to have Vout~1.4V for low-Vt array and Vout~0V for high-Vt array (V_{DD}=1.5V). Measured value of Vout from the sensor monitoring the low-Vt array leakage is close to 1.4V (within ~5% of the simulated value) (Fig. 3c, array leakage is modified using source-bias). To represent equal inter-die Vt shift the array and the sensor are designed with same types of devices (i.e. the sensor for low-Vt array is designed with low-Vt devices). As "Calibrate" switches from "high" to "low" during regular operation, the supply of the sensor is gated to minimize its static power dissipation.

The on-chip reference voltages (0.5V and 1V) are designed to have a small positive temperature coefficient (similar to Vout, realized using NMOS M_{T1} and M_{T2}) and low sensitivity to inter-die Vt shift (Fig. 6). Measured values of the reference voltage show low sensitivity to supply variation (Fig. 6c) and to Vt shift (changed using body-bias) of the transistors (Fig. 6d). Measured FBB (+0.5V) and RBB (-0.5V) values from on-chip bias generators (reference generators followed by op-amps [4]) show good stability against supply and chip-to-chip variation (Fig. 7). The high-activity row and column driver circuits are designed in the isolated p-well to minimize body current fluctuation. Moreover, sharp transition at the region boundary in Fig. 1a suggests that a small change in Vt can shift a large number of dies from region A and C to region B. Also, width of region B makes shifting of dies from region A to C very unlikely. This suggests that, stability requirement of the generated body bias is not very stringent. Measurement results from different chips show that the sensor output from low-Vt array is higher than the reference voltages (Fig. 8), which indicates that the self-repair system can apply proper body bias. Fig. 9 shows the successful transition of body voltage with selection of FBB and RBB (measured waveform).

Measurement of an SRAM cell shows that, FBB increases read and write currents which indicate lower access and write failures. RBB reduces the read voltage (i.e. voltage rise at node storing "0" while reading) which indicates a better read stability (Fig. 10a). Simulation in 0.13µm technology shows that the self-repair technique can reduce parametric failures at different inter-die corners (Fig. 10b). Simulations using 70nm devices [3] shows possibility of significant (5-40%, depending on the amount of inter-die Vt variation) improvement in design yield (Fig. 10c).

Conclusions

We presented a self-repairing SRAM to reduce parametric failures in memory. In the proposed scheme global inter-die variation is detected and corrected to reduce the effect of local within-die random variation. The proposed self-repair technique will help to improve SRAM yield under process variation in nanometer nodes.

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Reference

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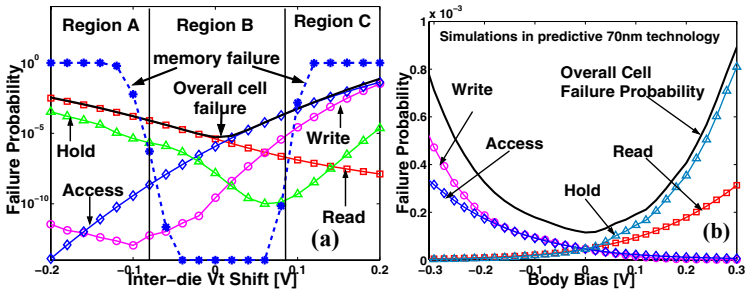

Fig. 1: Effect of (a) inter-die Vt, (b) body bias on SRAM failures; Simulation in predictive 70nm technology.

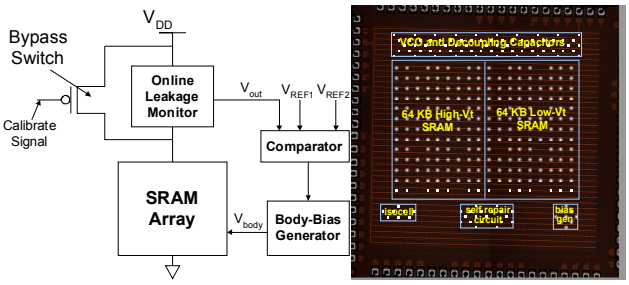

Fig. 2: self-repairing SRAM scheme and die-photo.

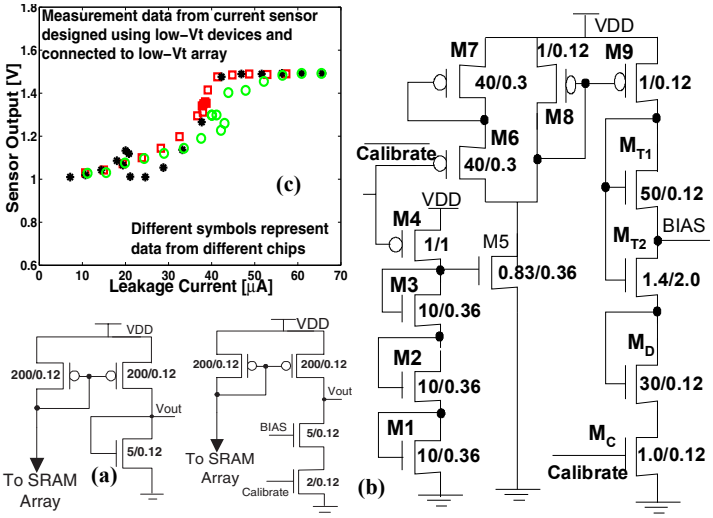

Fig. 3: Leakage sensor (a) conventional, (b) proposed (c) measured output.

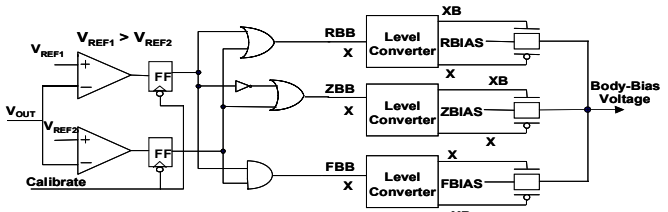

Fig. 4: Body-bias selection logic

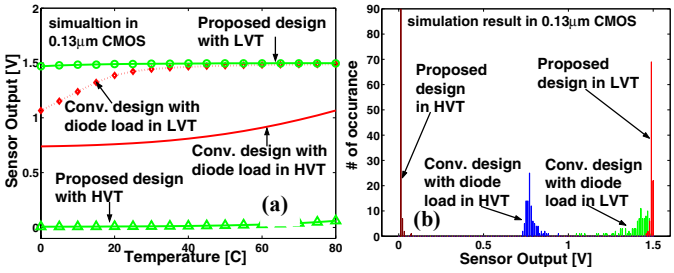

Fig. 5: Leakage sensor o/p with (a) temp. and (b) intra-die variation

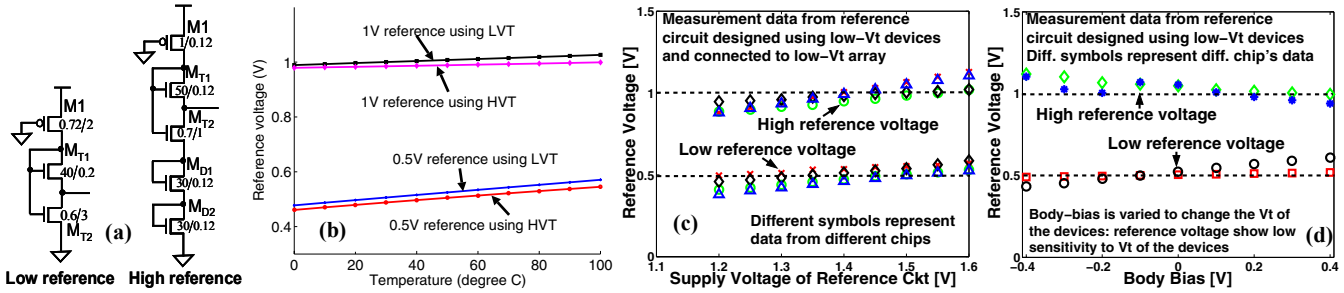

Fig. 6: (a) Reference generation circuit, (b) effect of temperature, measured reference voltage with (c) supply (d) body bias variation.

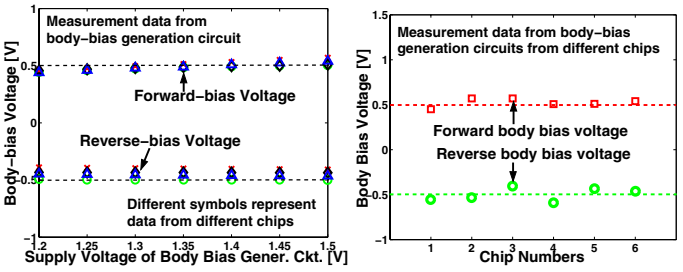

Fig. 7: Measured body-bias voltage for different chips

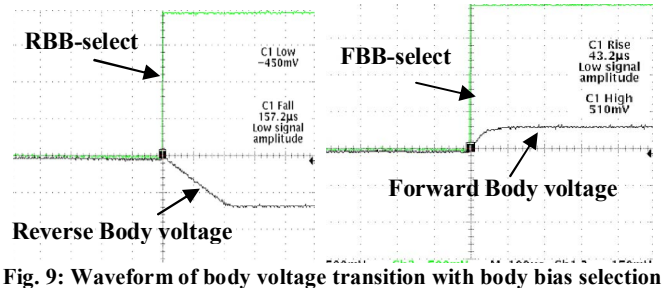

Fig. 9: Waveform of body voltage transition with body bias selection

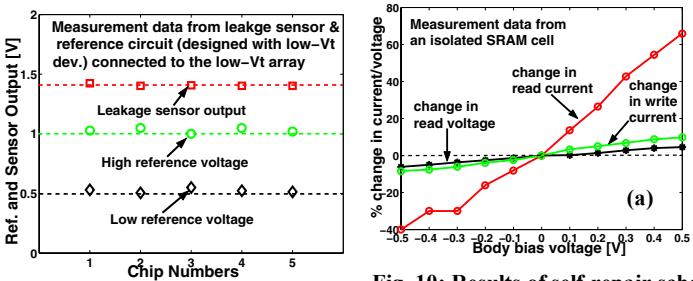

Fig. 8: Measured sensor o/p & reference voltage for diff. chips

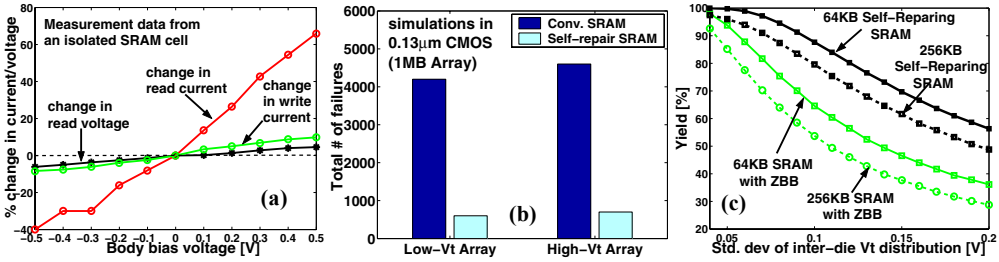

Fig. 10: Results of self-repair scheme: (a) measurement of single SRAM cell, (b) reduction of parametric failures (simulation in 0.13µm), and (c) yield enhancement (simulation in predictive 70nm).