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Back-Side Wafer Grinding Quality Affecting Back-End Assembly Process for LCD Driver ICs

Mu-Chun Wang[*,1], Zhen-Ying Hsieh [1], Kuo-Shu Huang [*,2], Shuang-Yuan Chen[1], Heng-Sheng Huang[1]

[1]Graduate Institute of Mechatronic Engineering, National Taipei University of Technology
No. 1, Sec. 3, Chung-Hsiao E. Rd., Taipei, Taiwan, R.O.C.
[2]Generalplus Technology Inc.
3F, No.8, Dusing Rd., Hsinchu Science Park, Hsinchu City 30078, Taiwan, R.O.C.
[*]Dept. of Electronic Engineering, Ming Hsin University of Science & Technology
No. 1 Hsin-Hsing Road, Hsin-Fong, Hsin-Chu, Taiwan, R.O.C.
[*]Tel.: 886-3-559-3142, FAX: 886-3-559-1402, E-mail: mucwang@must.edu.tw

ABSTRACT

Die size and thickness of IC substrate typically vary as a result of the various market demands while the semiconductor process and the product applications develop fast. In order to satisfy the market concerns, the improvement of wafer grinding and dicing saw technology is necessary to provide lighter, thinner and more reliable ICs. Generally, most of previous commercial ICs almost demonstrate the square profile, but some special applications such as liquid-crystal-display (LCD) driver ICs request approximate rectangle shape. Furthermore, the ratios of length / width of these drivers are near 14:1, therefore, it is easy to be broken during IC assembly process and induce some reliability defects. However, the growth rate of digital panel displays is gradually increased. This global market is more and more impressed.

In this study, how to promote the die strength and investigate the wafer grinding process for the previous LCD products is the main target. Through the analysis of data collection in die sizes, the suitable wafer grinding process is recommended in assembly line and some predictable trends for future panel IC applications are also exposed.

1. Introduction

Each of assembly industries pays a lot of efforts to extract optimal parameters on IC process technology that improving IC reliability and reducing IC cost. Because of the promotion of package equipments and related package materials, these two objectives have some chance to be implemented. To reduce the package cost, especially in lifetime and cost of diamond blade and throughput consideration, the dicing saw wafers will be ground at the back side to obtain the thinner thickness, such as ≤ 381 μm (= 15 mils). To effectively seek the aspect of assembly line yield more, we start to analyze the influence of IC die sizes on different grinding processes. In typical back-side wafer grinding, the first step, coarse grind, is adopted. Then, the second step, fine grind, is continuously applied to satisfy the reserved target. Basically, the fine grind only and slightly contributes the suffering of wafer thickness, such as 20 μm.

In the following, the water clean process will be employed to eliminate the silicon powder on ground wafer. In this grinding process, the main impact factors include the specifications of grinding wheels inside containing tiny diamond grains as abrasion, the amount of cooling water, the flushing angle, the category of protective tape for top-side wafer, and the grinding speed. Better controlling these factors, and better grinding quality. This quality significantly affects the assembly yield, especially in LCD driver ICs.

For LCD driving ICs, the reliability and the assembly yield are seriously attacked in assembly processes because of their rectangle shapes. The chip size and category of driver ICs are presented in Fig. 1. The unit for the ruler is centimeter (cm). The common package categories for LCD drivers are tape-carrier-package

(TCP), chip-on-film (COF) and chip-on-glass (COG). For current middle-and-short display panels, the COG package [1] is widely adopted.

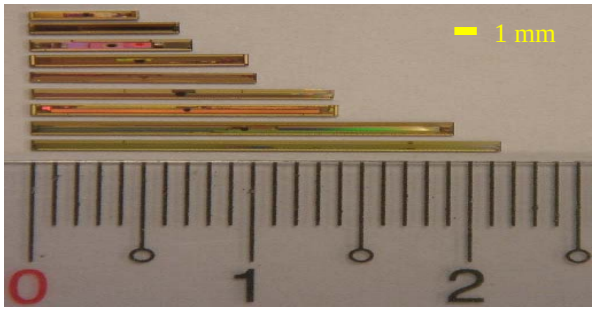


Fig. 1. Die sizes and categories of LCD driver ICs with a cm ruler.

Based on the improvement of package process, the pad pitch of driving ICs is continuously shorted. In the meantime, the chip size of driver ICs is not only shrunk, but also frequently changed. The technology roadmap summarized from numerous worldwide LCD-driver design houses is presented in Fig. 2 [2].

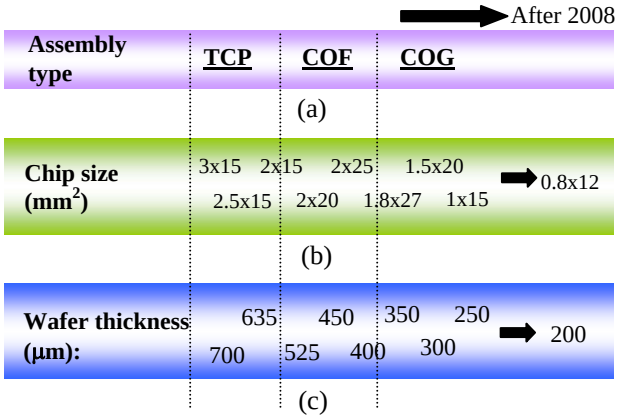


Fig. 2. Corresponding trend chart for assembly types, chip sizes and wafer thicknesses.

2. Experimental arrangement

According to the experimental design for grinding process parameters, chip sizes and wafer thicknesses, the optimal grinding quality and the low-cost assembly for IC design houses and assembly houses will be reached. In the following, these splitting variables will be investigated.

A. Split I: Chip Size

The die size is shrunk continuously from (width * length =) 3*15 to 1*15 mm^2 to satisfy the display panel requirement. The future die size will be 0.8*12 mm^2, as shown in Fig. 2(b). The distance of gold bump, no doubt, is decreased and turns into another challenge in assembly at one time. This is one of reasons to affect the strain tolerance of die sizes.

B. Split II: Wafer Thickness

The required wafer thickness is one of the critical factors to constrain the development of ultra-thin IC packaging. However, larger wafer diameter and thinner wafer thickness reveal the strict challenge on IC assembly, such as a 12" wafer and a thin thickness of wafer 200 μm or below.

C. Split III: Grinding Process

Using two sets of 8" wafer thicknesses, 200 and 300 μm, as the experimental samples, the first set in the final fine-grinding is with the grinding wheel inside, as shown in Fig. 3. The second set is with polishing method. This polishing method means that the wafer is ground with grinding pad plus slurry, pressing on wafer. The grinding pressure is about 157 kg/cm^2. This ground wafer presents a smooth mirror-like backside. The stress residue is simultaneously removed. If the fine grind with grinding wheel is applied, some residual tracks due to stress will be observed.

Fig. 3. Photo of grinding arrangement [3].

3. Measurement metrology

After wafer grinding, the sufficient strength of chips on wafer is necessary for the other backend assembly processes. Therefore, these ground chips should be tested. The test metrology is that the tested chip is placed on the break test machine, as shown in Fig. 4 [4].

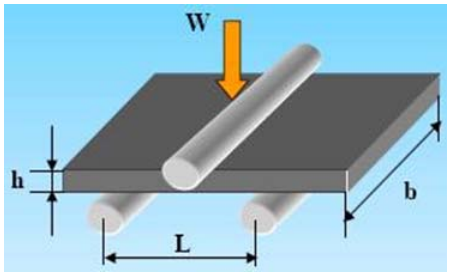


Fig. 4. Schematic of break testing structure [4].

Next, the breaking load data will be achieved. The contour feature size of a chip can be easily measured.

The span L between two metal rolls is also obtained by break instrument adjustment. The chip strength δ [Mpa] [5-8] can be expressed as

$$\delta = \frac{3LW}{2bh^2} \quad (1)$$

where W: breaking load [Nt], L: span [mm], b: chip width (mm), and h: chip thickness [mm].

4. Results and Discussion

In the experiment, there are 9 chip sizes, two wafer thicknesses, two fine grinding methods. The total grinding results are 36. Furthermore, if the backside of grinding wafer is ground downwards, this method is easier to break the wafer, comparing it upwards. If the fine grinding adopts the grinding wheel, the vein curves exist, as shown in Fig. 5. The distribution of vein curves is scattered from the center toward outside. Hence, each chip at the back side exhibits the vertical, horizontal, or oblique vein curves.

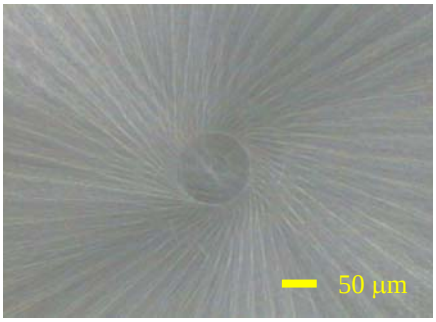


Fig. 5. Zoom-in for central vein curves of fine grinding process.

Again, the most fragile case is that the long side of IC chip is perpendicular to the vein curve. In the experiment, the total test results should demonstrate 144 types. Here, we chose the worst case, top-side wafer downwards and perpendicular case, to study the relationship of breaking load and chip strength between grinding methods and chip sizes, as shown in Fig.6-9. The chosen die sizes were 0.8*12, 1*15, 1.5*20, 1.8*27, 2*15, 2*20, 2*25, 2.5*15 and 3*15 mm^2. The ground wafer thicknesses were 200 μm and 300 μm. The fine grinding methods were with grinding wheel and polishing.

From Fig. 6 to Fig. 9, breaking load and die strength are presented with 200 μm and 300 μm wafer thicknesses. The x-axis in these figures is labelled as die sizes, and the y-axis contains pink and green-dash pillars, labelled as grinding-wheel grinding and polishing after fine grind, respectively. Each data set in these four figures was averaged with 5-test-point. In Fig. 6, the test magnitude of breaking load with polishing method is always higher than that with grinding wheel. The endurance capability of the previous can be over two times to the last, especially at the small die size. However, the die strength after calculation only shows the better improvement in small die size, as presented in Fig. 7.

In the meantime, not only is the endurance of breaking load with polishing, as presented in Fig. 8, greater than that with the other, but also the die strength with polishing is obviously greater than that with the other, as shown in Fig. 9. In addition, the wafer thickness really contributes the variation of die strength [9]. Thicker wafer depicts better die strength.

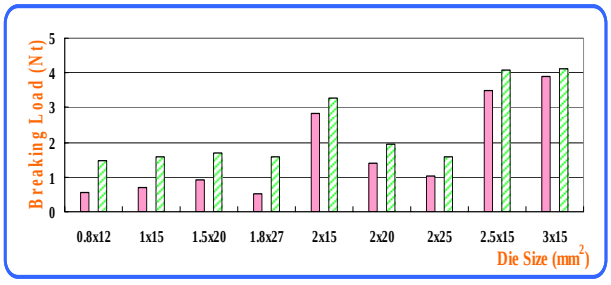


Fig. 6. Breaking load W with 200 μm wafer thickness.

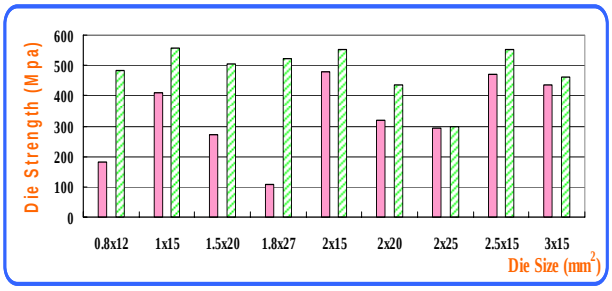


Fig. 7. Die strength δ with 200 μm wafer thickness.

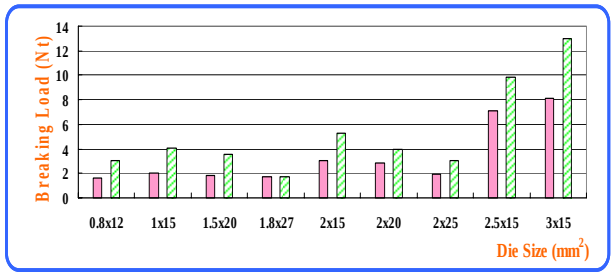


Fig. 8. Breaking load W with 300 μm wafer thickness.

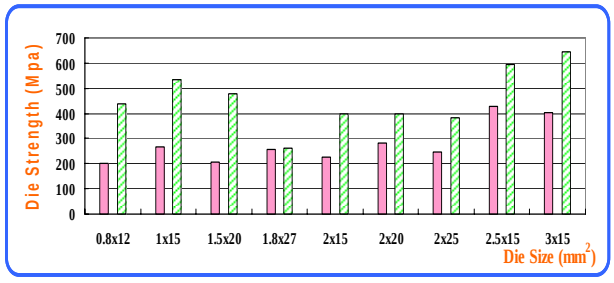
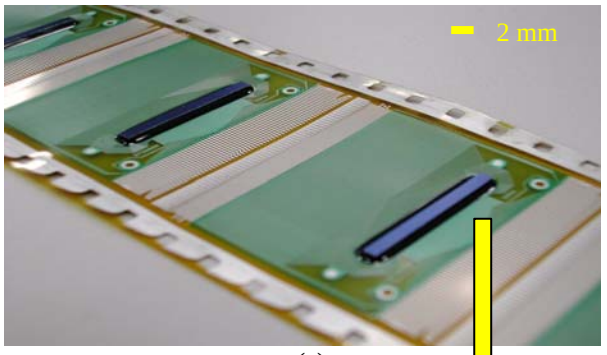


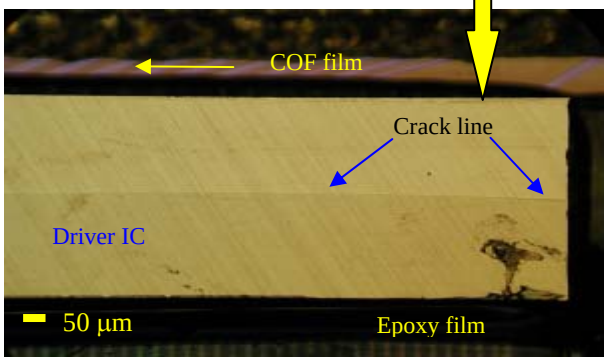
Fig. 9. Die strength δ with 300 μm wafer thickness.

In total, the priority of die strength in this experiment can be classified as polishing @ 300 μm, fine grinding @ 300 μm, polishing @ 200 μm, and fine grinding @ 200 μm, as presented in Fig. 10. Again, the thickness of recent driver ICs for middle-or-small display panels is chiefly ground at 300 μm. At the same time, the fine grinding process is currently adopted to reduce the assembly cost. However, after inner lead bonding (ILB) process on display panel, a crack line locating at the long side or the center of the short side of a chip frequently appears, as presented in Fig. 11. If this phenomenon usually occurs, the entire assembly yield will be decreased. Relatively, the whole product cost in LCD products is also increased.

Fig. 10. Die strength vs. back-side wafer grinding processes.



(a)



(b)

Fig. 11. Top view of COF package (a) drivers on LCD panel (b) a crack line on driver IC after ILB process.

5. Conclusion

From the experimental data, die sizes plus different grinding methods indeed affect the breaking load and the die strength in LCD driver ICs. According to these data, the best breaking load is with the biggest die size, 3 ∗ 15 mm^2 under thicker wafer thickness 300 μm. However, the bigger chip area will show the lower marketing competition. Selecting a suitable die size under a desired wafer thickness is a good challenge for LCD IC designers. At the same time, the adequate grinding method truly influences the die strength after ILB process. The assembly houses need investigate the better grinding method to ensure the chip strength and stabilize the assembly yield.

For instance, using the suitable grinding wheel [10] to reduce the variable cost of consuming materials and still maintain the good grinding quality is a good alternative. Moreover, the wafer-cutting process after grinding process sometimes influences the die strength because of the mechanical stress. This condition also needs to be paid attention. Seeking the optimal grinding parameters to ensure the sufficient die strength for distinct chips is, as usual, a challenge to assembly houses in the consideration between whole cost and assembly throughput.

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