Built-In Self-Test for Automatic Analog Frequency Response Measurement

Dayu Yang, Foster Dai and Charles Stroud
Dept. of Electrical and Computer Engineering, 200 Broun Hall,
Auburn University, AL 36849-5201, USA

***Abstract*—We present a Built-In Self-Test (BIST) approach based on direct digital synthesizer (DDS) for functional test of analog circuitry in mixed-signal systems. DDS with delta-sigma noise shaping is used to generate test signals with different frequencies and phases. The DDS-based BIST hardware implementation can sweep the frequencies through the interested bands and thus measure the frequency response of the analog circuit. The proposed BIST approach has been implemented in Verilog and synthesized into a Field Programmable Gate Array (FPGA). The actual device under test (DUT) was implemented using a Field Programmable Analog Array (FPAA) to form a complete BIST testbed for analog functional tests.**

I. Introduction

It is highly desirable to automate the analog testing process with low cost, built-in test circuitry. Built-In Self-Test (BIST) of analog circuits is important and necessary to produce highly reliable mixed-signal systems. Due to the constant increase of analog circuit speed and density, the nature of analog faults, and the embedding of analog functions within large digital systems, the detection and isolation of faults in these circuits is becoming more difficult. At operating frequencies beyond a few GHz, analog IC testing requires tester electronics to be located close to the device under test, or even better, directly built on-chip. Hence, BIST and other forms of embedded analog testing will come to market in just a matter of time [1].

A few techniques have been suggested to perform on-chip frequency-domain testing of mixed-signal circuits. These approaches normally focus on one or two simple parameter tests such as cut-off frequency of a filter and cannot perform rigorous and complete analog tests such as frequency and phase responses. The goal of prior art techniques was to overcome the complexity of integrating a traditional AC characterization approach [2]. Well-defined techniques for reducing the size of the test set while maintaining high fault coverage have been reported [3][4]. Some AC BIST techniques inject optimized digital inputs into a linear device under test and extract a DC signature [5][6]. These approaches are simple, but their precision is limited. On the other hand, Roberts [7] has proposed several methods to make frequency-domain tests using on-chip generated sine waves and analyzing the results with an on-chip digital signal processor (DSP). The approach requires 1-bit delta–sigma digital-to-analog converters (DACs) with moderate area overhead, yet the precision of the generated frequency is not fine enough for the test. Several techniques have been published to generate on-chip linear ramps [8]–[12], but the results either depend largely on the accuracy of the additional components in the test circuitry, or have not been proven experimentally. An on-chip ramp generator can perform monotonicity and histogram tests of analog-to-digital converters (ADCs), yet the linearity of the on-chip ramp generator itself needs to be very high. A FFT approximation algorithm was developed for on-chip sinusoidal signal generation and analysis in [13]; however, the area and power penalties associated with FFT calculations are large as indicated by the fact that the BIST approach was implemented in the largest Xilinx Virtex-II series Field Programmable Gate Array (FPGA). We have proposed a novel BIST scheme for analog linearity test using direct digital synthesizer (DDS) as the test generator and a simple multiplier/accumulator as the test analyzer avoiding using expensive FFT [15].

Analog functional test is a challenging task even as a manual test by an experienced engineer. It tests the functionality of the circuit against the system specifications. The complexity of the functional test depends on test tasks and the operational frequency. For instance, a base-band amplifier test normally includes its frequency response, phase response, in-band ripple and 3dB cut-off frequency.

We have developed a DDS based BIST approach, which can generate sinusoid waveforms with different frequencies, amplitudes and phases for analog functional test. For base-band digital test features such as the test pattern generator (TPG) and output response analyzer (ORA), we initially designed and synthesized the functionality in FPGA with the intent to eventually fabricate the design in a CMOS ASIC. We have been investigating and analyzing this DDS-based BIST approach for its ability to detect faults and to assist in characterization and calibration during manufacturing and field testing.

The vast majority of the BIST circuitry resides in the digital portion of the mixed-signal system to minimize area and performance impact on the analog circuitry. The test scheme utilizes the existing DACs and ADCs with relative speed and resolutions that are associated with conventional transceiver base-band architectures and thus provides accurate analog testing without adding much extra hardware. The DDS-based TPG can provide precise frequency sweep tones for the test of frequency response of analog circuits.

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The area penalty associated with a conventional DDS approach is minimized by size reduction of ROM look-up table. A delta-sigma noise shaping scheme for DDS is presented in this paper to reduce the spurs caused by finite phase word length in ROM. For each specific frequency sweep period, the DDS generates a constant frequency test signal according to a frequency control word (FCW). On the other hand, a delta-sigma modulator with DC input is stable and guaranteed to gain a high *SNR* (signal to noise ratio) at its output as long as the quantization white noise model for the modulator holds. We let the modulator modulate the FCW directly before it comes into the accumulator. This kind frequency domain delta-sigma modulation can make all output test sine waves have the same *SNR* no matter what frequency they are. Another challenge is the development of an efficient ORA that can make the frequency response measurement on-chip. Such a BIST approach can then be modeled in parameterized Verilog for easy incorporation in any mixed-signal design.

II. DDS WITH DELTA-SIGMA NOISE SHAPING

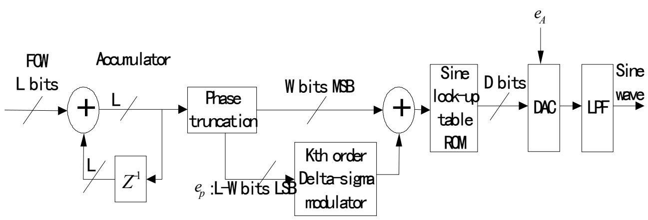

Figure1. Conventional DDS with delta-sigma modulation.

DDS is an important frequency synthesis technique that provides low cost synthesis with ultra fine resolution. As shown in Figure 1, a conventional DDS includes a digital accumulator that generates the phase word based on the input frequency word FCW. The synthesizer step size is defined as $f_{clk}/2^L$ where L is the number of bits in the accumulator. Fine resolution can thus be achieved using a large accumulator size. The DDS utilizes a look-up table to convert the phase word to a sinusoidal amplitude word, whose length is normally limited by the finite number of input bits of the DAC. A low pass filter is added after the DAC to remove the spurious components generated in the data conversion process. While a pure sinusoidal waveform is desired at the DDS output, spurious tones can occur mainly due to the following two nonlinear processes. First, in order to reduce the look-up table Read Only Memory (ROM) size, the phase word needs to be truncated before being used as the ROM addresses. This truncation process introduces quantization noise, which can be modeled as a linear additive noise to the phase of the sinusoidal wave. Second, the ROM word length is normally limited by the finite number of bits of the available DAC. In other words, the sinusoidal waveform can be expressed only by words with finite length, which intrinsically contains quantization error additive to the output amplitude. Considering the quantization errors due to phase truncation e_p (the truncated L-W LSBs), and amplitude truncation (finite ROM word length) e_A, and assuming the phase quantization error is small relative to the phase, the DDS output can be determined as:

$$\begin{aligned} A_{out} &= A\sin\left(\frac{2\pi Wi}{2^n} + e_p(i)\right) + e_A(i) \\ &\approx A\sin\left(\frac{2\pi Wi}{2^n}\right) + Ae_p(i)\cos\left(\frac{2\pi Wi}{2^n}\right) + Ae_A(i) \end{aligned} \tag{1}$$

It has been shown that the phase truncation process associated with the conventional DDS architecture introduces quantization error. To avoid aliasing during data conversion, the synthesized frequency is required to be smaller than the half of DDS clock frequency, $f_{clk}/2$. Thus, oversampling is always encountered in DDS, allowing noise-shaping techniques to be used to shift the phase quantization error to a higher frequency band, where the noise can be eventually removed by the low pass filter after the DAC. As shown in Figure 1, a k^{th} order delta-sigma noise shaper with unique transfer function is added after the phase truncation. It can be shown that the phase error e_p is high-pass filtered by the delta-sigma modulator before the amplitude modulation via the look-up table. This greatly reduces the close-in phase noise and de-correlates the phase truncation error. As a result, spurious components at the DDS output are greatly reduced or eliminated. A more ideal sinusoidal waveform with greatly reduced close-in phase noise and spurious components is achieved at the DDS output.

Considering the linear model of a delta-sigma modulator with white quantization noise that has a root mean square value (rms) e_{rms}, we can get the rms noise in the signal band

$$n_0 = e_{rms}\frac{\pi^K}{\sqrt{2K+1}}(2f_0\tau)^{K+1/2} \tag{2}$$

The noise falls $3(2K+1)$ dB for each doubling of the *OSR*. Thus a high *K* and a high *OSR* can result in high *SNR* at the output of modulator and so for the DDS.

In the DDS with delta-sigma modulator in phase domain (shown in Figure 1), the phase error e_p (L-W bits LSBs) has different repeating periods with different FCW. This leads to the input to the modulator to have changing frequencies. For instance, when the L-W LSBs of a FCW is small, the phase error e_p changes slowly and the modulator's input frequency is slow. On the other hand, it can be very fast when L-W LSBs of a FCW is very big. At the same time, the sampling clock f_{clk} for the delta-sigma modulator is fixed. So the *OSR* of the delta-sigma modulator in DDS phase domain changes with different FCW. The output sine waves with different frequencies thus have different *SNR* and it would influence the test accuracy.

In order to eliminate the varying over-sampling ratio, the input of the delta-sigma modulator is best to be a constant. We thus relocate the delta-sigma modulator in front of the accumulator and let it modulate the FCW directly before it goes to the phase accumulator. The DDS structure with delta-sigma modulation in frequency domain is shown in

Figure 2. We can see that the L-bit FCW is truncated to W-bit MSB and L-W bits LSB. The L-W bits LSB which is a constant is fed into a K^{th} order delta-sigma modulator before it adds back to the frequency word. This is a typical case of a delta-sigma modulator with DC input. The high SNR can be guaranteed as long as the order of the modulator is high. Another advantage of this structure is the length of the phase accumulator is also cut from L to W which saves hardware area. Because the FCW is L-bits, this DDS still keeps a frequency resolution of $f_{clk}/2^L$.

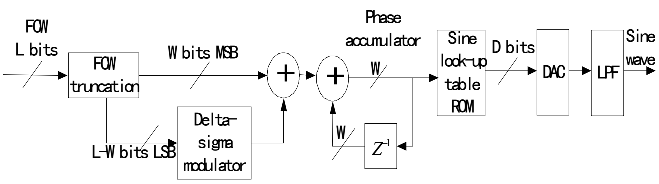

Figure 2. DDS with delta-sigma modulator in frequency domain

In order to prove the concept, we modeled proposed DDS architecture using delta-sigma modulation in frequency domain in MATLAB. Figure 3 demonstrates high-pass noise shaping effect of the 3^{rd} order delta-sigma modulation with a 60dB/dec slope in DDS output spectrum. Compared with the 2^{nd} modulator structure [14], we also realized the 3^{rd} order delta-sigma modulator using four topologies including MASH, feed-forward, feed-back and error feedback. All of them have very good 3^{rd} order noise shaping effect in the output waveforms.

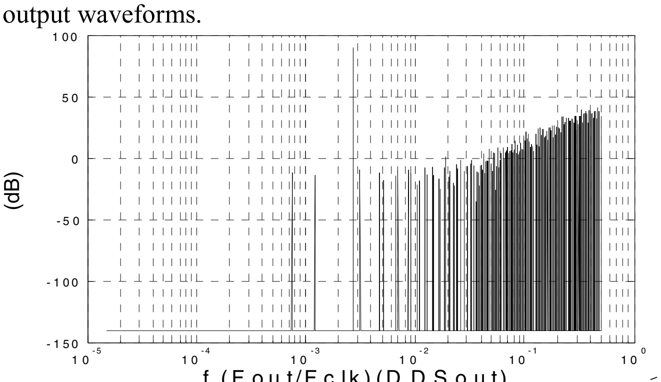

Figure 3. Simulated DDS output spectrum with 3^{rd} order noise shaping

III. Frequency Response Test Using DDS

Frequency response (both amplitude and phase response) is the key measure for analog integrated filters and amplifiers. The commonly interested cut-off frequency of the filters and amplifiers can be found by measuring the pass-band and stop-band amplitude response, while the linearity (group delay) can be determined from the phase response. To test the analog filter and amplifiers, the DDS generates frequency tones with fine resolution. A DDS-based TPG and two ORAs can scan the pass and stop bands of the device with fine step size and can thus measure the frequency and amplitude responses of the device, as shown in Figure 4.

Note in Figure 4 that DDS1 generates a fine-toned sine wave T1 with a DC bias k1. After the test signal T1 passes through the analog device, both its amplitude and phase will change. The signal output of DUT (Device Under Test) is given by $D = A_2\cos(\omega_1 t+\vartheta)+k_2$. A second DDS (DDS2) is used to generate test signal T2 that has the same frequency and amplitude as T1. A level shifter is used to shift the T2 signal such that it is symmetrical to the X-axis (from $-A_1/2$ to $A_1/2$). During the frequency sweep, if all the test signals T2 start from phase 0, namely $T2=A_1\cos\omega_1 t$, the signal after the multiplier is hence given by:

$$MUL = A_1\cos(\omega_1 t)\cdot(A_2\cos(\omega_1 t+\theta)+k_2)$$
$$=\frac{A_1A_2}{2}\left[\cos\theta+\cos(2\omega_1 t+\theta)\right]+A_1k_2\cos\omega_1 t \quad (3)$$

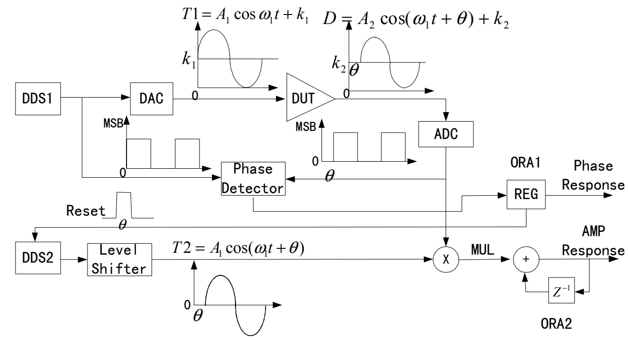

Figure 4. BIST of frequency response of an analog circuit

We use an accumulator to obtain the above result and we end the accumulation on a common period of all the test sine multiplication. The period of the different test signal is:

$$T_p=\frac{1}{\frac{FCW}{2^L}\cdot F_{clk}}=\frac{2^L}{FCW}\cdot T_{clk} \quad (4)$$

By setting the step of input frequency control word to be a power of 2, we can get the same period for all the test signals. In our case, the biggest period of the test signal is when FCW=2 which is $2^{L-1}T_{clk}$, so we set the time of calculation to be $2^L T_{clk}$. The phase step is set to 2 to achieve the finest frequency resolution which is $2/2^L$. The accumulator translates the output to a constant:

$$ORA=\frac{A_1A_2}{2}\cos\theta\times 2^L \quad (5)$$

If there is no phase shift, θ=0, the degradation of A_2 compared with A1 will be shown in the ORA. When the ORA value decreases to 0.707 times its initial value, we have reached the 3dB amplitude point of the analog circuit. Unfortunately, analog circuits always have phase shift θ. Therefore, we need to measure θ first and make adjustments to the test signal to achieve the same phase shift.

The MSB of the test signal T1 and the MSB of the signal D from the ADC are square waveforms with the same frequency and phase as their sine waveforms. Therefore, we can get the phase difference with a phase detector and record the phase shift θ corresponding to this frequency in a register and output it to the computer. For the next test frequency the register will record another phase shift and after the whole frequency sweep, we will get the frequency response of the analog device. Before the change to next test frequency, the BIST circuitry also performs the amplitude response test. When the amplitude test begins, the DDS2 is reset and delayed for a phase θ that is stored in the phase register. Hence, its output T2 has the same frequency and amplitude as those of T1 but has a phase shift θ as D does, namely,

$$T2 = A_1 \cos(\omega_1 t + \theta) \qquad (6)$$

With the modified T2 as one input to the multiplier, the ORA1's output in equation (5) will have no effect of phase shift θ and we can get both the correct frequency response and amplitude response of the analog device.

IV. Experimental Results

We have used the proposed BIST scheme to measure the frequency response of a low pass filter (LPF). As discussed, the built-in DDS generates the test tones that scan over the frequency from 0 to ½ f_{clk} with a frequency step $(1/2^{L-1})f_{clk}$. A first order low pass filter was used as a device under test to test our BIST method which automatically applied the test tones at the input of the filter and measured its output magnitude response from ORA2. The cutoff frequency of the amplifier and LPF modules, which is 3dB below the pass-band magnitude, can thus be found at 46kHz from Figure 5.

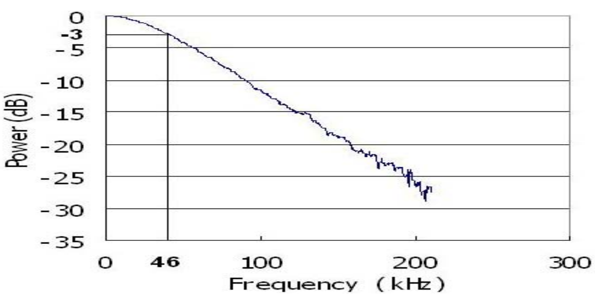

Figure 5. BIST measured frequency response of a low pass filter

The DDS-based TPG, test controller, and multiplier-accumulator-based ORA were modeled in Verilog along with an interface to allow PC control of the BIST circuitry and retrieval of the BIST results. The complete Verilog model is approximately 510 lines of non-commented code. The Verilog code can be parameterized to facilitate easy adaptation of the BIST circuitry for different size DAC and ADC for synthesis into standard cell based ASICs or into FPGAs. In our implementation, we used an 8-bit DAC and ADC and synthesized the BIST circuitry into a Xilinx Spartan XC2S50 FPGA. The synthesized circuit required less than 25% of the total logic resources in the Spartan 2S50 and, as a result could easily fit into the smallest Spartan II FPGA. This means that the BIST-based frequency response measurement circuitry can be efficiently implemented in the digital portion of an ASIC with little area overhead.

V. Conclusions

We have presented a DDS-based BIST approach analog circuit functional testing frequency response. The DDS with a 3rd order delta-sigma modulator is used to generate test tones. We also developed an output response analyzer consisting of a multiplier and an accumulator. The BIST analyzer avoids using a traditional FFT-based spectrum analysis, which consumes much more power and die area. We have implemented the BIST approach in Verilog which was subsequently synthesized into an FPGA and verified on actual hardware using a low pass filter as the device under test. Through measurements for an 8-bit sample system, we found that the BIST circuitry can obtain accurate amplitude and frequency responses of the analog device. The proposed BIST scheme using the existing ADC/DAC will automatically meet the system dynamic range requirement, which fully demonstrates the fidelity of the proposed BIST approach for analog circuit functional test.

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