MODULES DEVELOPMENT FOR THE TTC SYSTEM

Per Gällnö, CERN, Geneva, Switzerland
(email: per.gallno@cern.ch)

Abstract

Some of the hardware components designed for the CERN - RD12 optical Timing, Trigger and Control system project [1] are presented, as well as some future developments.

INTRODUCTION

The Large Hadron Collider (LHC) experiments (ALICE, ATLAS, CMS and LHC-B) all require a means of distributing timing, trigger and control information to the different sub-detector Front End (FE) and Read Out systems. This information comes normally from the LHC machine, the Level-1 (LVL1) Central Trigger Processor (CTP), the Data Acquisition system and the Detector Control System.

A multipurpose Fibre Optic (FO) based distribution system, the TTC, has been developed for this purpose within the framework of the CERN - RD12 project. Accepted triggers, trigger information, event count, various calibration, control, reset and test commands can be sent over the TTC network.

THE TTC SYSTEM

System Description

The TTC system is a unidirectional optical fibre based transmission system, where two information channels, A and B, are Time Division Multiplexed (TDM) and Bi-Phase Mark (BPM) encoded using the LHC Bunch Crossing (BC) clock (40.08 MHz) as the carrier frequency. One channel (A) carries exclusively the LVL1 trigger accept (L1A) information and the other (B) carries packaged address and data information for the sending of various reset commands or calibration, control and test parameters.

The LHC BC clock is used as the TTC system master clock and is distributed to all destination systems by the receivers extracting it from the BPM encoded signal.

The data packages sent on the B-channel can either be of short format (8 data bits), used for broadcast commands or of long format (14 address, 8 sub-address and 8 data bits) for individually addressed commands or data transfers. Error correction coding is implemented by adding standard Hamming code, 5 respectively 7 bits, to the two data formats. Commands may either be transmitted asynchronously or in a fixed timing relation to the LHC BC Clock and Orbit signals.

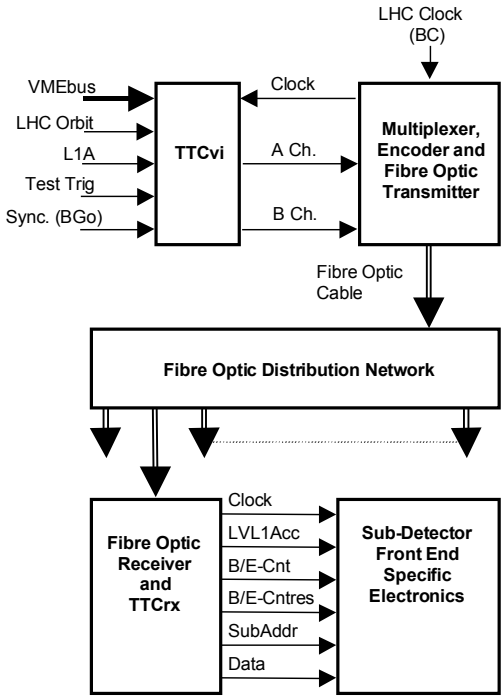

Figure 1. The TTC system block diagram

A final system integrated in the experiment will comprise the following hardware components:

- The LHC Clock and Orbit signals receiver/fan-out crate, TTCmi
- The VMEbus interface module, TTCvi
- The modulator (TDM + BPM) and optical fibre laser transmitter unit
- The tree structured optical fibre distribution network
- The photo detector diode and the TTC receiver ASIC[1], TTCrx
- The FE or Read-Out system specific modules carrying the TTCrx

New developments for TTC

A number of test and evaluation TTC systems are at the present being used at CERN and at collaborating institutes around the globe. In order to get compact and inexpensive TTC systems for such purposes, a low power optical fibre transmitter, with an integrated TDM/BMP encoder, has been designed into a VME sized module (TTCvx).

[1] Application Specific Integrated Circuit

A simple receiver prototype module (TTCsr), in PCI[2] Mezzanine Card (PMC) standard, carrying the TTCrx ASIC has been developed at CERN. Specifications of a second improved version of this TTCsr module are being prepared.

VMEbus INTERFACE - TTCvi

Module Description

Main functions of the TTCvi [2] are to select a trigger source from either the L1A input, test trigger inputs, an internal rate programmable random trigger generator or triggers generated by a specific VME access. The selected trigger source is made available on the communication channel A output and an internal event counter is incremented for each outgoing trigger.

Formatted address/data/command packages are sent on the communication channel B. This is achieved by a VME master writing data to the TTCvi, where it gets buffered in four FIFO's[3] before being requested, then formatted, serialised and sent to the B-channel output. The preloaded data words in the FIFO's may be requested for sending in number of modes. Each of the four FIFO buffers is associated with a front panel input, B-Go[0..3], which can be used to trigger requests for sending packages, either asynchronously or in a programmable timing relation to the LHC Orbit signal. The B-Go signals may also be generated internally by specific VME accesses. Possibility exists to select a sending request mode where only the presence of data in the FIFO is checked in order to initiate B-channel transfers. Yet another mode permits the re-transmission of the content in the FIFO.

Four pulse generators, with programmable delay and duration timings and each associated with a FIFO buffer, are triggered by the LHC Orbit signal (11.245 kHz / 88.924 μs) to produce the signals INHIBIT[0..3]. The INHIBIT signals schedules, when running in a synchronous mode, the B-channel transfers from the FIFO buffers in a way that the commands arrive to the destination systems in a precise timing relation to the LHC bunch structure.

Un-buffered asynchronous long or short transfers on the B-channel may, as an alternative, be achieved by writing data to specific VME registers.

The content of the internal event counter, together with the trigger type code generated by the CTP are buffered and then transferred on the B-channel for each on the A-channel outgoing trigger.

An arbitration scheme is implemented in order to grant the different B-channel transfer request types on a priority basis, where the B-Go[0] ones has the highest and the VME register ones the lowest.

BC clock and Orbit signals may either come from an external source (TTCmi) or be generated internally for stand alone test purposes.

The TTCvi is a 6U/4TE size VME slave module with A24/D16 + D32 capabilities.

Status

Two batches of 20 TTCvi modules each have so far been fabricated of which 30 modules have been delivered to the users. Before launching fabrication of a subsequent batch a questionary will be addressed to all TTCvi users in order to collect some opinions. The milestones for the ATLAS requirements are a preliminary design report in December 1999, the final one in September 2000 and final version of TTCvi in June 2001.

TTCvi Test Module

A test bench has been set up for the testing of TTCvi modules before delivered to the users. For this purpose has a TTCvi Test Module been designed, which generates the necessary input signals to the TTCvi and de-serialises, strips and buffers packages generated on the B-channel. A menu driven test software has been written to check, among other features, data and Hamming code correctness.

ENCODER AND FIBRE OPTIC TRANSMITTER - TTCvx

Module Description

The TTCvx [3] module function is to multiplex and encode the A and B communication channels generated by the TTCvi and to transmit the resulting modulated signal to the destination TTCrx's via fibre optic cables. Time Division Multiplexing (TDM) is used where the A and B channels are sampled alternatively every half period of the basic clock. The encoding is achieved by using a Bi-Phase Mark (BPM) scheme.

[2] Peripheral Component Interconnect
[3] First In First Out memory

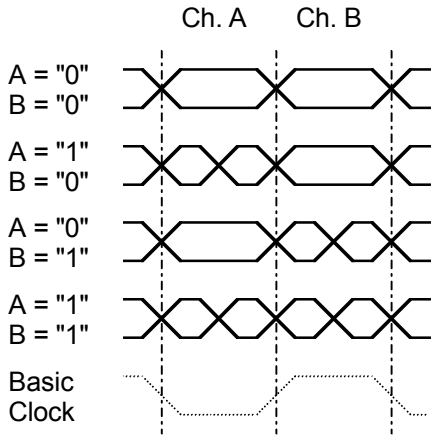

Figure 2. Encoder output wave forms

The TTCvx has an internal clock, as well as an input for an external one. The switching between the two clock sources is automatic by the means of an external clock detection circuit. A PLL frequency synthesizer circuit handles the necessary clock multiplication for the encoding. The basic clock frequency from the PLL is available on the module front panel in both LVDS[4] and ECL[5] levels and is used for synchronization with the TTCvi. Up to four light emitting devices can be fitted to drive fibre optic cables. The encoded signal is also available on the front panel in both ECL and LVDS levels.

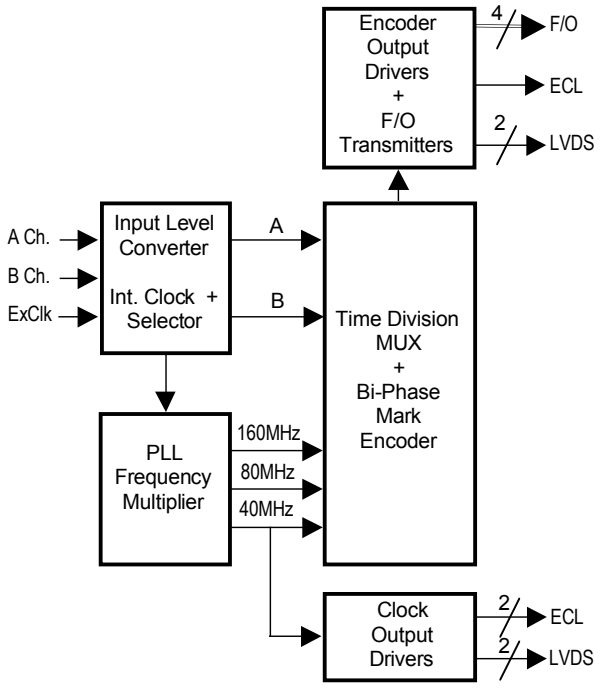

Figure 3. TTCvx Block diagram

The TTCvx is a 6U/4TE size VME module without any signal connection to the VMEbus, only the +5V and -12V power rails are used. The design has been implemented using PECL[6] technology.

The fibre optic transmitter works at a wavelength of 1330 nm and has an average output power of min. -19 dBm, which is sufficient for test set-ups, as fibre optic receivers normally have in input sensitivity of approximately -32 dBm. For example has a 100 m long fibre optic cable of 50/125 µm type a typical damping of -2 dB.

Status

25 TTCvx modules have so far been fabricated, whereof most have already been delivered to the users. A second batch will be put into fabrication as soon as some feedback has been collected.

RECEIVER ASIC - TTCrx

Brief description

The TTCrx [4] with associated photo detector diode and pre-amplifier receive and decode the signal on the optical fibre. Received packages are recognised as being either broadcast commands or individually addressed internal or external sub-address/data words. Each TTCrx has a unique 14-bit identification (ID) number serving as its system address. The ID is stored locally and read by the TTCrx on initialisation. The contents of the TTCrx internal bunch crossing and event counters, the LVL1 trigger decision and the received sub-address/data information are made available to external systems on the outgoing busses. The LHC clock is recovered from the incoming BPM encoded signal and is presented on output pins for system synchronisation. Internal programmable de-skewing circuits allow proper timing of the extracted clock, broadcast commands and the trigger decision. The TTCrx ASIC chip is available in a 100-pin BGA[7] package.

Availability

The fabrication of a revised radiation hardened version has just been submitted and samples should be available towards the end of 1999. A limited number of the present version of the TTCrx is still available.

SIMPLE RECEIVER INTERFACE - TTCsr

The TTCsr [5] is implemented as a PMC module carrying the fibre optic receiver, preamplifier, the TTCrx, data buffers and the interface logic. The information on the different TTCrx busses is buffered in FIFO's before presented to the PCI bus interface. Some of the clock, strobe and reset signals from the TTCrx are passed onto front panel connectors via level converters.

[4] Low Voltage Differential Signalling
[5] Emitter Coupled Logic
[6] Positive Emitter Coupled Logic
[7] Ball Grid Array

New specifications

A couple of TTCsr prototypes of the present version have so far been assembled and tested. The ATLAS data acquisition team foresees the integration of such a module into their system and is presently collaborating in writing the specifications of an enhanced performance version of the TTCsr.

TTC SYSTEM LATENCY

The latency between an input of the TTCvi module and an output of the TTCrx ASIC was measured in two cases, namely the one for the LVL1 accept signal and the other for a broadcast command. The following figures show the net TTC system latency:

- ♣ LVL1 Accept: ≈ 100 ns
- ♣ Broadcast command: ≈ 230 ns (end of package to output strobe)

EXPERIMENTS REQUIREMENTS

The future TTC system requirements, with respect to the number of partitions and destinations, of the LHC experiment have not yet been fully investigated. Estimates for the ATLAS experiment talk for at least 40 partitions with up to 10'000 destinations.

CONCLUSION

Complete sets of components and modules are now available for the TTC system. Feedback from the LHC experiments should be taken into account before a final specification is established. A subsequent production will then be launched within the two coming years.

REFERENCES

[1] B.G. Taylor: "RD12 Timing, Trigger and Control (TTC) Systems for LHC Detectors" http://www.cern.ch/TTC/intro.html

[2] Ph. Farthouat and P. Gällnö: "TTC-VMEbus Interface (TTCvi)" http://www.cern.ch/TTC/TTCviSpec.pdf

[3] P. Gällnö: "TTCvx Technical Description and Users Manual" http://www.cern.ch/TTC/TTCvxManual1a.pdf

[4] J. Christiansen, A. Marchioro and P. Moreira: "TTCrx Reference Manual" http://pcvlsi5.cern.ch:80/MicDig/ttc/MANUAL22.PDF

[5] J. Ferrer Prieto: "TTCsr Documentation" http://www.cern.ch/TTC/TTCsrDoc.pdf