Circuit Simulation Models for Coming MOSFET Generations

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Abstract— **The urgent tasks of MOSFET modeling for circuit simulation are easy adaptation to new physical phenomena arising for advancing technologies, and, of course, sufficient simulation accuracy. Approaches currently being pursued for developing such MOSFET models are summarized. Their capabilities for accomplishing these tasks as well as the important remaining problems are discussed.**

I. Introduction

CIRCUIT simulation predicts performance of a given design on the transistor or layout level with transistor response such as currents. These responses such as drain current dependence on drain and gate voltages are modeled analytically as simple functions of these voltages including model parameters. With increasing circuit size two different types of simulators become necessary to handle the complexity, while maintaining sufficient accuracy: One is the physical level simulator including the analytical models, commonly called SPICE simulator. The other is a high level simulator dealing primarily with the circuit logics in stead of the I-V characteristics (see for example [1]). Even the high level simulator usually relies on analytical transistor models for the preparation of the performance data (e. g. delay times, driving currents) of its library elements. Thus the transistor model is a key for both types of simulation.

Requirements for circuit simulation are increasing according to the development of system integration with many different functions. This development trend forces standarization of fabrication processes to merge different functions among different fabrication facilities including utilization of existing IPs. To assist the development, the most important modeling issue is to guarantee sufficient simulation accuracy and applicability for any advanced technology. For achieving this task it is inevitable to maintain a physically correct modeling of the real technology processes which govern the function of these MOSFETs, even in the circuit simulation model. Here the approaches to realize the outlined requirements are summarized. It will be also demonstrated that the models can be skillful not only for circuit simulation with advanced MOSFETs but also for rapid device optimization through concurrent development with 2D process/device simulations.

II. Different Approaches for Modeling

Fig. 1 shows a commonly used equivalent circuit of a MOSFET [2]. Analytical circuit models describe all components in the equivalent circuit as a function of applied voltages on the four terminals (gate, source, drain and bulk). These four terminals induces three charges inside the transistor as shown in Fig. 2. The mobile charge density Q_i underneath the gate is partitioned into two components Q_s (source charge) and Q_d (drain charge) according to dynamic operations. Here analytical MOSFET models suffer two contradictory requirements: They should be as simple as possible, and should be highly accurate at the same time. There are different approaches intending to find an optimum compromise between these requirements. An important quality measure of the resulting model is the number of model parameters, and whether the model parameters reflect applied technology.

A. Conventional Drift Approximation

Most models such as the BSIM series [3], developed by the UC Berkeley, and the Philips MOS Model 9 [4] are descendants of the Meyer model, the first MOSFET model ever developed [5]. The Meyer model describes the device characteristics in a simple way as a function of applied voltages. The explicit descriptions were derived by the drift approximation ignoring the diffusion component. Since the original Meyer model fails to fulfill the charge conservation, the capacitance model was improved by Ward et al. [6] to simulate accurate charge storage behavior.

At an early stage of the IC-technology development the accuracy of this model was satisfactory. However, two major problems became remarkable with advancing technology: One is existence of discontinuities [7] in the model description and the other is the appearance of short-channel effects. The discontinuities occur due to application of the drift approximation. The drain current I_{ds} is written by

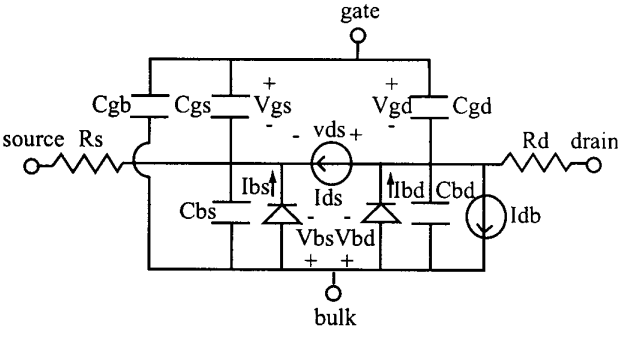

Fig. 1. Equivalent Circuit of a MOSFET for circuit simulation.

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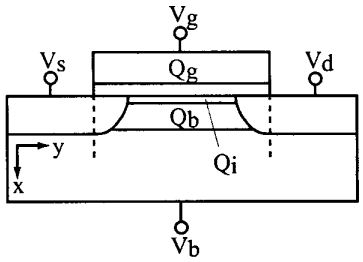

Fig. 2. Schematics of a MOSFET cross-section with induced charge densities.

fixing the potential at the threshold value [8]

$$I_{ds} \propto C_{ox}[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2] \quad (1)$$

Here C_{ox}, V_{gs}, V_{ds}, and V_{th} are oxide capacitance, gate voltage, drain voltage, and threshold voltage, respectively. Equation (1) is valid in principle only in the linear region. I_{ds} is extended to the subthreshold region by

$$I_{ds} \propto \{1 - \exp(-\frac{V_{ds}}{v_t})\} \exp(-\frac{V_{gs} - V_{th} - V_{off}}{\mathbf{n}v_t}) \quad (2)$$

where v_t is the themal voltage and other parameters have the same meaning as in [3]. At the transition between these two regions occurs a discontinuity (see Fig. 3), which is smoothed numerically by transforming the physical V_{gs} into an effective V_{gseff} [3]

$$V_{gseff} = \frac{2\mathbf{n}v_t \ln[1 + \exp(\frac{V_{gs} - V_{th}}{2\mathbf{n}v_t})]}{1 + 2\mathbf{n}C_{ox}\sqrt{\frac{2\Phi_s}{q\epsilon_{si}N_{ch}}} \exp(-\frac{V_{gs} - V_{th} - 2V_{off}}{2\mathbf{n}v_t})} \quad (3)$$

Another discontinuity occurs at the transition between the linear and the saturation region. It is caused by the assumption that V_{ds} is small in order to derive (1). This is again smoothed numerically by introducing an effective V_{ds}

$$V_{dseff} = V_{dsat} - \frac{1}{2}\Big(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}\Big) \quad (4)$$

where definition of all parameters is found in [3].

The slight I_{ds} increase in the saturation region as a function of V_{ds} for reduced short-channel lengths is modeled by the channel length modulation in such piece-wise models [3]. As the short-channel effects, three phenomema are observed in the subthreshold region [9]; the V_{th} reduction as a function of gate length L_{gate} and as a function of V_{ds} as well as a slight increase of the subthreshold swing. The modeling is based on the charge sharing concept developed by Yau [10]. The sharing of the depletion charge among the channel and the S/D contacts is described geometrically in a simple way, and thus requires many fitting parameters to reproduce measured V_{th} characteristics. A big advantage of the drift approximation is that model equations are explicit functions of applied voltages. However, the drift-based models suffer from non-physical parameters introduced only for smoothing. Another problem of these models is that the technology is hardly reflected in the model parameters, since the technologically most senstive subthreshold region is described by a mathematical equation with a fitting parameter **n** as shown in (2).

B. Drift-Diffusion Approximation

The drift-diffusion approximation was originally developed by Pao and Sah [11]. The physical reliability of the approximation has been proved by 2D device simulators for MOSFETs with channel lengths even down to 0.1μm [12]. Instead of solving the basic equations (the Poisson equation, the current density equation) in 2D, the charge-sheet approximation was developed, which ignores the inversion channel width to simplify the calculation procedure [13]-[15]. Resulting key equations are the 1D Poisson equation and the following equation

$$\frac{\phi_{SL}}{v_t} = \frac{\phi_{S0}}{v_t} + \frac{V_{ds}}{v_t} + \ln\frac{Q_i(L)}{Q_i(0)} \quad (5)$$

derived from the drift-diffusion approximation, where Q_i is the inversion charge density. Here the two surface potentials ϕ_{S0} and ϕ_{SL} are those at the source and the drain side, respectively. All transistor characteristics are described as functions of these potential values. The main drawback of models based on the drift-diffusion approximation is that the surface potentials are implicit functions of applied voltages. Thus two iteration procedures for obtaining ϕ_{S0} and ϕ_{SL} are necessary. However, it has been demonstrated that in spite of the iteration procedures the total calculation time required for circuit simulation can be even less than a

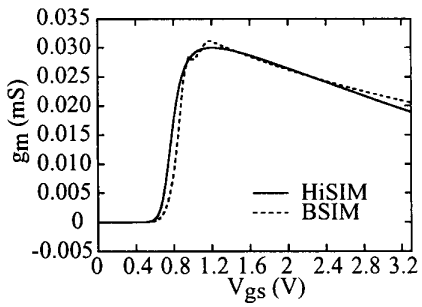

Fig. 3. Comparison of simulated transconductance g_m at $V_{ds} = 0.1V$.

conventional piece-wise model [16]. In fact a drift-diffusion model has more advantages than drawbacks. The most important one is that the model is valid for all applied voltage regions without discontinuities (cf. Fig. 3). This simplifies the model description, keeps the number of model parameters in principle at minimum, and results in simple parameter extraction. A couple of models based on the drift-diffusion approximation have been already developed [16]-[19]. Two models among them [17],[18] treat the saturation condition explicitly by considering the region where carriers flow in 2D [20]. The gradual-channel approximation, employed to obtain decriptions for device characteristics in closed form, aviods the saturation condition in the channel [13],[16]. A model based on the drift-diffusion approximation named HiSIM (Hiroshima-university Starc IGFET Model) is currently developed by Hiroshima University and STARC (Semiconductor Technology Academic Research Center), and is proved to be valid for L_{gate} down to 0.10 μm. It was shown that HiSIM reproduces observed device performances including the quantum and poly-depletion effects for any L_{gate} only with 19 model parameters. The reason for the drastical parameter reduction in comparison with BSIM3v3, as well as MOS Model 9 requiring nearly 100 model parameters, is exactly due to the drift-diffusion based description of HiSIM. All short-channel effects are described by the lateral electric-field gradient as their physical origin [16]. The field gradient is included explicitly in the model equations for solving the surface potentials, and is derived from measured V_{th} shifts in comparison to a long-channel transistor. Fig. 4 shows simulated potential values as a function of V_{gs} and V_{ds} for $L_{gate} = 0.12\mu m$. Fig. 5 compares simulated I-V characteristics with measurement. HiSIM simulation results reproduce measurement excellently, without the channel-length modulation as a function of V_{ds} and the charge-sharing parameters needed in the conventional models.

Even though the superiority of a drift-diffusion model is obvious, the most commonly used model is based on the drift approximation. This has 3 important reasons: One reason is the history of the model development aiming to simplify the description. The most severe reason is the complexity to derive descriptions for all device characteristics appearing in the equivalent circuit shown in Fig. 1. Another important problem for a circuit model based on the drift-diffusion approximation is to ensure numerical precision. It has to be emphasized that surface potential values require an accuracy of $10^{-12}V$ to get stable convergence in circuit simulation.

C. Other Modeling Approaches

The EKV model developed by Enz et al. is based on an approach similar to the drift approximation [21]. Instead of focusing on the inversion condition, as the models based on the drift approximation, EKV concentrates on the low gate-voltage region up to moderate inversion which is important for analog applications. Distinguishable improvement in comparison with BSIM3v3 is not observable [22].

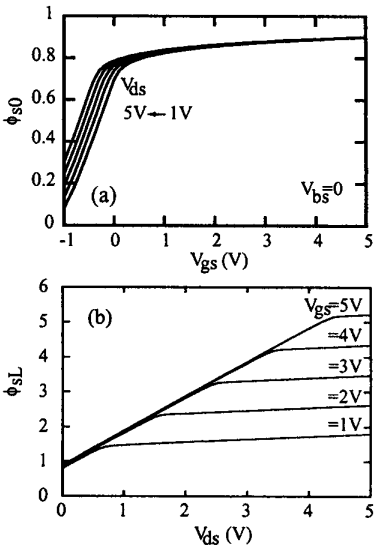

Fig. 4. Calculated surface potential (a)ϕ_{S0} as a function of gate voltage V_{gs}, (b)ϕ_{SL} as a function of drain voltage V_{ds} for $L_{gate} = 0.12\mu m$.

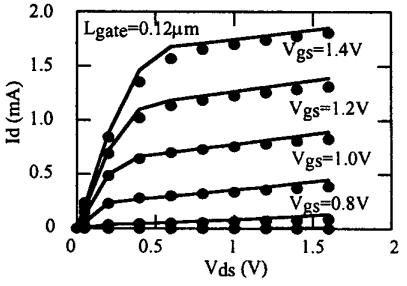

Fig. 5. Comparison of I-V characteristics between measurements (symbols) and calculated results (lines) at V_{bs}=0.

III. Future Requirements for Circuit Simulation

A. Technology Fluctuations

The minimum L_{gate} employed for advanced technologies is reduced down to $0.10\mu m$ and the gate oxide thickness is as thin as $3nm$. Under such conditions the influence of technological fluctuations on device characteristics cannot be ignored. Usually the circuit simulation includes the fluctuation by considering the boundaries as worst case parameters [23],[24]. There are many, mostly mathematical methodologies to determine technology fluctuations, which sensitively affect device performance fluctuations. These methodologies mainly focus on finding the condition giving the minimum parameter fluctuation [25]. However, more

desired is to provide a methodology to minimize the device performance fluctuation caused by the technology fluctuations with less statistical data. For this purpose the transistor model is an important candidate. However, transistor characteristics are already very complicated, and analytical models require many model parameters. To secure the robustness of the simulation result, reliability test of model parameters may be done such as shown in Fig. 6. The test proves whether the model parameters coincide exactly with device parameters determined by technology. If this is realized, the device perfromance as well as the circuit performance distribution is well predicted as shown in Figs. 7 and 8, respectively [26]. Such reliability tests can be done only with the help of 2D simulations.

B. Robustness for Advanced Technologies

Technology development pursues the device development scenario. As a result new phenomena are continuously discovered in each development era. The reverse short-channel effect, observed since more than ten years, is one of such phenomena, and is more and more enhanced. The origin of the effect is the substrate impurity pileup at the surface near the source/drain contact [27],[28]. This impurity concentration determines the subthreshold as well as the moderate inversion characteristics. The impurity profile was modeled by a linear function of the depth to allow its easy extraction. It was demonstrated that the extraction can be done with measured V_{th}-V_{bs} characteristics as shown in Fig. 9 [29]. Fig. 10 compares the extracted impurity profile with the 2D process simulation result [30]. In spite of this simplification the profile is extracted with sufficient accuracy in the channel region. However, the inavoidable inaccuracy of this analytical description can be recognized at the same time especially at positious deeper in the substrate.

The most precise method for predicting circuit performances is with 2D device/circuit mixed mode simulators solving all basic transistor equations numerically. Even

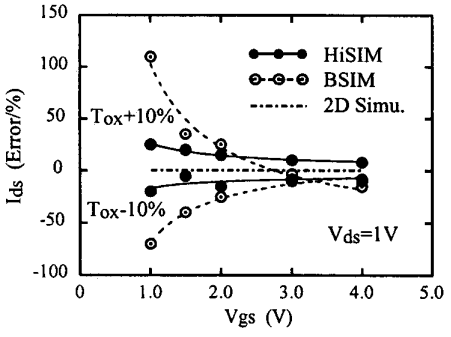

Fig. 6. Robustness test of the gate-oxide thickness T_{ox} appearing in circuit models. If T_{ox} has the same meaning as it should be, simulation results with its deviated values from +10% to -10% should be correct.

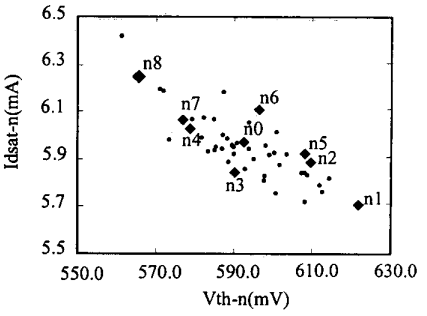

Fig. 7. Measured distribution of saturated drain current I_{dsat} as a function of threshold voltage fluctuation (solid circles) for n-channel MOSFETs. Numbers from n1 to n8 with solid diamonds are calculated boundaries with a model [24].

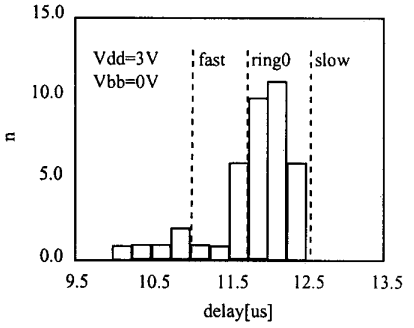

Fig. 8. Meaured histogram for the 23-stage ringoscillator delay. Three dashed lines represent the calculated nominal (ring0) and boundary values with a model [26].

though simulation time is drastically reduced by improved CPU time, no 2D simulator can treat a circuit with more than 10 transistors up to now. A clear advantage of the analytical model is the rapid extraction of the essence of the phenomena from measured data and the capability to describe it in a simple way. On the contrary 2D simulators results enable to determine process conditions and their influence on device characteristics exactly. Thus concurrent development of 2D process/device and circuit simulation with analytical models enables device optimization to achieve required circuit performance with reduced performance distribution [31]. A possible scheme for such a concurrent development is shown in Fig. 11. The key issue to realize such concurrent developments is that the model parameters have to coincide with device parameters determined by the process technologies. Once the model describes a phenomenon according to its physical origin, it is also easier to extend the model to new phenomena appearing in the following technology generations. As an example Fig. 12 demonstrates an extension of the drift-diffsion model HiSIM for an advanced technology with the poly-gate depletion effect. This extension is achieved with-

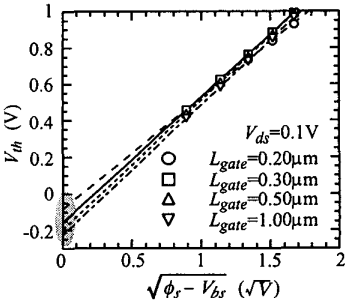

Fig. 9. Measured V_{th} as a function of $\sqrt{\phi_S - V_{bs}}$, where ϕ_S is fixed to the potential value at threshold condition. The shadowed spoitting at $\sqrt{\phi_S - V_{bs}} = 0$ is attributed to the reverse short-channel effect [19].

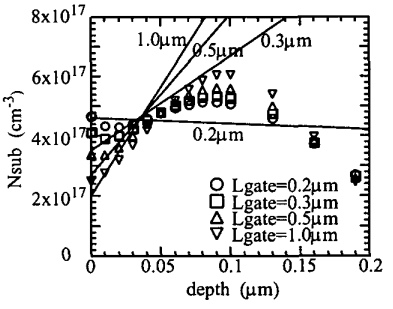

Fig. 10. Comparison of model impurity profiles extracted from simulated V_{th} (lines) and those of 2D process simulation results (symbols) used for the V_{th} simulation.

out any difficulty only by including the potential drop in the gate-poly Si region [19].

C. Beyond the quasistatic approximation

The CMOS technology development starts to enable application for high frequency operation. Cutoff-frequencies of 50Ghz have already been observed for a single transistor [32]. Under such high frequency operation the conventional quasistatic approximation, describing the transient behavior by assuming that charges are only functions of instantaneous terminal voltages [5],[33], has to be improved. The developed non-quasistatic approximation treats the channel as a nonlinear transmission line with time dependent external voltages. Here all possible incremental variables have to be included in analyzing the high frequency operation [34]. A simplified equivalent circuit for such a case is shown in Fig. 13. All components are extracted by Y-parameter analysis derived from S-parameter measurements [35]. It can be seen from the equivalent circuit that derivatives of all device characteristics as a function of all possible applied voltages are required for the simulation. Successful simulation results have been reported [36],[21]. However, to secure the simulation accuracy for any operation condition robustness of all model parameter values is definitely required.

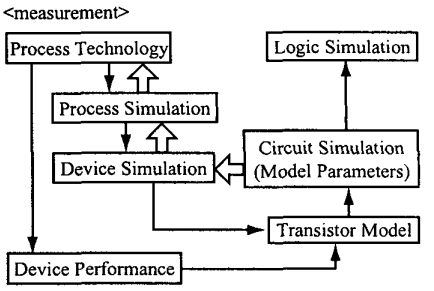

Fig. 11. Schematics of concurrent process, device, and circuit engineering. Open arrows are not yet accomplished, but are desired to realize future development.

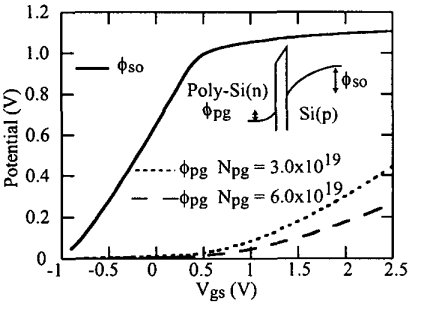

Fig. 12. Surface potential in substrate (solid curve) at the source side and poly-Si (dashed curves) as a function of gate voltage V_{gs}.

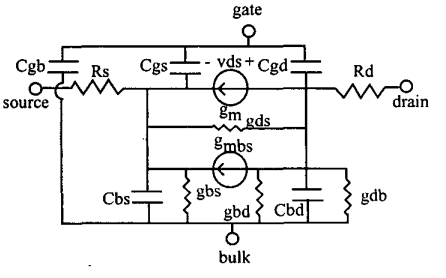

Fig. 13. Equivalent circuit of a MOSFET for small-signal ac analysis.

IV. Conclusion

Importance of analytical MOSFET model is increasing with the complexity of IC design and by pushing the technology to its limit. Here we have demonstrated that the model cannot only predict circuit performance for given transistor characteristics but also can expand its role to the optimization to achieve high performance yield as well as to predict future development. Success of these expansions depends on the robustness of circuit-simulation model and its parameters. For this purpose concurrent development with 2D process/device simulation is an important issue.

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