# Investigation of novel junctionless MOSFETs for technology node beyond 22 nm

Peng Xu<sup>a</sup>, Yinghua Piao<sup>a</sup>, Liang Ge<sup>a</sup>, Cheng Hu<sup>a</sup>, Lun Zhu<sup>a</sup>, Zhiwei Zhu<sup>a</sup>, David Wei Zhang<sup>a</sup>, Dongping Wu<sup>a</sup>

<sup>a</sup> State Key Laboratory of ASIC and System, Fudan University, Shanghai 200433, People's Republic of China (e-mail of the corresponding author Dongping Wu: <u>dongpingwu@fudan.edu.cn</u> and Zhiwei Zhu: zhiwei zhu@fudan.edu.cn)

In this paper, junctionless MOSFETs with un-uniformly doped source/drain and channel regions have been thoroughly investigated. Un-uniformly doped junctionless MOSFET has the same type of dopants in source/drain and channel while the doping level in the source/drain is much higher than that in the channel. Performance of DC, AC and variability of the uniformly doped, un-uniformly doped junctionless and conventional P-N junction MOSFETs featuring a gate length of 16 nm has been obtained by device simulation through Silvaco software package. Compared with uniformly doped junctionless MOSFETs, un-uniformly doped junctionless MOSFETs exhibit significantly improved overall DC and AC performance as well as lower sensitivity to variations of channel thickness. In addition, un-uniformly doped junctionless MOSFETs also demonstrate marginal performance enhancement compared with conventional P-N junction MOSFETs.

# **INTRODUCTION**

Recent announcement of the success of Intel's 22 nm node IC symbolizes that the semiconductor industry is stepping into 22 nm technology node and beyond (1). According to International Technology Roadmap for Semiconductors (ITRS), 3D or planar FDSOI device architectures are likely to be implemented for technology nodes beyond 22 nm, owing to their superior performance in control of device short channel effects (2). For either 3D or FDSOI devices, formation of ultra-shallow junctions and low series resistances at source/drain regions is a must since the source/drain regions are playing more critical role in device performance for ultra-scaled MOSFETs. MOSFETs without junctions, i.e., the junctionless MOSFETs, have been recently proposed in order to overcome the challenges in formation of ultra-shallow junctions (3-9). The source/drain and channel regions of the proposed junctionless MOSFETs are uniformly doped with only one type of dopants (P or N-type), hence, there is no P-N junction existing between source/drain and channel. Junctionless MOSFETs having near-ideal subthreshold slope and extremely low leakage currents have been reported, however, they have demonstrated lower driving current and transconductance compared with conventional P-N junction MOSFETs as a result of higher source/drain series resistances and lower channel carrier mobility (10). In order to mitigate the aforementioned performance degradation associated with the uniformly doped junctionless MOSFETs, un-uniformly doped junctionless MOSFETs have been recently proposed and investigated (11). Un-uniformly doped junctionless MOSFET has the same type of dopants in source/drain and channel while the doping level in the source/drain is much higher than that in the channel. In this paper, the performances of DC, AC and variability against channel thickness of un-uniformly doped junctionless MOSFETs are thoroughly investigated and compared with that of conventional MOSFETs and uniformly doped junctionless MOSFETs. Furthermore, the potential of applying un-uniformly doped junctionless MOSFETs in technology nodes beyond 22nm is discussed.

# DEVICE STRUCTURE AND SIMULATION SETUP

Silvaco software package is used to construct the device structures and simulate the performance of DC, AC and variability for the un-uniform junctionless, uniform junctionless and conventional nMOSFETs. In order to acquire a direct and simple insight about the impact of device structures on device performances, two dimensional fully depleted double-gate device structures are employed to emulate three-dimensional device structures which are assumed to be applied in technology nodes beyond 22 nm. The geometrical parameters and doping profiles of the simulated nMOSFETs are shown in Figure 1 (a) and (b), respectively.



Figure 1. Schematic cross-section (a) and the net doping profiles along the surface of the channel (b) of the simulated nMOSFETs.

TABLE I. The physical parameters used for the simulated MOSFETs.

THE DID R. The physical parameters used for the simulated highlight.			
nMOSFETs	Conventional	Un-uniform junctionless	Uniform junctionless
Channel doping (atom/cm <sup>3</sup> )	1e18(B)	1e18(As)	4e19(As)
Source/drain doping (atom/cm <sup>3</sup> )	4e19(As)	4e19(As)	4e19(As)
Junction lateral abruptness (nm/decade)	1.6	1.6	N/A
Gate work-function (eV)	4.575	4.6	5
Permittivity of gate dielectric	4.875	4.875	4.875

All of the simulated MOSFETs have a physical gate length of 16 nm, a 4-nm thick body silicon and a 1-nm thick gate dielectric. Physical parameters of the simulated three-types of MOSFETs are listed in TABLE I. The permittivity of the gate dielectric is set to be 4.875 in order to obtain an effective gate oxide thickness of 0.8 nm. The differences among the un-uniform junctionless, uniform junctionless and conventional MOSFETs mainly lie in the channel region: the uniform junctionless MOSFET has a channel doping level of 4e19 atom/cm<sup>3</sup> while the un-uniform junctionless and conventional MOSFETs have a lower channel doping level of 1e18 atom/cm<sup>3</sup>. The source/drain regions of the three types of the MOSFETs are equally doped at 4e19 atom/cm<sup>3</sup> level in order to guarantee that impact of the source/drain region on the transistor performance is fairly

comparable for all of the MOSFETs. In order to achieve comparable threshold voltage values ( $V_T$ ), the work-function of the simulated metal gates for un-uniform junctionless uniform junctionless and conventional MOSFETs are set to be 4.6eV, 5eV and 5.575eV, respectively.

# **RESULTS AND DISCUSSIONS**

#### DC characteristics

The  $I_D$ -V<sub>G</sub> characteristics of the un-uniform junctionless, uniform junctionless and conventional nMOSFETs in saturation region (V<sub>DS</sub>=0.8V) and linear region (V<sub>DS</sub>=0.1V) are shown in Figure 2(a) and Figure 2(b), respectively. Due to the proper setting of work-function of the gate electrodes, all of the three types of MOSFETs exhibit almost identical saturation threshold voltages around 0.21V.



Figure 2.  $I_D$ -V<sub>G</sub> characteristics of the un-uniform junctionless, uniform junctionless and conventional nMOSFETs at V<sub>DS</sub>=0.8V (a) and 0.1V (b).

As shown in Figure 2, the un-uniform junctionless MOSFET demonstrates a little higher drive current than that of conventional MOSFET while the uniform junctionless MOSFET exhibits lowest drive current than both types of junctionless MOSFETs. This phenomenon can be explained as follows.

The channel concentration of the un-uniform junctionless MOSFET (1e18 atom/cm<sup>3</sup>) is much lower than that of the uniform junctionless MOSFET (4e19atom/cm<sup>3</sup>), hence the effective electron mobility of the un-uniform junctionless MOSFET at similar electric field is higher than that of the uniform junctionless MOSFET. As a consequence, the uniform junctionless MOSFET demonstrates a lower drive current than the un-uniform counterpart. Compared with the conventional MOSFET, the slight higher drive current of the un-uniform junction MOSFET could be attributed to its slightly lower vertical electric field which will be shown in subsequent section. The lower vertical electric field will in turn lead to higher electron mobility as well as drive current.

Based on the data presented in Figure 2, the drain induced barrier lower (DIBL) values of the un-uniform junctionless, uniform junctionless and conventional MOSFETs are extracted to be 10mV, 20mV and 10 mV, respectively. The subthreshold slope (SS) values of the un-uniform junctionless, uniform junctionless and conventional MOSFETs are extracted to be 63.1, 65.8 and 63.4 mV/dec., respectively. Therefore, it can be concluded that the un-uniform junctionless MOSFET can even potentially possess

marginally better short channel control than the uniform junctionless MOSFET. The worst short channel control for the uniform junctionless MOSFET is attributed to its high doping concentration in the channel. The transconductances of the three types of the MOSFETs in saturation and linear regions can be derived from Figure 2 and are shown in Figure 3(a) and Figure 3(b), respectively. As expected, the un-uniform junctionless MOSFET demonstrates slightly higher peak transconductance than the conventional MOSFET and significantly higher peak transconductance than the uniform junctionless MOSFET.



Figure 3. Transconductance of the un-uniform junctionless, uniform junctionless and conventional nMOSFETs at  $V_{DS}=0.8V$  (a) and 0.1V (b).

The electric fields with a drain voltage of 0.8V along the surface of the channel are shown in Figure 4(a) for  $V_G$ =2.0V and Figure 4(b) for  $V_G$ =0V. When  $V_G$  is biased at 2V, the un-uniform junctionless MOSFET shows significantly higher vertical electric field than uniform junction MOSFET and marginally lower electric field than conventional MOSFET. Interestingly, when the MOSFETs are operated in off-state ( $V_G$ =0V), the ununiform junctionless MOSFET exhibits substantially lower electric field than uniform junctionless MOSFET and marginally higher electric field than conventional MOSFET.



Figure 4. Surface electric fields of the un-uniform junctionless, uniform junctionless and conventional nMOSFETs at  $V_G=2.0V$  (a) and 0V (b).

### AC characteristics

The gate-to-source ( $C_{GS}$ ) and gate-to-drain ( $C_{GD}$ ) capacitances of the un-uniform junctionless, uniform junctionless and conventional nMOSFETs at  $V_{DS}$ =0.8V is shown in Figure 5. It is clearly shown that  $C_{GD}$  and  $C_{GS}$  of the un-uniform junctionless MOSFET is very similar to those of the conventional MOSFET while the uniform junction MOSFET shows a significantly higher  $C_{GS}$  at on-state.



Figure 5.  $C_{GS}$  and  $C_{GD}$  vs.  $V_G$  of conventional, un-uniform junctionless and uniform junctionless nMOSFETs at  $V_{DS}=0.8V$ .

The characteristics of cut-off frequency vs.  $V_G$  of the three types of the MOSFETs are shown in Figure 6. Interestingly, the un-uniform junctionless MOSFET shows highest cut-off frequencies at interested gate voltage range, which could be mainly attributed to its relatively higher transconductance.



Figure 6. Cut-off frequency vs.  $V_G$  of the un-uniform junctionless, uniform junctionless and conventional nMOSFETs at  $V_{DS}$ =0.8V.

#### Variability

The  $I_D$ -V<sub>G</sub> characteristics of conventional, un-uniform junctionless and uniform junctionless MOSFETs with 3, 4 and 5 nm channel thicknesses are shown in Figure 7. V<sub>T</sub>, SS and GIDL leakage current of un-uniform junctionless and conventional MOSFETs are found to be rather insensitive to the variation of channel thickness compared with those of uniform junctionless MOSFETs.



Figure 7.  $I_D$ - $V_G$  characteristics of the un-uniform junctionless, uniform junctionless and conventional MOSFETs with various channel thickness at  $V_{DS}$ =0.1V (channel thickness increases from 3nm to 5nm along the direction of the arrows).

### Conclusions

Owing to the decoupling of the doping level in the channel and source/drain regions, novel un-uniform junctionless MOSFET is shown to have clearly improved drive current, transconductance, cut-off frequency and short channel control than the uniform junctionless MOSFET. In addition, Un-uniform junctionless MOSFET demonstrates much lower sensitivity to variations of channel thickness. Compared with conventional P-N junction MOSFET, un-uniform junctionless MOSFET also demonstrates marginally better drive current, peak transconductance and cut-off frequency. The performance gain of the un-uniform junctionless MOSFET over the conventional MOSFET is mainly attributed to its lower on-state surface electric field gate. Therefore, un-uniform junctionless MOSFET is a strong candidate to replace conventional P-N junction MOSFET for technology nodes beyond 22 nm.

# Acknowledgments

This work was financially supported by "National S&T Major Project 02" (Project No.

2009ZX02035-003), the National Natural Science Foundation of China (Grant No.

61176090 ) and the Program for Professor of Special Appointment (Eastern Scholar) at Shanghai Institutions of Higher Learning.

### References

- 1. http://www.intel.com/content/www/us/en/silicon-innovations/intel-22nm-technology.html.
- 2. International Technology Roadmap for Semiconductors (ITRS), 2010 update, http://www.itrs.net.
- 3. J.-P. Colinge, et al, Nature Nanotechnology, 5, pp. 225-229 (2010).
- 4. C.-W. Lee, et al, *Solid-State Electronics*, **54**(2), pp. 97-103 (2010).
- 5. C.-W. Lee, et al, Appl. Phys. Lett., 94(5), 053511/1-2 (2009).
- 6. C.-W. Lee, et al, *Solid-State Electronics*, **51**, pp. 505-510 (2007).
- 7. C.-W. Lee, et al, *Solid-State Electronics*, **52**, pp. 1815-1820 (2008).
- 8. J.-P. Colinge, et al, Appl. Phys. Lett., 96, 073510 (2010).
- 9. Y. Cui, et.al, Nano Lett. 3(2), pp. 149-152 (2003).
- 10. X. Qian, et al, Intel. Conf. IC Design & Technology (2011).

- 11. P. Razavi, et al, 2011 12th International Conference on Ultimate Integration on Silicon, pp.122-125 (2011).
- 12. Rios, R, et al, IEEE Electron Device Letters, **32**(9), pp.1170-1172 (2011).