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Development of Digital Signal Processing Platform for Digital Hearing Aid

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ABSTRACT: There has been a tremendous growth for the past few years in the field of VLSI and real time signal processing. Number of signal processing algorithms have been developed which allow the user to process real time signals such as speech to accomplish the signal with desired quality. Development of CMOS technology provides wide selection of low power FPGAs to be used in Digital system design. This paper introduces an efficient method to design a Digital Programmable Hearing Aid system working in association with Analog interface module. Real time signal processing algorithms such as Feedback and echo cancellation, Adaptive filtering , Dynamic range compression, Digital filter for decimation along with FFT and IFFT algorithms have been discussed using a 32 bit RISC processor core and hardware digital signal processing block, both residing in a Xilinx FPGA. Hardware configuration and software implementation are discussed in detail. Xilinx Spartan3, FPGA is used in system design. Spartan3 board has inbuilt ADC inside the chip so there is no need to use external CODEC system in design. Finally the challenges and the future work for additional improvement are discussed.

KEYWORDS: Adaptive filtering, Feedback cancellation DRC, Hearing threshold, FPGA, RISC core, FFT, IFFT.

I.INTRODUCTION

Traditionally Digital signal Processing Algorithms are developed using signal processing chip (DSP chip) for lower rate applications. For higher rate, Application Specific Integrated Circuits (ASIC) are used to process the real time signal. The advent of FPGAs created a new era for DSP engineers. Along with low cost, it provides better functionality in terms of speed and power consumption. System design cycle time also shrinks with large amount when FPGA is used to process the real time signal such as audio, video and image.

Implementation of real time speech signal processing algorithms for digital hearing aid using FPGA as a hardware platform reduces the power requirement which is a major issue in consumer electronics devices.

Digital Hearing Aid process the speech signal in the same manner as human ear functions. Human ear has three main part outer ear, middle ear and inner ear. Outer ear receives the signal from outside world and direct towards the middle ear, in Digital Hearing Aid directional microphone performs this task. Middle ear acts as an impedance matching network and as an amplifier. Main function which middle ear performs is the distribution of frequency bands into several small bands. Digital Hearing Aid uses some kind of impedance matching network along with the amplifier. Signal processing algorithms such as DFFT, FFT, Uniform or Non-Uniform filter bank is implemented on FPGA to split the entire frequency band into several small bands so that desired band of frequency can be manipulated as per the need of patient. This provides the flexibility to the doctors to customize the hearing parameters of a patient on the same hearing aid without any replacement of component while conventional analogue hearing aid does not provide this flexibility. Inner ear functions as a spectrum analyser which encodes the signal at various frequency, amplify the low amplitude signal and compress the signal which is above the hearing capability of human , minimize the noise power, makes different nerve cells resonates and finally transmits the short pulses to the brain. In Digital Hearing Aid these functions are performed by various signal processing algorithms such as adaptive filtering, feedback and echo cancellation, dynamic range compression, and finally using the IFFT algorithm and DAC, frequency domain signal converted back into continuous time domain and delivered to the speaker.

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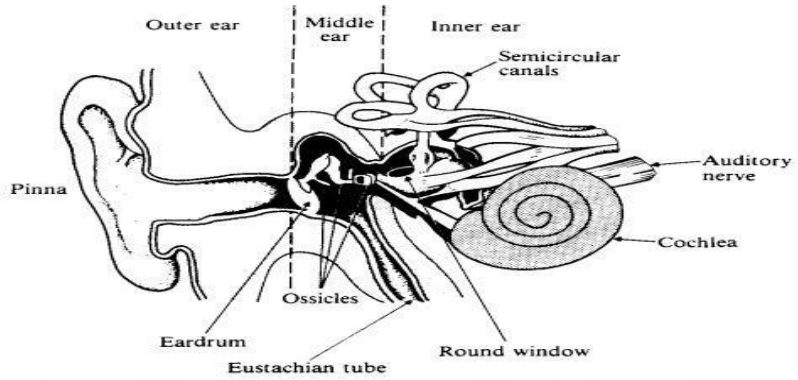

Fig. 1 Structure of Human ear

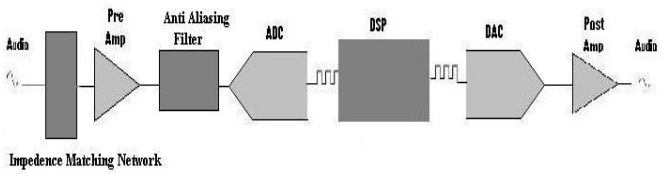

Fig 2 structure of digital hearing aid

Figure 1 and 2 presents a pictorial comparison between human ear and Digital Hearing Aid.
In this design Xilinx's Spartan 3, FPGA platform is used which has 32 bit RISC processor core support to process the real time speech signal. It has inbuilt memory unit to store the DSP algorithms. Two types of host interface can be used in design, one is USB physical interface and another one is serial UART interface with 9600 bps rate. Program can be downloaded in the device using PC along with suitable interface. Xilinx ISE tools along with system generator DSP support is used in design. All the Signal Processing algorithms can be designed using MATLAB signal processing toolbox.
Section 1 introduces the idea behind DHA functionality and its similarity with human ear. Section 2 is the literature review part in which various techniques which have been used in hearing aids is discussed. Section 3 compares hearing profile of impaired patient with normal person. In section 4, various DSP algorithms are discussed. Section 5 contains details of hardware and software implementation. Conclusion and Reference are introduced in subsequent sections.

II. LITERATURE REVIEW

The application domain which we are considering is the audio signal processing, more specifically the digital hearing aids. Conventional analogue hearing aids is designed in early 1950. [5]
After that so many improvements have introduced to make the analogue hearing aid more efficient but the main problems remain unchanged which are flexibility and hard wired circuitry. Up until 1986 the same hearing aids based on analogue circuitry was in use. The first integrated circuit which was used with same analogue hearing aid was designed in the same year. [6, 10]
Traditionally the digital hearing aids are implemented on Application Specific Integrated Circuit (ASIC). Power consumption of ASIC based Digital Hearing Aids are between 0.5 to 1mW (at 1.0V supply). [9]. With the advancement in audiology many speech processing algorithms has been developed such as Dynamic Range Compression, Echo cancellation, Feedback cancellation, Adaptive filtering, Noise reduction etc. [5] These algorithms increase the efficiency of Hearing Aids but with more complexity and space requirement, and because implementation of digital hearing aid on ASIC is much tedious task and also more power consuming. For this reason industries are push towards to obtain an ultra low power DSP platform which can provide less power consumption and less area constraint. [5, 10]
Comparison of power consumption in analogue and Digital (ASIC based) Hearing aids along with area coverage is given in following table 1.Since ASICs are expensive enough and not flexible in terms of verification of the system, FPGAs are the better option for Digital Hearing Aid System. It provides higher level of flexibility to the designer along with low power consumption in case of ASICs based digital hearing aids. FPGA is a type of programmable logic

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device (PLD) which can be reconfigured several times. [4] Compared to the DSP chips which implement the algorithms in "VON NEUMANN" style, FPGA implements algorithms in much stronger parallelism as its hardware is inherently parallel. [4,12] Due to parallel computing of FPGA, its computational speed is very high which is a key factor of FPGA to be used in real time signal processing system.

Table 1:
Analog and Digital Hearing Aid comparison

Parameters	Analog Hearing Aid	ASIC based Digital Hearing Aid
Power consumption (mW)	40 to 50 mW	1 to 10mW
Current	2 to 4 mA	17 μA
Area	5-10 cubic centi meters	7.3 cubic milli meters
Cost per Unit	$ 395 to $ 900	$ 1700 to $ 4750
Basic circuitry	Fixed hard wired	Flexible, programming facility

III. HEARING PROFILE OF IMPAIRED PERSON

Hearing impaired person has higher hearing threshold as compared to the normal person. So Digital Hearing aids are required to boost the signals which come under the hearing threshold. Signals which are higher than the higher threshold value of the patient needs to be attenuated so that signal can remain under the dynamic range of patient.

A. *Dynamic Range and Audibility*

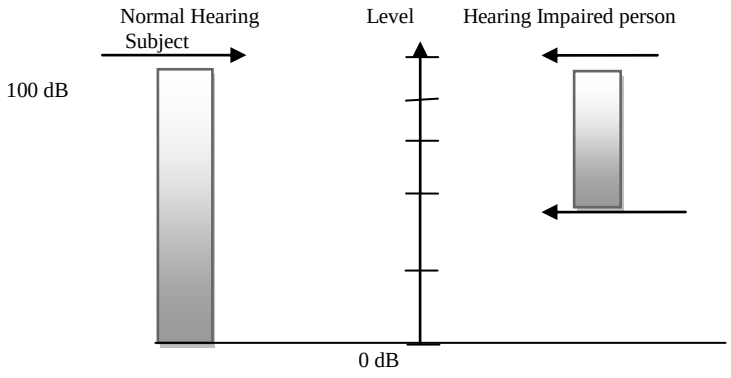

Fig. 3: Dynamic Range Comparison

As per the above figure hearing impaired person has higher hearing threshold compared to the normal person. Digital hearing aids are required to amplify the signals which fall below the dynamic range of patient.

B. *Dynamic Range Compression*

In Digital Hearing Aid compressor compress the environmental sound level so that it comes under the decreased dynamic range of impaired person. The important parameters of compression systems are *Compression Threshold, Compression Ratio, Attack Time* and *Release Time*.

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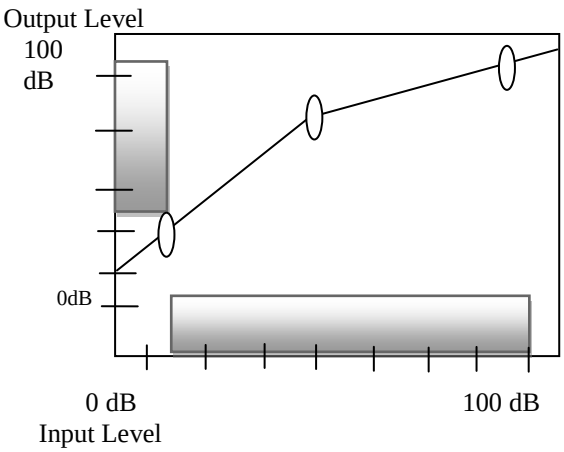

Fig. 4: dynamic range compression

Given figure gives the idea about how the dynamic range compression algorithm is useful in hearing aid. Horizontal axis represents the dynamic range of normal person which needs to be reduced in case of hearing impaired person. This function is performed by DRC algorithm in the considered hearing aid.

C. *Signal to noise ratio* (*SNR)*

Hearing impaired person needs larger signal to noise ratio (5 to 10 dB) for speech understanding in noisy environment.

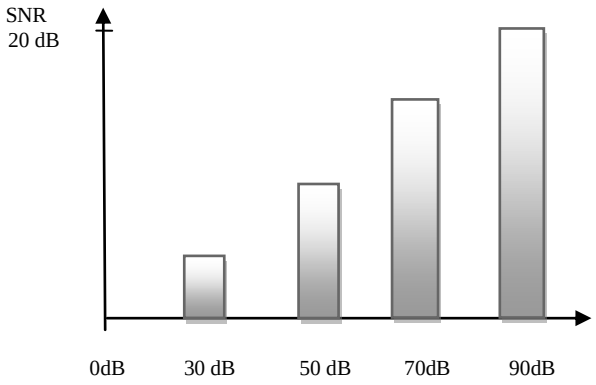

Fig. 5: SNR vs. Hearing loss

Above graph gives the relationship between the values of SNR required and the degree of Hearing loss present in particular patient.

IV. SIGNAL PROCESSING ALGORITHMS DEVELOPMENT

Most of the signal processing system which interact with outside world, contain some of signal processing techniques or algorithms. Digital hearing aid system does contain very sophisticated algorithms and digital filters. They also contain various algorithms for transformation of time domain signal into the frequency domain.

The basic purpose of any Digital hearing aid is to amplify the sound of certain frequency band of interest which lies below the hearing threshold of patient and compress the loud signal. [13] There are some well known techniques to do this. The most common techniques are *Uniform Filter banks, Non Uniform Filter banks, Wavelet Transform* and *Fast Fourier Transform.* [6]

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A. *Wavelet transform*

Wavelet transform is widely used transformation in real time application. It is suitable for Digital hearing aid because it works logarithmically. It provides better resolution at lower frequency bands.

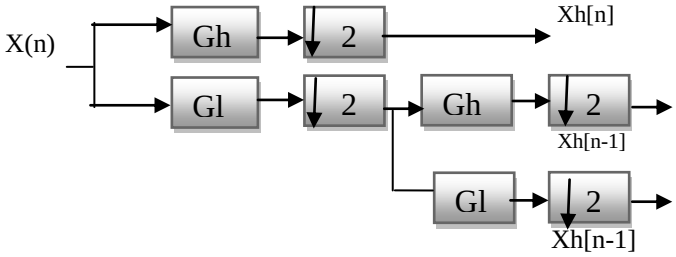

Fig. 6: Wavelet sub band division

In wavelet transform, signal is given to the high pass and low pass filter which is further down sampled by factor 2. The signal from low pass filter is further sampled to obtain better frequency resolution at lower frequency. This process can go further for more frequency bands.

Wavelet transform along with FFT algorithm gives better resolution at lower frequency bands.

B. *Fast Fourier Transform (FFT)*

To transform time domain signal into frequency domain, DFT algorithm is widely used from long time. But the problem with DFT is its mathematical complexity. Fast Fourier Transform provides better option in terms of mathematical complexity in domain transformation. For N point FFT it performs only N *log2N computations while DFT performs N*N computations.

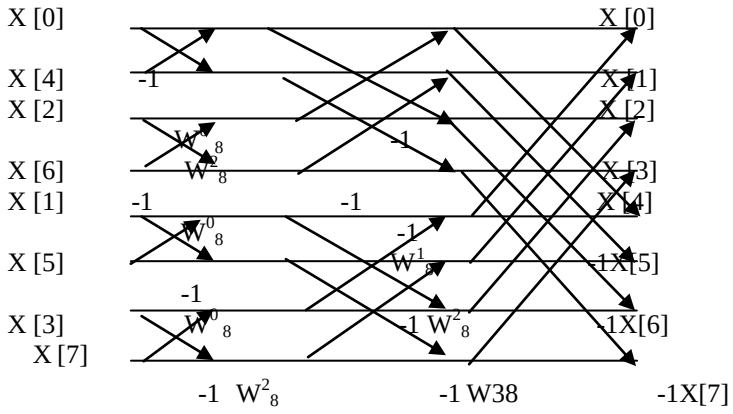

Fig. 7: Decimation in time

1. Invert the bit order of index and arrange it in even and odd index group as shown in fig. 8

In case of decimation in time FFT algorithm is implemented in three steps-

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Sample no.	Natural order	Reverse order	Sample no.
0	000	000	0
1	001	100	4
2	010	010	2
3	011	110	6
4	100	001	1
5	101	101	5
6	110	011	3
7	111	111	7

Fig. 8: Bit order in FFT calculation

1. Calculate the twiddle factor using the equation-

$$W = cos(\theta) + sin(\theta) \quad (1)$$ Where,

$$\theta = -2\pi\ (no.of\ groups) \times (no.of\ butterflies) \quad (2)$$

2. Perform the butterfly operation which will finally represent the frequency on specific indexes.

Butterfly operation could be mathematically represented in form of equations.

$$X(i) = X_e(i) + W_i^N X_0(i) \quad (3)$$

$$X\left(i + \tfrac{N}{2}\right) = X_e(i) - W_i^N X_0(i) \quad (4)$$

After processing the particular band of frequency through various algorithms, signal in frequency domain is converted back into time domain using inverse FFT or IFFT algorithm and input to the DAC.

C. *Dynamic Range Compression (DRC) Algorithm*

The role of DRC algorithm in hearing aid is to map the wide dynamic range of input signal into the reduced dynamic range of hearing impaired person. The basic function of DRC algorithm is to enhance the speech signal such that all the important features of speech signal are above the hearing threshold but at the same time below the discomfort level.
DRC algorithm is basically the multi band DRC algorithm because hearing loss and dynamic range varies with variation in frequency bands. The basic overview of DRC algorithm is given in fig. 10.

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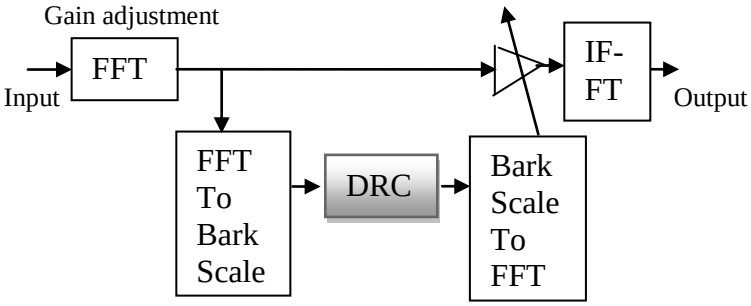

Fig 10: Multi band DRC algorithm

Parameters to be concerned while designing the DRC Algorithms are *Compression Threshold (CT), Compression Ratio (CR), Attack Time*(a_t), *Release Time*(r_t) *and DRC Gain* (G_{dB}^{s})

CT is defined in dB and determined the point where DRC becomes active.
Compression Ratio (CR) determines the degree of compression required for input audio signal.
Attack Time (a_t) is the time taken by compressor to react to increase the input signal level.
Release Time (r_t) is the time taken by the compressor to decrease the level of input audio signal.
DRC Gain (G_{dB}^{s}) is the speech DRC gain selected by the user.
For DRC input signal level is given by the following equation,

$$P_{DRC,dB}^{in,s}(k,l) = 20log_{10}\left(\frac{\left|P_{DRC\,dB}^{in,s}(k,l)\right|}{P_{ref}}\right) \qquad (5)$$

Where k is used to indicate that linear frequency is now mapped to Bark Scale and P_{ref} is the reference sound pressure (20 micro Pascal).

Output level for DRC is given by the following equation no. 6,

$$P_{DRC,dB}^{OUT,S}(k,l) = \begin{cases} P_{lin,dB}(k,l), & if\ P_{DRC,dB}^{in,s}(k,l) < CT \\ P_{cp,dB}(k,l), & \text{if } P_{DRC,dB}^{in,s}(k,l) \geq CT \end{cases} \qquad (6)$$

Where,

$$P_{lin,dB}(k,l) = P_{DRC,dB}^{in,s}(k,l) + (G_{dB}^{s}) \qquad (7)$$

$$P_{cp,dB}(k,l) = CT + \frac{1}{CR}\times\left(P_{DRC,dB}^{in,s}(k,l) - CT\right) + (G_{dB}^{s}) \qquad (8)$$

Using the above mathematical equations one can implement the DRC algorithm for desired value of DRC gain (G_{dB}^{s}).

D. *Adaptive Filtering Approach*

Modern hearing aids size is decreasing day by day, which is desired from an aesthetic point of view. Decrease in size also generate acoustic feedback problem in Digital hearing Aid which results when amplified speech signal from speaker gets picked up by microphone and amplified again. This limits the maximum gain of the hearing aid.
Two techniques are widely in used to overcome the acoustic feedback problem in hearing aid system, i.e., *Forward Suppression* and *Feedback Cancellation.* [2]
Forward Suppression techniques use some kind of notch filter [1, 2] in the forward path to reduce the acoustic feedback. Generally the benefits of notch filters are limited because these techniques operate in forward path which can compromise the frequency response and speech quality of hearing aids.
Feedback Cancellation algorithm is highly researched area in now a day. In this algorithm an acoustic feedback model is developed which predicts the feedback signal in the microphone signal. This predicted feedback signal is then

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subtracted from the microphone signal. Adaptive finite impulse response filter (FIR) is generally used to model the acoustic feedback path in the system. [4, 7]

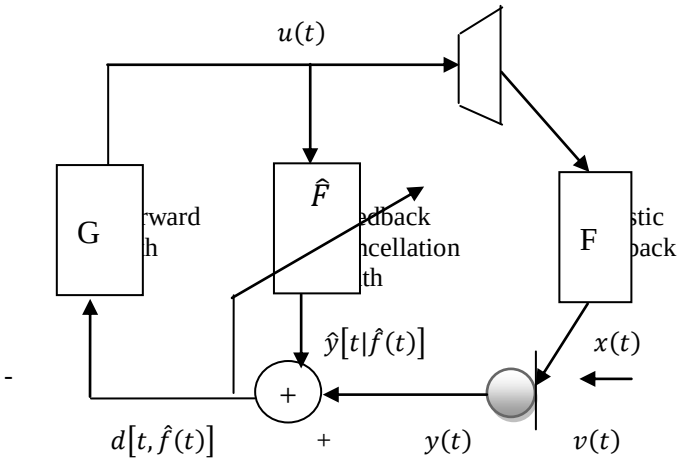

Fig. 11: Adaptive Feedback Cancellation (AFC) algorithm

Microphone signal is given by equation 9.

$$y(t) = v(t) + x(t) = v(t) + F(q,t)u(t) \qquad (9)$$

Where q is the time shift operator and t is the discrete time variable. $F(q,t)$ Is the feedback path between loudspeaker and the microphone, $v(t)$ is the near end signal, and $x(t)$ is the feedback signal.
The forward path $G(q,t)$ maps the microphone signal $y(t)$ after AFC to the loudspeaker signal $u(t)$. It consist of an amplifier with time varying gain K (t) cascaded with linear equalization filter $j(q,t)$ such that,

$$G(q,t) = K(t)j(q,t) \qquad (10)$$

Main aim in adaptive feedback cancellation is to model a finite impulse response (FIR) adaptive filter in parallel with feedback path. The feedback canceller produces an estimate of the feedback signal x (t) which is further subtracted from the microphone signal y(t).
The feedback compensated signal is given by the following equation (11),

$$d(t) = v(t) + \left[F(q,t) - \hat{F}(q,t)\right]u(t) \qquad (11)$$

Some time adaptive filters does not only predict and cancel the feedback component in microphone signal but also some part of near end signal, which gives distorted feedback compensated signal d(t). To overcome this problem, Prediction Error Method (PEM) [3] approach can be used in future design along with AFC.

V. HARDWARE IMPLEMENTATION

All of the Digital Hearing Aid contains almost common hardware units. These are Directional Microphone, some kind of impedance matching network, anti-aliasing filters, pre-amplifier, analog to digital converter, specific processor to support signal processing algorithms, digital to analog converter, post amplifier and speaker. Basic system level diagram is given in the following figure.

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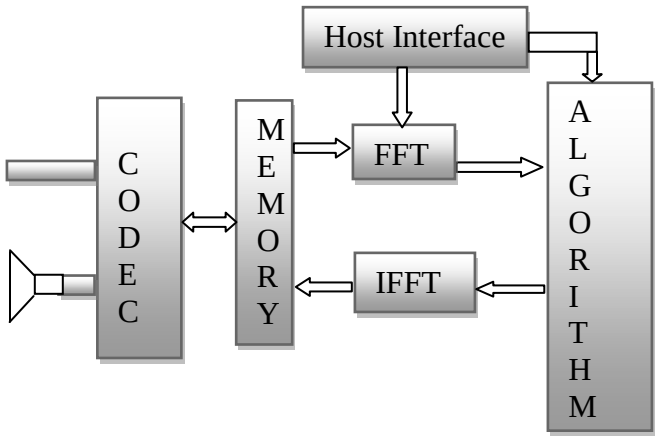

FIG. 12: SYSTEM LEVEL DIAGRAM OF DHA

For the purpose of implementation Xilinx Spartan3 FPGA board is used. It has on board codec which performs ADC and DAC operation. FPGA chip contains memory element to store the samples from ADC. These samples in memory are stored in FIFO manner. 16 samples from FIFO queue are collected and processed through FFT block where time domain signals are converted into frequency domain. According to the user impairment, desired bands of frequency are amplified. Gain value can be changed by doctors using USB or serial UART interface through PC.
After converting the signal from time domain to frequency domain, complex signal processing algorithms such as echo and feedback cancellation, noise reduction, filtering, adaptive filtering cancellation etc. can be used to improve hearing. Finally each frequency bands are converted into time domain by IFFT algorithm and given back to the memory. Samples from memory are input to the DAC and analog output of DAC is delivered to the speaker.

VI. CONCLUSION

The main purpose of this paper is to develop a digital signal processing platform for Digital Hearing Aid device. In the first part hearing profile of a hearing impaired patient is discussed which provides an idea about how can a Digital hearing aid should be customized to meet the patient requirement. In the second part, algorithm for conversion of time domain signal into frequency domain such as wavelet transform and FFT is discussed. In the next part some complex speech processing algorithms such as dynamic range compression and feedback cancellation with Adaptive Filtering approach are discussed. These algorithms give better hearing improvements with high value of signal to noise ratio. Finally hardware and software implementation are discussed.

In real time signal processing latency is the main issue to take care about. Another problem is the limited amount of memory and processing power. Overlap Add and Overlap Save algorithms can be used in future design to overcome these problems. Identifying the feedback path model in case of Adaptive Feedback Cancellation step, correlation between near end signal and loudspeaker signal is the main problem. De-correlating Pre-filters along with AFC algorithm can be used to remove the correlation problem in AFC.

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