Clock and Data Recovery Circuit for 10-Gb/s Asynchronous Optical Packets

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***Abstract*—We demonstrate an all-optical clock and data recovery circuit for short asynchronous data packets at 10-Gb/s line rate. The technique employs a Fabry–Pérot filter and an ultrafast nonlinear interferometer (UNI) to generate the local packet clock, followed by a second UNI gate to act as decision element, performing a logical AND operation between the extracted clocks and the incoming data packets. The circuit can handle short packets arriving at time intervals as short as 1.5 ns and arbitrary phase alignment.**

***Index Terms*—Asynchronous traffic, clock and data recovery (CDR), optical packet switching, ultrafast nonlinear interferometer (UNI).**

I. Introduction and Concept

THE development of high bandwidth applications has imposed requirements on fiber networks, not only in terms of their transmission throughput capacity but also their ability to handle bursty traffic. The concept of optical packet switching has been put forward in order to fulfill the bandwidth efficiency and achieve a higher grade of capacity utilization [1], [2]. Due to the bursty nature of packet traffic and in order for optical packet switching to become implementable, several key functionalities may be best handled in the optical domain. Clock and data recovery (CDR) circuits belong to this set of critical modules, responsible for reliable data reception and information exchange. As data packets originate from different sources and travel different paths before entering a switching node, CDR modules designed for packet switching must be able to handle packet traffic, arriving asynchronously [3].

A typical CDR circuit consists of two discrete elements: a clock recovery circuit used to extract the clock and a decision circuit driven from the extracted clock and used to regenerate the data at its output. For asynchronous packet traffic, clock extraction must be performed separately for each incoming packet, irrespective of its precise phase on arrival, ideally immediately as soon as it arrives and the clock signal must persist only for the duration of the packet.

So far, only electronic solutions have been proposed for CDR implementations [4]–[7]. High-rate CDR has been demonstrated with synchronous traffic using electronic phase-locked loops (PLLs) [4], but PLL circuits require a long time for synchronization and are not appropriate for asynchronous traffic. Electronic implementations capable of handling asynchronous traffic up to 2.5 Gb/s have been demonstrated [5], [6], while a 10-Gb/s CDR circuit requiring several bytes for synchronization has been presented recently [7]. Optical clock recovery circuits have shown remarkable potential for use in an optical CDR circuit, to extract the local clock within a few bits [8] even from high-rate asynchronous packets [9], [10].

In this letter, we demonstrate an all-optical CDR module capable to handle 10-Gb/s asynchronous short packets with very low synchronization overhead. Clock extraction is performed on a packet-by-packet basis using a recently presented unit that consists of a low-finesse Fabry–Pérot (FP) filter and a semiconductor optical amplifier (SOA)-based ultrafast nonlinear interferometer (UNI) gate [8]. The FP filter operates as a passive oscillator and determines both the locking time and the guard-band required between successive data packets, whereas the nonlinear gate operates as an equalizer, smoothing out the amplitude modulation at the output of the FP filter. Data recovery is executed in an additional UNI gate performing an AND operation [11] between the original data and its corresponding clock signal. The AND gate serves as the decision element and contributes in the regeneration of the incoming data packets. This is the first time, to our knowledge, that an optical CDR circuit is demonstrated to operate successfully with short (41-b long), asynchronous 10-Gb/s optical packets, with small guard-bands between them (as short as 1.5 ns). The circuit is self-synchronizing, requires no high-speed electronics, and could be applied for data reception and regeneration purposes.

II. Experiment

The experimental setup is depicted in Fig. 1 and consists of the asynchronous packet flow generator and the data recovery circuit, which comprises a packet clock recovery circuit and an all-optical AND gate. To generate the asynchronous data packets, a distributed feedback (DFB) laser diode (LD1) at 1549.4 nm was used, gain switched at 1.290 75 GHz to provide 8.2-ps pulses after linear compression. This pulse train was modulated with a $2^7 - 1$ pseudorandom binary sequence (PRBS) pattern in a Li:NbO_3 modulator (MOD1) and was inserted in a three-times fiber bit interleaver to generate a pseudodata pattern at 10.326 Gb/s. A second Li:NbO_3 modulator (MOD2), driven by a programmable pulse generator, was used to modulate the PRBS data stream into packets of adjustable length and period. The data packets generated were introduced

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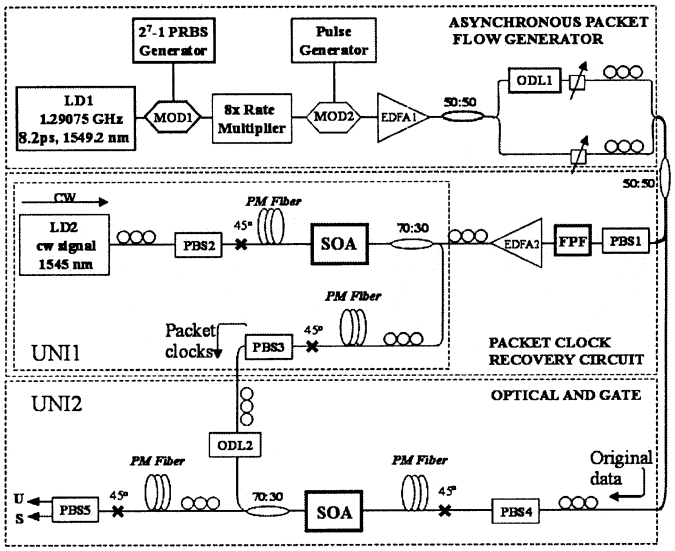

Fig. 1. Experimental setup.

in the asynchronous packet flow generator. This consisted of a 3-dB coupler with fiber lengths at its output, to provide 30.6 ns of differential delay between the two paths before recombination in a second 3-dB coupler. Fine phase adjustment of the packets was achieved with a variable optical delay line (ODL1) inserted in one of the arms of the flow generator and the resulting packet stream was introduced in the CDR circuit. Polarization controllers and a polarization beam splitter (PBS1) were used to copolarize the two signals.

The clock recovery circuit consisted of an FP filter with free spectral range equal to the line rate and finesse equal to 20.7, followed by a UNI gate [8]. Introduction of each data packet into the FP filter, leads to the partial filling of the "0s" in the data stream due to the lifetime of the filter, resulting in an amplitude modulated but-packet clock resembling signal. By inserting this signal into the UNI gate (UNI1) as the control signal, pulse amplitude equalization can be achieved. The UNI gate was powered by a counterpropagating continuous-wave (CW) signal provided by a DFB laser diode (LD2) at 1545 nm and was designed for 10-Gb/s operation. The active nonlinear element of UNI1 was a commercially available (Opto Speed S.A.), 1.5-mm bulk InGaAsP–InP ridge waveguide SOA with 27-dB small signal gain at 1550 nm, 24 dB at 1545 nm, and a recovery time of 100 ps, when driven with 700-mA current. The CW signal plays the role of an optical holding beam [12] and it was used to provide the signal for the packet clock, while its power was adjusted to saturate deeply the SOA. In this fashion, it forces the UNI to operate as a hard limiter, providing at the switch port a nearly equal amplitude clock signal of similar length to the original packet, while at the same time it helps to reduce the SOA recovery time.

The data packets were sampled in a second UNI gate (UNI2), built identically to UNI1, and configured to perform a logical AND operation between the incoming data packets and their corresponding self-extracted packet clocks. A variable optical delay line (ODL2) was used to synchronize the data packets with their equivalent clocks in UNI2 and the received packet data stream was obtained in the switched Port S of UNI2.

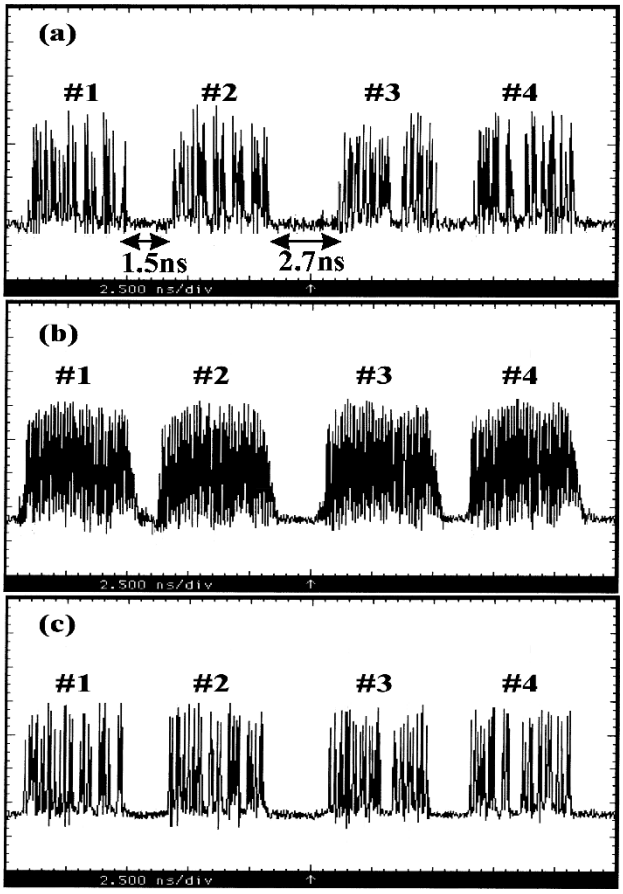

Fig. 2. (a) Incoming asynchronous data packets, (b) recovered packet clocks, and (c) recovered data packets. The time base is 2.5 ns/div.

III. Results and Discussion

By changing the width, period, and delay of the electrical pulse train driving the second modulator, data packets of various length, period, and contents were generated in order to test the performance of the CDR circuit. Fig. 2(a) illustrates a typical sequence of four asynchronous data packets, each containing 41 b (approximately 4.1-ns duration). Packets #1 and #3 are traveling through the same branch of the flow generator and are phase misaligned compared to packets #2 and #4. The time interval between packets #1 and #2 is 1.5 ns while between packets #2 and #3 is 2.7 ns. Fig. 2(b) shows the corresponding recovered packet clocks and Fig. 2(c) shows the received packet stream in the S-port of UNI2. Best operation was achieved with 900 μW of optical power from the CW source and 100-fJ/pulse energy from the control signal for UNI1, 2-fJ/pulse energy from the packet flow signal, and 22 fJ/pulse from the recovered clock for UNI2.

Fig. 3 provides information about the quality of the recovered clock and data and reveals the regenerative properties of the configuration. Fig. 3(a) shows one of the incoming packets (packet #4), while Fig. 3(b) shows the eye diagram of the asynchronous data stream for a random phase adjustment in the packet flow generator. Severe amplitude modulation on the data pulses is evident in both figures and is caused by the bit interleaving process of the eight times rate fiber multiplier. Fig. 3(c) illustrates the corresponding recovered clock for packet #4. The clock rises

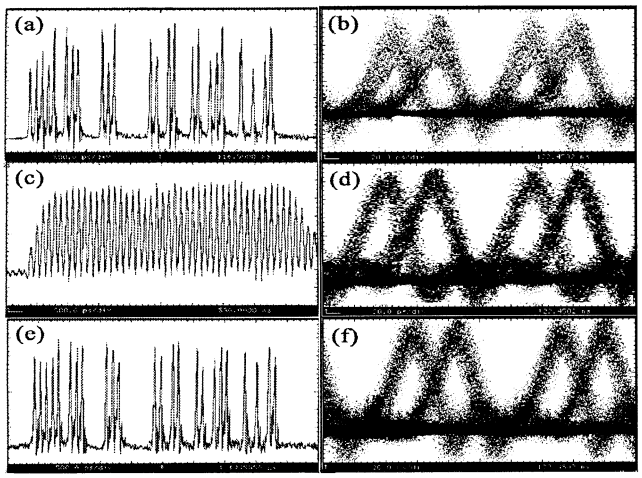

Fig. 3. Single-packet pulse trace and eye diagram of the asynchronous signal for (a), (b) original data, (c), (d) recovered clock, and (e), (f) recovered data, respectively. The time base for pulse traces is 500 ps/div and for the eye diagrams 20 ps/div.

within 2 b and falls to 1/e within 8 b, while the amplitude modulation is reduced to 1.5 dB in the frame of the 41 more intense pulses. Both rise and fall times are due to the storage property of the FP filter and are determined by its finesse. The recovered, asynchronous packet clock signal is displayed in Fig. 3(d) and its eye shows significant improvement. Fig. 3(e) presents the received packet #4 and shows an obvious reduction of its amplitude modulation in comparison to the original packet #4 of Fig. 3(a). Fig. 3(f) shows the eye diagram and verifies the improvement of the recovered asynchronous packet stream at the output of UNI2. The CDR circuit was evaluated for different settings of the relative phase between packets and always provided similar performance.

The timing jitter performance of the CDR circuit was analyzed with a 40-GHz photodiode and a microwave spectrum analyzer. This method provides better accuracy than jitter measurements obtained from the eye diagram with the sampling oscilloscope [13]. The recovered data displayed timing jitter of 600 fs, reduced from the timing jitter of 1.5 ps of the original data. By comparison, the timing jitter of the recovered packet clock signal was 300 fs.

The regenerative properties of this unit originate from the nonlinear characteristics of the gate, when triggered by almost jitter-free clock pulses. The input data pulses of unequal amplitude experience the saturated gain of the amplifier, resulting in switched pulses of equal amplitude at the output of the gate. Furthermore, the tolerance of the nonlinear transfer function of the interferometer to small timing fluctuations results in effective retiming of the output signal.

IV. Conclusion

We have presented an all-optical CDR circuit that recovers clock and data from short asynchronous optical packets at 10-Gb/s line rate, arriving at time intervals of only 1.5 ns. The circuit is based on simple optical filtering and switching elements, requires no high-speed electronics, and provides improved bandwidth efficiency since it acquires synchronization within a few bits regardless of the phase variation between successive packets. Moreover, the rise and fall times of the module are determined as a number of bits, independent of the line rate and the packet length. Given that optical gates have been shown to perform successfully at higher rates [11] and given the existence of techniques to reduce the recovery time of SOAs [12], [14], [15], it is expected that the operation of the proposed CDR module should be possible to line rates beyond 10 Gb/s. The amplitude and timing jitter suppression properties of the circuit suggest that it could be used in a receiver or regenerator.

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