

# Design and Implementation of a Multiplierless Reconfigurable DFT/DCT Processor

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**Abstract** - A Multiplierless Reconfigurable DFT/DCT Processor (MRP) design suitable for multicarrier applications is presented. The MRP implementation is based on a Reconfigurable Systolic Array (RSA) architecture that supports N-point DFT or DCT computations. All multiplication blocks in the MRP circuit have been implemented using the CSE-BitSlice technique to reduce hardware usage, and power consumption. Simulation results show that the MRP DFT circuit implementations can be used in most OFDM modulation realizations required by broadband communication systems and compression schemes of major digital video standards. The reconfigurability of the MRP makes it suitable for Shape Adaptive DCT (SA-DCT) computations required by object based video coding systems.

## I. INTRODUCTION

In today's communications systems, hardware solutions that offer computational flexibility are needed to enable the systems to operate in a multi-standard and multi-mode environment. Furthermore, efficient circuit implementation to achieve low hardware usage is essential to many wireless applications where cost and power consumption is critical to system development. For digital video applications, block-based DCT is used in the data coding process required by many compression standards such as JPEG, MPEG-1 and MPEG-2. However, other video standards such as MPEG-4 require a flexible DCT processor that supports shape adaptive DCT (SA-DCT) computations for object-based video coding [1-3]. For broadband communications, the DFT technique has been widely employed in the modulation/demodulation of OFDM subcarriers. A number of reconfigurable FFT architectures proposed for OFDM realization in the 802.11, DAB, DVB, ADSL and VDSL standards have been published in the literature [4-5]. Reconfigurable architectures that support both FFT and DCT modes of operation have also been proposed for broadband and multimedia applications [6-7]. Implementations of DFT and DCT using array multipliers result in circuits with high hardware complexity. As a result, design techniques that help to minimize or eliminate the use of multipliers to achieve circuits with low hardware usage are essential for low power broadband and multimedia applications.

In this paper, a circuit that is reconfigurable and supports DFT and DCT modes of operation required by different OFDM standards and digital video applications is presented. The computation of N-point DFTs for OFDM modulation-

demodulation of subcarriers in multiple radio standards such as DAB, DVB, VDSL, and ADSL can be carried out by an MRP circuit. The MRP can also be configured to compute DCT for video compression applications. The MRP has been designed and implemented on FPGAs with all multiplication operations carried out by building blocks designed using the CSE-BitSlice technique [8].

## II. RSA FOR DFT AND DCT COMPUTATIONS

In this section, configuration techniques related to DFT/DCT implementations on the RSA architecture in order to achieve low arithmetic complexity are described [9]. The DFT of a finite duration sequence  $x(n)$  of length  $N$  is expressed by the following equation:

$$Y_{DFT}(k) = \sum_{n=0}^{N-1} x(n) e^{-\frac{j2\pi nk}{N}} \quad k = 0, \dots, N-1 \quad (1)$$

The DCT of the sequence  $x(n)$  is calculated as the real part of the DFT of  $z(n)$  multiplied by  $(k)$  and a twiddle factor  $W_{2N}^{k/2}$  as follows [10]:

$$\begin{aligned} Y_{DCT}(k) &= \operatorname{Re} \left( \alpha(k) W_{2N}^{\frac{k}{2}} \sum_{n=0}^{N-1} z(n) e^{-\frac{j2\pi nk}{N}} \right) \quad k = 0, \dots, N-1 \\ Y_{DCT}(k) &= \operatorname{Re} \left( \alpha(k) W_{2N}^{\frac{k}{2}} DFT(z(n)) \right) \end{aligned} \quad (2)$$

where

$$\begin{cases} z(n) = x(2n) \\ z(N-n-1) = x(2n+1) \quad n = 0, \dots, \frac{N}{2}-1 \\ \alpha(0) = \sqrt{1/N} \quad ; \quad \alpha(k) = \sqrt{2/N} \end{cases}$$

If  $N$  is a multiple of four, (1) can be rewritten as follows:

$$Y_{DFT}(k) = S_1(n) + (-j)^k S_2(n) + \left( \sum_{n=1}^{\frac{N}{4}-1} (S_3(n) + S_4(n)) * a(n) + j \sum_{n=1}^{\frac{N}{4}-1} (S_3(n) - S_4(n)) * b(n) \right) \quad (3)$$

where

$$\begin{aligned}
S_1(n) &= x(0) + (-1)^k x\left(\frac{N}{2}\right); S_2(n) = x\left(\frac{N}{4}\right) + (-1)^k x\left(\frac{3N}{4}\right) \\
S_3(n) &= x(N-n) + (-1)^k x\left(\frac{N}{2}-n\right) \\
S_4(n) &= x(n) + (-1)^k x\left(\frac{N}{2}+n\right) \\
a(n) &= \cos \frac{2\pi nk}{N}; b(n) = \sin \frac{2\pi nk}{N}
\end{aligned}$$

The output sequences  $Y(N-k)$ ,  $Y(N/2+k)$ , and  $Y(N/2-k)$  can be inferred to be as follows:

$$\begin{aligned}
Y_{DFT}(N-k) &= S_1(n) + (j)^k S_2(n) + \\
&\left( \sum_{n=1}^{\frac{N}{4}-1} (S_3(n) + S_4(n)) * a(n) - j \sum_{n=1}^{\frac{N}{4}-1} (S_3(n) - S_4(n)) * b(n) \right) \quad (4)
\end{aligned}$$

$$\begin{aligned}
Y_{DFT}(N/2+k) &= S_1(n) + (-j)^{\frac{k+N}{2}} S_2(n) + \\
&(-1)^n \left( \sum_{n=1}^{\frac{N}{4}-1} (S_3(n) + S_4(n)) * a(n) + j \sum_{n=1}^{\frac{N}{4}-1} (S_3(n) - S_4(n)) * b(n) \right) \quad (5)
\end{aligned}$$

$$\begin{aligned}
Y_{DFT}(N/2-k) &= S_1(n) + (j)^{\frac{k+N}{2}} S_2(n) + \\
&(-1)^n \left( \sum_{n=1}^{\frac{N}{4}-1} (S_3(n) + S_4(n)) * a(n) - j \sum_{n=1}^{\frac{N}{4}-1} (S_3(n) - S_4(n)) * b(n) \right) \quad (6)
\end{aligned}$$

As seen from the above equations, by factoring out expressions that multiply a common coefficient, a significant number of complex multiplications have been eliminated. It has also been shown that each set of output sequences  $Y_{DFT}(k)$ ,  $Y_{DFT}(N-k)$ ,  $Y_{DFT}(N/2+k)$ , and  $Y_{DFT}(N/2-k)$  can be calculated simultaneously with  $N/4$  complex multiplication operations. For an  $N$ -point DCT, where  $N$  is a multiple of four, each set of four output sequences  $Y_{DCT}(k)$ ,  $Y_{DCT}(N-k)$ ,  $Y_{DCT}(N/2+k)$ , and  $Y_{DCT}(N/2-k)$  can be calculated simultaneously with  $(N/4)+4$  complex multiplication operations. A more detailed description of the RSA configurations for DFT computations can be found in [9].

### III. MULTIPLIERLESS RECONFIGURABLE DFT/DCT PROCESSOR DESIGN

#### A. The MRP Architecture

In this section, the MRP designs based on the RSA architecture depicted in [9] are presented. The MRP design consists of an access control block and an RSA building block comprised of an 8-by-4 array of processing element (PE) and switch (SW) cells as shown in Fig. 1.

The 8-by-4 RSA building block is the MRP's computational engine for  $N$ -point DFTs/DCTs. There are two main building blocks in the RSA architecture: the PE and the SW. The PEs in the array are interconnected with one another by a network of switches. The PE and SW modes of operations are loaded into the array under the command of the access control block (AC). The DFT/DCT coefficients are also loaded into the PE cells based on the addresses generated by the AC block. The configuration data and the coefficients can be shifted into the array in real time.

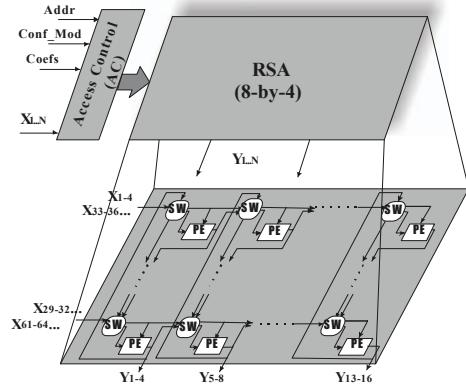


Fig. 1. Architecture of the multiplierless reconfigurable DFT/DCT processor.

This RSA array can be configured to compute a 16-point DFT in parallel. The array also supports  $N$ -point DFT computations for  $N$  larger than 16 based on sequential modes of operation. The MRP enables 32 input data samples to be shifted into the circuit on every clock cycle. Depending on the configuration mode, a set of 4 input data samples shifted into the PE cell is combined and the result multiplied by the factored coefficient. The products generated by the multiplication process in the PE cell are then combined with partial results shifted in from the PE cell on the north side to produce a set of partial results on every clock cycle. For sequential mode of operation, the 16 partial results shifted out of the RSA block are looped back into the PE cells in the first row of the array as shown in Fig. 1. Thus for  $N$  equal to 8 or 16, one clock cycle is needed to shift out a complete set of DFT outputs. For  $N$ -point DFT computations where  $N$  equals to 32, 64, ..., or 2048, the total number of clock cycles needed to shift out  $N$  DFT outputs is  $(N/16)(N/32)$ . For DCT computations, one clock cycle is required to compute an  $N$ -point DCT where  $N$  is 8 or 16. For  $N$ -point DCT computations where  $N$  is 32, 64, ..., or 2048, the total number of clock cycles needed to shift out  $N$  DCT outputs is  $(N/16)(N/32)+(N/16)$ . The MRP circuit computes the  $N$ -point DFT/DCT with a latency of  $N/4$  clock cycles.

For digital video applications where DCT is used in data compression algorithms on 8X8 or 16X16 blocks of pixels, the 8-by-4 RSA can be configured to compute 8-point or 16-point 1D-DCTs. For 8-point DCT computations, the 8-by-4 RSA can perform simultaneously two 8-point DCTs on 2 sets of input data, each of which consists of 8 data samples. Groupings of two columns of the RSA, in this case, are configured to compute 8-point DCTs as shown in Fig. 2.

The PE consists of multiplier and adder circuits that could be configured to implement arithmetic functions that target multicarrier applications. The PE can be configured to support several modes of operation, including complex multiplication, real multiplication, addition or a combination thereof. The complex multiplication-accumulation configuration is required for DFT implementations while complex multiplication-accumulation and complex multiplication configurations are needed for DCTs. For DFT implementations, the PE can be configured to compute a set of partial results for

$Y_{DFT}(k)$ ,  $Y_{DFT}(N-k)$ ,  $Y_{DFT}(N/2+k)$ , and  $Y_{DFT}(N/2-k)$  based on the equations described in (3), (4), (5), and (6).

The SWs in the MRP design route signals from the input of the array to the PE cells. The SWs also route the output signals of the PE cells to other PE cells as well as to the output of the RSA.

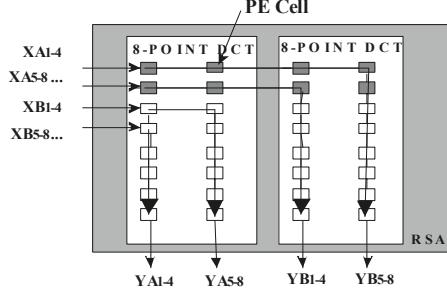


Fig. 2. Configuration of the 8-by-4 RSA for two 8-point DCT computations.

### B. Multiplierless Circuit Design

In this section, we consider the design of the PE, whose multiplier circuits are implemented on the basis of the CSE-BitSlice technique [8]. The PE consists of four real multipliers and twenty real adders that can be configured to perform a wide range of arithmetic computations involving the input signals and a set of coefficients. The CSE-BitSlice technique for multiplication of two variables is used in the design of each multiplier. The four multipliers  $S_1, S_2, S_3$ , and  $S_4$  in the PE cell perform multiplication of the four input data samples  $x_1, x_2, x_3, x_4$  and four coefficients  $C_1, C_2, C_3$ , and  $C_4$  as follows:

$$S_k = x_k * C_k \quad k = 1, \dots, 4$$

Using the 2-Term decomposition technique, where each coefficient component  $C_k$  consisting of  $B$  bits is decomposed into two data slices, each of which consists of  $B/2$  digits, the real multiplication of  $x_k$  and  $C_k$  can be expressed as:

$$S_k = x_k * C_k = x_k * \left( C_{k,2} * 2^{\frac{B}{2}} + C_{k,1} \right) = x_{k,s} * C_{k,2} + x_k * C_{k,1}$$

$$S_k = x_{k,s} * \left( C_{k,1} \bullet \overline{C_{k,2}} \right) + (x_{k,s} + x_k) * \left( C_{k,1} \bullet C_{k,2} \right) + x_k * \left( \overline{C_{k,1}} \bullet C_{k,2} \right) \quad (7)$$

$$x_{k,s} = x_k \ll 2^{\frac{B}{2}}$$

The symbol  $\ll$  represents the shift left operator where  $C_{k,1}$  and  $C_{k,2}$  are the first  $B/2$  and the last  $B/2$  digits of the coefficient component  $C_k$  respectively. The symbol  $\bullet$  represents the logical AND operator. By factoring out the common digits in  $C_{k,1}$  and  $C_{k,2}$  a total of  $B/2$  additions would be required to compute a real multiplication of an input  $x_k$  and the coefficient  $C_k$ . Thus the total number of additions required to compute all four real multiplications using 2-Term CSE-BitSlice technique is  $2B$ . Figure 3 depicts the design of a multiplier block in the PE cell using the 2-Term CSE-BitSlice technique.

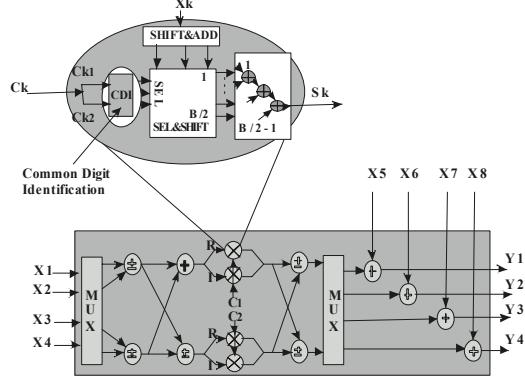


Fig. 3. Multiplier block diagram based on the 2-Term CSE-BitSlice approach.

### IV. MULTIPLIERLESS RECONFIGURABLE DFT/DCT PROCESSOR IMPLEMENTATION AND SIMULATION RESULTS

In this section, FPGA implementation and simulation results for the MRP circuit are presented. Two's complement number representation and fixed-point arithmetic has been used throughout. Hardware implementations have been carried out using Xilinx's 5VLX330FF1760-2 FPGA device. The PE circuit implementation is based on the architecture depicted in Fig. 3. Complex coefficients consist of 18 bit words with 9 bit real and 9 bit quadrature. Each input data bus of the PE cell is 24 bits wide and each cell output is represented by 34 bits, all in complex format. Simulation results for MRP circuit implementations based on the CSE-BitSlice technique are summarized in Table I. The clock rate performance of the MRP shows that the circuit can shift out an  $N$ -point DFT every 22.2 ns for  $N$  equal to 8 and 16. The same processing time can be achieved for 8 and 16-point DCT computations. For  $N$  equal to 32, 64, ..., 2048, a complete set of  $N$ -point DFTs can be shifted out after  $(N/16)(N/32)(1/45)$   $\mu$ s based on the MRP circuit. Thus, the MRP circuit performance satisfies the throughput requirements of several OFDM transmission schemes including DAB, ADSL, and the IEEE 802.11a standards. Table II shows the performance of the MRP circuit configured for various broadband standards in terms of DFT size and processing time. It is clear that the MRP circuit supports the DFT throughput requirements as it relates to the OFDM circuitry for the IEEE 802.11a, DAB, and ADSL standards. Furthermore, the MRP circuit also supports OFDM processing throughput requirements of DVB-T and VDSL for  $N$  up to 2K. The MRP has a flexible architecture, which could be used in OFDM transmission schemes where the number of subcarriers is not a power of two.

In multimedia systems where 2D DCTs are used to perform data compression on blocks of 8X8 pixels, the MRP can be configured to compute DCT on each row and column of the 8X8 array using a row-column separation strategy [10]. Since the MRP can shift out two complete sets of 8-point DCT outputs at every clock cycle, a total of 8 clock cycles is required to process a block of 8X8 input data. Table III shows the performance of the MRP circuit configured for 2D DCT

computations of data frames of different size for various image compression standards.

TABLE I  
IMPLEMENTATION AND SIMULATION RESULTS FOR THE MRP CIRCUIT DESIGN.

Logic Resources/Clock Rate	
FF	32673/207360 (15 %)
4-Input LUT	122809/207360 (59 %)
Clock Rate (MHz)	45

TABLE II  
MRP DFT CONFIGURATIONS AND THROUGHPUT FOR DIFFERENT BROADBAND STANDARDS.

DFT (N)	Standard	Transf. Time Req. (μs)	MRP Proc. Time (μs)
64	IEEE 802.11a	3.2	0.18
256	DAB	31	2.8
512	DAB, ADSL, VDSL	62, 231, 231	11.3
1024	DAB, VDSL	124, 231	45.4
2048	DAB, DVB-T, VDSL	248, 224, 231	181

TABLE III  
MRP DCT CONFIGURATIONS AND THROUGHPUT FOR DIFFERENT IMAGE COMPRESSION STANDARDS.

DCT size (NXM)	Standard	Proc. Rate Req. (Frames/s)	MRP Proc. Rate (Frames/s)
352X288	SIF	25	3554
525X720	CCIR-TV	25	953
1152X1296	HDTV	50	162

From the results in Table III, it can be seen that the MRP supports the frame rates required by the Source Input Format (SIF) and the International Consulting Committee on Radio and Television (CCIR-TV) standard of 25 frames per second. The processor throughput performance shows that it also supports the required frame rate of the High Definition TV (HDTV) standard at 50 frames per second. The MRP circuit implementation on the VIRTEX-5 FPGA provides favorable frame rate performance for the SIF, CCIR-TV and HDTV applications as compared to alternate realizations reported in the literature [11].

## V. CONCLUSION

A multiplierless reconfigurable DFT/DCT processor suitable for broadband and multimedia applications has been presented. Simulation results of the MRP circuit configured for DFT and DCT computations of various data sizes have shown that the MRP satisfies the processing requirements of most broadband and digital video standards. Since the RSA is a modular

architecture, the 8-by-4 RSA building block could be expanded to increase the processing power of the MRP circuit. The addition of extra rows or columns of PE and SW cells to the 8-by-4 RSA array would allow the MRP to support the DFT transform rates required by the DVB and VDSL standards for N equal to 4K and 8K. The MRP can also be configured to compute N-point DCTs where N is not a power of two. This reconfigurability characteristic enables the MRP to support object-based video coding applications where the block of data to be processed is of arbitrary geometry. The MRP processor has been implemented without the use of conventional multipliers and as a result, low hardware usage has been achieved. The MRP supports real time reconfigurations of DFT, DCT as well as complex multiplication and/or addition functions and its flexibility makes it suitable for other applications such as software defined radio.

## REFERENCES

- [1] A. Kaup, "Object-Based Texture Coding of Moving Video in MPEG-4," IEEE Trans. on Circuits and Systems for Video Technology, Vol. 9, No. 1, pp. 5-15, February 1999.
- [2] P. Tseng, C. Haung, and L. Chen, "Reconfigurable Discrete Cosine Transform Processor for Object-Based Video Signal Processing," Proc. of the 2004 Int'l Symposium on Circuits and Systems, ISCAS'04, Vol. 2, pp. 353-356, May 2004.
- [3] J. Gause, P. Cheung, and W. Luk, "Reconfigurable Computing for Shape-Adaptive Video Processing," IEE Proc. of Computers and Digital Techniques, Vol. 151, No. 5, pp. 313 – 320, September 2004.
- [4] Y. Zhao, A.T. Erdogan, and T. Arslan, "A low-power and domain-specific reconfigurable FFT fabric for system-on-chip applications," Proc. of the 19th IEEE International Parallel and Distributed Processing Symposium, IDPDS'05, April 2005.
- [5] G. Zhong, F. Xu, and A. Willson, "An energy-efficient reconfigurable FFT/IFFT processor based on a multi-processor ring," Proc. of the European Signal Processing Conference, EUSIPCO'04, pp. 2023-2026, September 2004.
- [6] E. Tell, O. Seger, and D. Liu, "A converged hardware solution for FFT, DCT and Walsh transform," Proc. of Seventh Int'l Symposium on Signal Processing and Its Applications, ISSPA'03, Vol. 1, pp. 609 – 612, July 2003.
- [7] R. Pandey and M. Bushnell, "Architecture for Variable-Length Combined FFT, DCT, and MWT Transform Hardware for a Multi-Mode Wireless System," Proc. of the 20th Int'l Conf. on VLSI Design, VLSID'07, pp. 121-126, January 2007.
- [8] H. Ho, V. Szwarc, and T. Kwasniewski, "Hardware Optimization of a Configurable Polyphase-FFT Design Using Common Sub-Expression Elimination," Proc. of the IEEE Int'l MWSCAS/NEWCAS '07 Conf., August 2007.
- [9] H. Ho, V. Szwarc, and T. Kwasniewski, "A Reconfigurable Systolic Array SoC Design for Multicarrier Wireless Applications," Proc. of the IEEE Int'l Midwest Symposium on Circuits and Systems, MWSCAS'08, August 2008.
- [10] J. Makhoul, "A Fast Cosine Transform in One and Two Dimensions," IEEE Trans. on Acoustics, Speech, and Signal Processing, Vol. 28, No. 1, pp. 27-34, February 1980.
- [11] K. Bukhari, G. Kuzmanov, and S. Vassiliadis, "DCT and IDCT Implementations on Different FPGA Technologies," Proc. of the Annual Workshop on Sig. Proc., Integrated Syst. and Circuits ProRISC'02, pp. 232-235, November 2002.