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BOOTH RECODED WALLACE TREE MULTIPLIER USING NAND BASED DIGITALLY CONTROLLED DELAY LINES

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ABSTRACT

Digital controlled delay line (DCDL) is a digital circuit used to provide the desired delay for a circuit whose delay line is controlled by a digital control word. There are wide varieties of approaches available for constructing the DCDL. The previous approach deals about designing a DCDL with and without glitches. More over Glitches are the most considerable factor that limits the use of DCDL in many applications. The Glitches in a circuit can be analyzed by increasing delay control code in a circuit. By reducing the number of glitches a delay line also further reduced. . In this paper NAND based DCDL improved using Wallace tree multiplier, which used to give an accurate value, as well increase speed of operation. It aims at additional reduction of latency and area of the Wallace tree multiplier using the delay control units based on the DCDL unit. The simulation have been carried out using modelsim and xilinx tools.

Keywords: booth multiplier, arithmetic unit, encoder, compressor, DCDL, wallace tree, spread spectrum.

1. INTRODUCTION

Analog circuits are difficult to design since designing these circuits fail to do the job more efficiently and it work an continuous level signals. But a digital circuits are easy to design, since automation can applied at various level of circuit. Hence time domain resolution of analog signals become more important than voltage resolution of analog signals [1]. Digital circuits operate on only two levels i.e,0's&1's.Digital circuits have an high degree of flexibility. DCDL used in many applications like spread spectrum clock generator (SSCG) and ultra wide band (UWB)[17],[18]..DCDL [3] [6], [9],[17] mainly used in the purpose of clock signals. By that it will produce an output with respect to an input. Initially DCDL design with a MUX which may provide a minimum delay (t_{min}) which is an critical design parameter of many applications. A $t_{min\ \ occurs}$ due to an increase in number of cells.MUX with DCDL have an tradeoff between delay range and minimum delay. Increase in number of cells may chance of more num of delays in the circuit. It might reduced by using tree-based multiplexer topology, however it produce an irregular structure to the device. Due to an irregularity it provides a more complicates to the circuit. Further it moves on into some other concept to overcome above drawbacks.

Hence DCDL was design with an regular cascade of equal delay elements(DE)[12]-[15].In regular cascade of delay elements the above multiplexer has spreader among the cells, by that it reduce the number of delay(t_{min}) as much better than above MUX based DCDL, and become dependent of number of cells. A DCDL with regular cascade of delay elements design with an NAND gates. Which may provide an high regularity to the circuit. Additionally it provides an very good linearity and resolution. Obtaining resolution as $2.t_{NAND}$ (delay of NAND gate)

DCDL is constructed with a three state inverters (TINV)[18].The above concept reveals that a DCDL with an regular cascade of delay elements design with an NAND gates. Hence here instead of NAND gates it designs with a TINV. Each element is constructed by an three state inverters. Here we obtain a resolution as $2.t_{TINV}$ .Resolution of TINV is higher than resolution of NAND gates. Because pull up network of TINV requires two series devices and NAND requires single device only.

The DCDL with an cascade of equal delay elements [12]-[15], allows an simple layout organization. Here it has constructed by an inverter and inverting multiplexer. It may require some drawbacks. Among that, t_{min}(minimum delay)which is an critical parameter of many application obtains an mismatch between odd and even control codes. Due to that mismatch there may increase in integral non linearity (INL).Its an one of drawback. Another drawback is, multiplexer increases in number of cells, due to that delay might increase, it provides higher resolution than both a NAND and TINV –based DCDL.

Occurrence of glitching in a circuit may limit its application and its an major drawback of a process .And glitching is common problem in a circuit. DCDL is most probably applied for an process of an clock signals. Due to that we go for glitch free circuit. The circuit without an glitch has used for an wide range of applications. The glitch-free circuit obtained by designing a NAND based DCDL with an delay control code switch. Glitching may also avoid by using an thermometer code on control bits i.e. used to avoid numbers of delays in a DCDL circuit.

DCDL has an application like all digital delay locked loop(ADDLL) [9]-[16], all digital phase locked loop(ADPLL)[2]-[8].In a ADDLL glitches may avoid by using phase detector and harmonic locking circuitry during locking phase.

This paper contributes about two processes. Initially it describes about a proposed NAND based DCDL without a glitch. second it deals about encoding a NAND based DCDL into an Wallace tree multiplier ,as a future work .And proves much better result ,by encoding

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that Wallace into NAND based DCDL. Achieves a good resolution.

2. PREVIOUSLY PROPOSED NAND BASED DCDL WITH AND WITHOUT GLITCHES

The Figure-1 shows the NAND based DCDL without glitches. The circuit which contains unit delay in a block of delay control unit is used to hold the delay while transferring the messages from sender to receiver, by that number of delays reduced in a circuit due to that circuit obtained with glitch free circuit and a spread spectrum to detect a jitter problem in order to avoid signal deviation. Hence the NAND based DCDL also contain a block of spread spectrum clock generator along with phase locked loop. Spread spectrum used for the purpose of secure transformation by converting the messages from one format into another format, like encoding and decoding method. Phase locked loop frame buffer control the system that generates a output signal whose output is related to input signal.

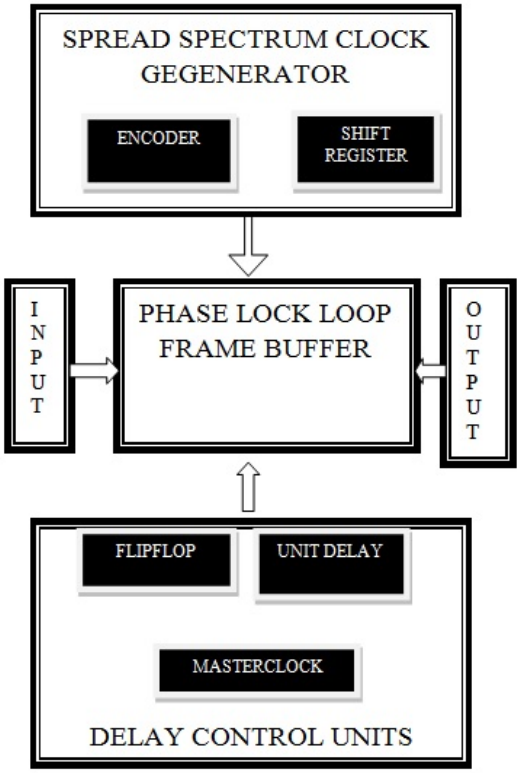


Figure-1. NAND based DCDL.

Hence here driving circuits are also introduce in order to avoid delays. The driving circuit may act with a D-flip flop. The glitch free NAND operation may detailed with an inverting and non-inverting topology of a NAND gates. The topology may act with a binary values such that 0's and 1's. Stuck at 1(s_a_1) for non-inverting topology and Stuck at 0 (s_a_0) for inverting topology.

Here the two control bits S_i and T_i act as a thermometric code and one cold fact. The both control bits encoded by this view. In occurrence of a glitch circuit there is a possible of only two states namely "pass state" and "post state" for a delay elements .But in turn of Glitch-free circuit it acts in possible of three states i.e. "pass state" Turn state" and finally a "Post-turn state".

3. BLOCK DIGRAM OF NAND BASED DCDL WITHOUT GLITCHES

The NAND based DCDL determines the parameter as Area, Power, Delay, through control units and spread. The control units have a flip-flop, Unit delay and Master clock. Master clock is used here in order to control analog signals and digital signals; it's a precision clock that provides timing signals synchronize slave clocks as a part of clock networks. Unit delay block hold and delays its input by the sample period which specified by the certain user. Signal act as a scalar or vector, accepts one input and generate one output. Flip-flop is a storage device has two stable states. It has one or two outputs as well inputs, it's a bistable multivibrator.

From Figure-1- let us Consider an two users, which transfer an input clock signals in certain frequency, through phase locked loop frame buffer which may transfer an input with respect to an output.

Hence while transferring an input clock signals. In order to avoid an no. of delay elements here we use a control units in factor of unit delay, flip-flop and master clock. Then a spread spectrum clock generator used here to avoid a jitter problem at an output i.e. signal deviation during the process.

4. SIMULATION RESULT WITH AND WITHOUT GLITCHES

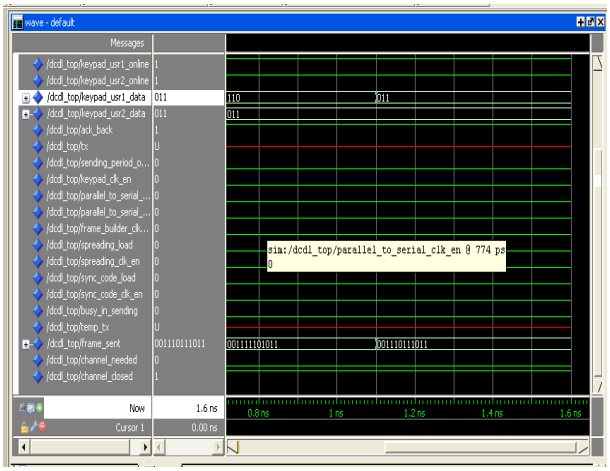
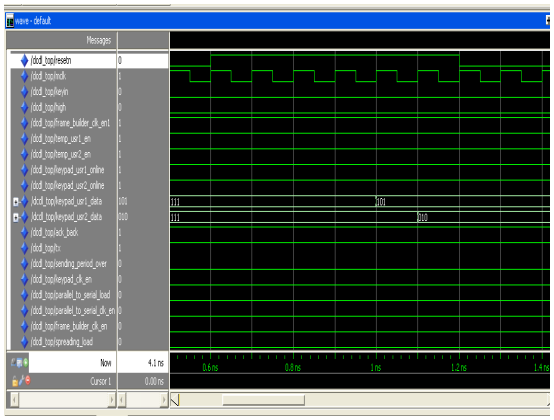


Figure-2. Circuit with glitch.

INFERENCE

The red color line in a above simulation indicates that a line was not enabled,causes a glitches in a circiut



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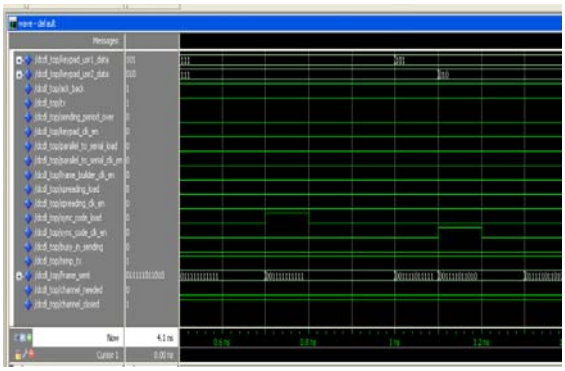

Figure-3. Glitch free circuit.

5. PROPOSED NAND BASED DCDL WITHOUT GLITCHES USING WALLACE TREE MULTIPLIER

The proposed work determines with a multipliers. Which is improved version of NAND based DCDL without glitches, and provide more efficient to the circuit than previous work.

Multipliers

It has two basic operations such as, Partial products and their accumulation, by this operation we can speed up the process.

By reducing no. of partial product it also reduces complexity and the time needed to accumulate the partial product, and both can applied simultaneously.

Types of multipliers

There are various types of multipliers, such as

1) Array multiplier
2) Wallace tree multiplier
3) Booth multiplier
4) Dadda multiplier

The above three multiplier is a high speed multiplier. Among that multiplier Wallace tree multiplier is going to encode with an NAND based DCDL to provide better result.

Drawbacks

1. **Array multiplier**
   - Worst case delay of multiplier proportional to the width of multiplier
   - Speed will be low for very wide multiplier

2. **Dadda multiplier**
   - Dadda multiplier is similar to Wallace tree multipler, which may also have same three steps to evaluate the process.
   - However, Wallace multipliers that reduce as much as possible an each layer, Dadda multiplier do as few reduction as possible.
   -

Why multiplier encoded with a NAND based DCDL

Multiplier is a fast arithmetic circuit and it plays important role in digital circuits and various applications. Multipliers offer following design parameters such as area, low power consumption, high speed regularity of layout. And hence multiplier was encodes with an NAND based DCDL. Which provide better result than NAND based DCDL.

Advantage of wallace tree and booth Multiplier

- Small in delay
- No. of logic levels required to perform summation can be reduced with Wallace tree

. In **Booth multiplier,**

Reduce No. of partial products, thus make it extensively used in multiplier with long operands (716 bits) .And this is a main reason why we using a Wallace tree in NAND based DCDL

By including a partial product it achieves highest reduction in stages and high performance. Booth multiplication is a multiplication that multiples two signed number in 2's complement. Booth uses a desk calculator that where faster at shifting than adding &created the algorithm increases their speed Booth recoding improves the cost and cycle time of standard multiplier by certain constant factors.

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6. A PROPOSED WALLACE TREE MULTIPLIER

A high speed and area efficient booth recoded wallace tree multiplier for fast arithmetic circuits using NAND based DCDL is proposed in this paper. It is an improved version of tree based Wallace tree multiplier architecture. This paper aims at additional reduction of latency and area of the Wallace tree multiplier using the delay control units based on the DCDL unit. This is accomplished by the use of Booth algorithm and compressor adders. The Wallace tree multiplier is improvised with NAND based DCDL and hence provide efficient result than previous.

From Figure-4 Wallace tree is an efficient hardware implementation of a digital circuits that multiple two integer. The benefit of Wallace tree is that there are only O(logn) reduction layers and each layer has O(1) propagation delay.

As Wallace tree includes partial product, booth encoding, and compressor technique along with multiplier and multiplicand value.

Wallace tree multiplier works in a three step process operation:-

a) Multiply each bit of one of the arguments, by that each one yield one another.

b) By introducing a partial product number of stages reduced by layers of full adder and half adders.

c) Then finalizing the result as, group the wires in two numbers and add then with a conventional adder.

Tabulation for previously proposed NAND based DCDL power and delay

Delay

Minimum period	6.665 ns
Minimum I/P arrival time before clock	4.606ns
Maximum O/P arrival time after clock	6.21 ns
Maximum frequency	150.029 MHZ

Inference: The delay may reduced by adding an delay control unit to NAND based circuit such as Flip-Flop, Master Clock, Unit Delay.

Power

Name	Power
clock	0.058 W
Logic	0.002 W
Signals	0.006 W
I/O's	0.544 W
Total Quescent Power	0.043 W
Total Dynamic Power	0.728 W
Total power	0.772 W

Inference

A proper Power has utilized by a both output and input using an phase locked loop frame buffer, In case of PLL the input applied may obtained with respect to output.

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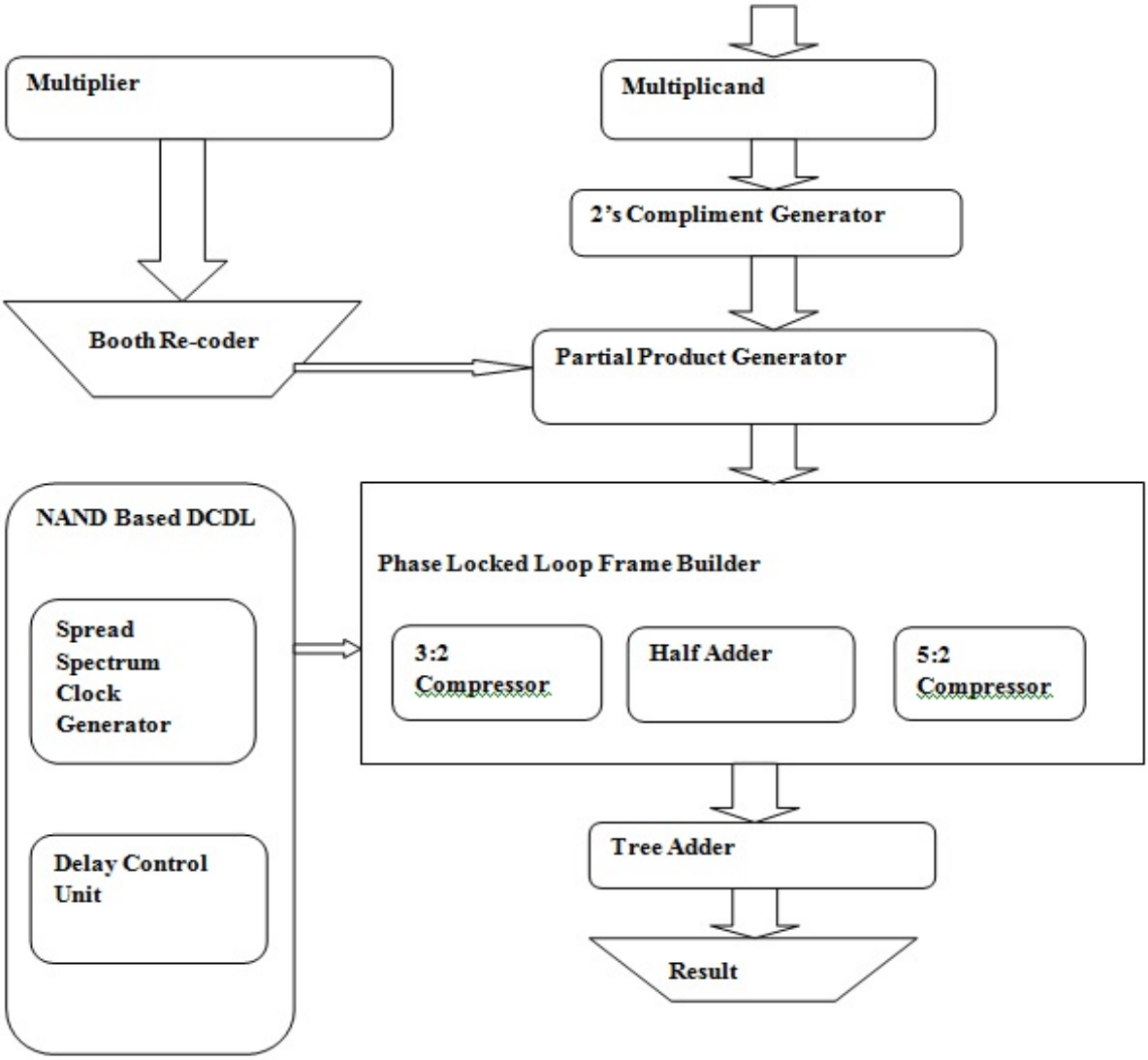

Figure-4. Wallace tree multiplier with NAND based DCDL.

7. RESULTS AND DISCUSSIONS

Tabulation and simulation results of power and delay using wallactree-nand based DCDL

Delay

Minimum period	6.665 ns
Minimum I/P arrival time before clock	4.606ns
Maximum O/P arrival time after clock	4.26 ns
Maximum frequency	150.029 MHZ

Inference

The delay has further reduced by improvising NAND based DCDL with Wallace tree multiplier.

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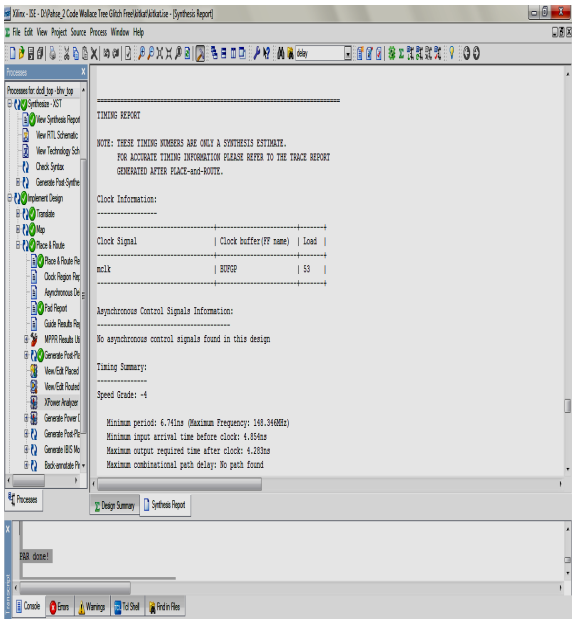
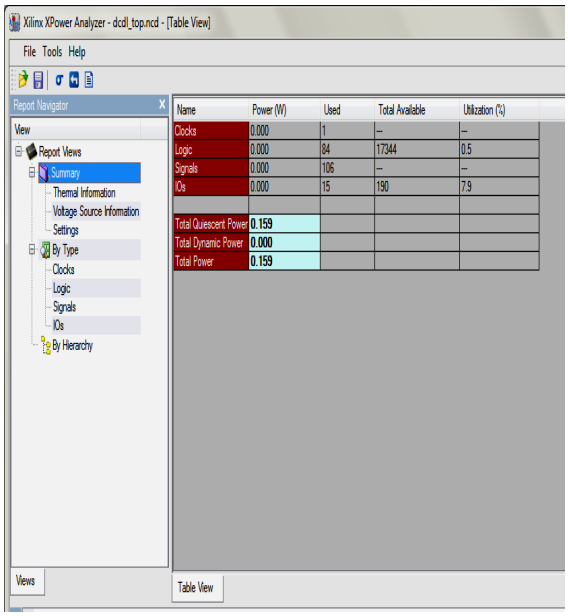
Simulation result OD delay



Simulation result of power



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8. CONCLUSIONS

In this paper NAND based DCDL is enclosed with Wallace tree multiplier and developed with a control delay units as well spread spectrum clock generator, in order to reduce no. of delays in a digital circuit. And a area obtained and power utilization for the proposed circuit has declared. The circuit of NAND based DCDL with Wallace tree shows the difference of both glitch and glitch free circuit and reduce in dealy and power. The simulation results confirm the correctness of developed model and show that proposed solution improve the resolution with respect to previous approaches.

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