

OPTIMIZING CIRCUIT PARTITIONING BY IMPLEMENTING DATA MINING AND VHDL TOOLS PERTINENT TO VLSI DESIGN

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Abstract

The relevance of VLSI in performance computing, telecommunications, and consumer electronics has been expanding progressively, and at a very hasty pace. In order to build complex digital logic circuits it is often essential to sub-divide multi-million transistors design into manageable pieces. Circuit partitioning is a general approach used to solve problems that are too large and complex to be handled at once. In partitioning, the problem is divided into small and manageable parts recursively, until the required complexity level is reached. In the area of VLSI, circuit complexity is rapidly multiplying, together with the reducing chip sizes; the integrated chips being produced today are highly sophisticated. There are many diverse problems that occur during the development phase of an IC that can be solved by using circuit partitioning which aims at obtaining the sub circuits with minimum interconnections between them. This paper aims at circuit partitioning using clustering technique by applying two clustering algorithms K-Means and PAM (Partitioning around medoids). These two algorithms were tested on a BCD to Seven Segment Code Converter circuit consisting of eight nodes and also were tested on a circuit consisting of 15 nodes. The two algorithms were implemented on VHDL. The tested results show that PAM yield better subcircuits than K-Means.

Key words: Circuit Partitioning, VLSI, K-Means, PAM

I. INTRODUCTION

Advances in semiconductor technology and in the integration level of integrated circuits have enhanced many features, increased the performance improved reliability of electronic equipment, and at the same time reduced the cost, power consumption and system size. As size and complexity of digital system has increased, more computer aided design tools are introduced into hardware design processes. VLSI design automation has attracted a great deal of interest. A recent survey [1] lists almost 200 papers on the subject. Circuit partitioning in VLSI design is key role in physical design. The objective of circuit partitioning is to divide the circuit into number of subcircuits with minimum interconnections between them.

In past two decade, partitioning problems has been studied by researchers and various heuristic algorithms have been developed [2]-[4]. The circuit partitioning is also achieved by using some of the clustering algorithm [6]. In this paper to achieve circuit partitioning, with minimum interconnections is obtained by applications of two clustering algorithms PAM and K-means. These two clustering algorithms are applied on the circuit BCD to Seven segment conversion circuit consisting of eight nodes. Results show that PAM gives better clusters with minimum interconnections. Both the clustering algorithms are run on VHDL code and testing results are obtained.

II. IMPLEMENTATION

The implementation consists of three stages consisting of data extraction, partitioning and result. In data extraction, a VLSI circuit of BCD to 8 segment converter is considered. The circuit considered is shown below

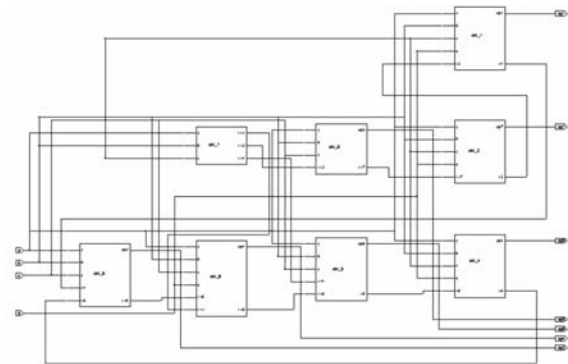


Fig. 1 BCD to Seven segment display Circuit with 8 nodes

In the above circuit each rectangular box is considered as a node. The circuit consists of 8 nodes with interconnection between them. The sub circuits within one of the node are shown in Fig 2. The input to this circuit is a BCD(Binary coded Decimal) code and output is seven segment display.

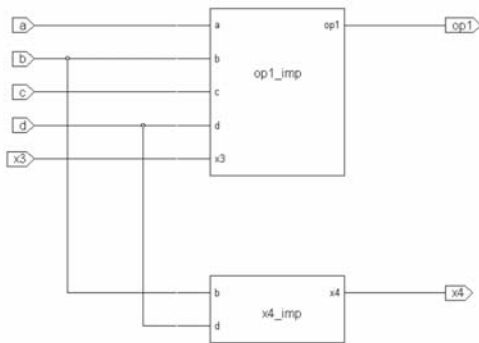


Fig. 2 Circuit Depicting Within One of the Node

Fig. 3 shows the internal view of op1_mp which consists some of the basic gates like AND OR and inverter gates. Similarly each node consists of all the basic gates

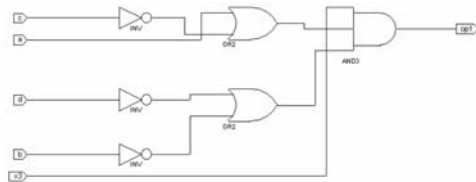


Fig. 3 Circuit within OP1_mp Consisting of Basic Gates

The out put is the seven segment display is depicted in Fig 4.The input to the circuit and the corresponding output obtained is shown in table 1.

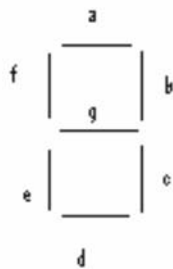


Fig. 4 Seven Segment Display

From the table 1 it is clear that whenever the input of '0', in the seven segment display except 'g' all other values are '1'. Since the input is BCD the input values are taken from '0' to '9' only.

Table 1: Input and Output for the BCD to Seven segment display Circuit

Input 1	Input 2	Input 3	Input 4	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	0	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	0	1	1

III. SUMMARY OF CLUSTGERING ALGORITHM

Clustering is referred as unsupervised learning segmentation. The clusters are formed by finding the similarities between data according to characteristics found in the data. It can be thought of as partitioning or segmenting the data into groups that might or might not be disjointed. In this paper K-Means and PAM (Partitioning around mediods) are used get the best clusters.

A. K-Means Algorithm

K-Means is an iterative clustering algorithm [9] in which items are moved among sets of clusters until the desired set is reached. As such, it may be viewed as a type of squared error algorithm, although convergence criteria need not be defined based on the squared error. A high degree of similarity among elements in clusters is obtained, which a degree of dissimilarity among elements in different clusters is achieved simultaneously. The cluster mean if $K_i = \{t_{i1}, t_{i2}, \dots, t_{im}\}$ is defined as

$$mi = \frac{1}{m} \sum_{j=1}^m tij \tag{1}$$

B.PAMAlgorithm

This algorithm [9] represents a cluster by a mediod. Using this algorithm handles outliers well. Quality of clusters is measured by the sum of all distances from a non-mediod object to the mediod for the cluster it is in. We use C_{ph} to be the cost change for an item t_j associated with swapping mediod t_i with non-mediod t_h . The total complexity per iteration is $n(n-k)2$.The cost is the change to the sum of all distances from items to their cluster mediods.The total impact to quality by a mediod change TC_{ph} is given by

$$TC_{ih} = \sum_{j=1}^n C_{jih} \tag{2}$$

The above clustering was also applied for the 15 node circuit. The circuit consisting of 15 nodes considered is shown in Fig 5. In this also, PAM clustering algorithm gave the circuit with minimum interconnection compared to K-means.

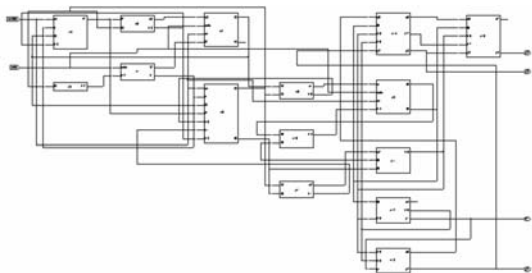


Fig. 5 Circuit Considered For Testing With 15 Nodes

IV. RESULTS AND CONCLUSION

In data extraction, the circuit which is a BCD to seven segment code converter consisting of 8 nodes is considered. The circuit is represented by an adjacency matrix where the values represent the distances between the nodes. The adjacency matrix is fed into algorithm which gives the sub-circuits with lowest amount of interconnections between them. The partition is tested on the circuit. The table below gives the performance of PAM and K-means algorithm. The algorithm is implemented on Xilinx 6.1 using project Navigator using VHDL.

V. CONCLUSION

In this paper the Circuit Partitioning which plays a critical role in physical design of an integrated circuit with minimum interconnections is obtained by implemented using two clustering algorithm PAM and K-Means. Experimental results shows that K-Means gives four clusters where are PAM gives two clusters for the same input. The circuit also shows the minimum interconnections between them.

Table 2. Performance of PAM and K-Means

Input	No. of Clusters	
	PAM	K-Means
BCD to seven segment	2	4

The results shown in Fig 6, shows that the partitioning achieved by K-Means algorithm results in 10 interconnections between the 4 sub-circuits and 9 interconnections between the 2 sub-circuits on partitioning using PAM algorithm

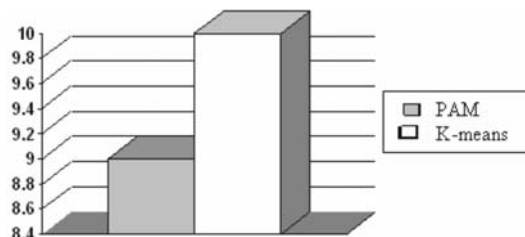


Fig 6. Graph Depicting the Interconnections Obtained Two Algorithm

The number of interconnections between sub-circuits in the circuit with 15 nodes is 12 Refer Fig. 8,9 & 10 in the case of K-Means and only 7 in the case of PAM. Similarly, the number of interconnections in the circuit with 8 nodes is 10 in the case of K-Means and 9 in the case of PAM is shown in Fig 7.

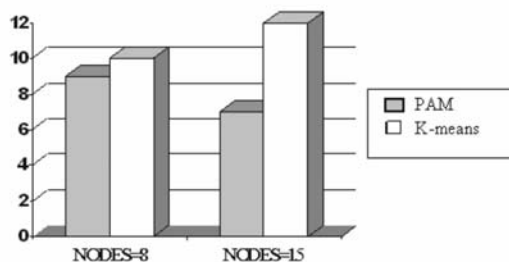


Fig 7. Graph Depicting the Interconnections Between Subcircuit For 8 Nodes and 15 Nodes

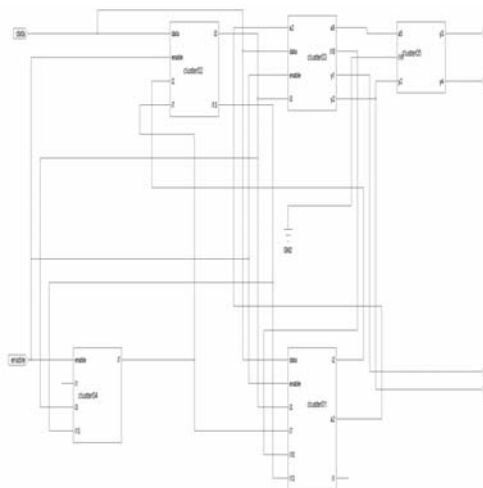


Fig 8. Circuit Partitioning For 15 Nodes After Application of K-means Algorithm

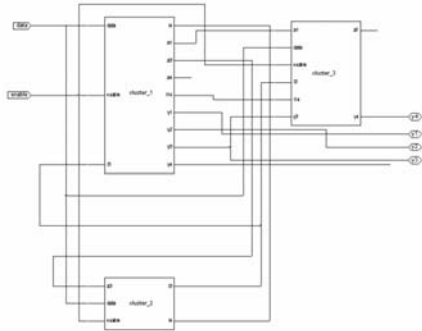


Fig 9. Circuit Partitioning For 15 Nodes After Application of Pam Algorithm

Screen Shots depicting the Circuit Partitioning for the Circuit BCD to Seven segments Display

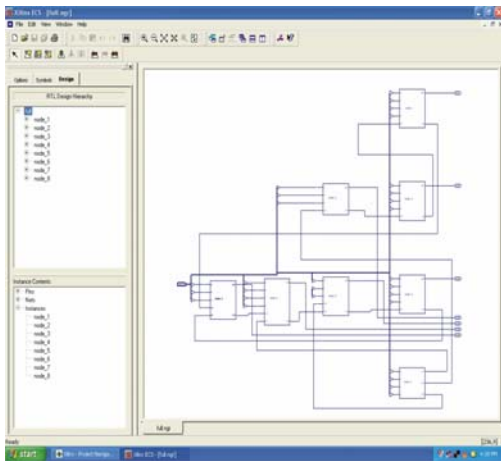


Fig 10. a. Screen Shot Showing the BCD to Seven Segment Display

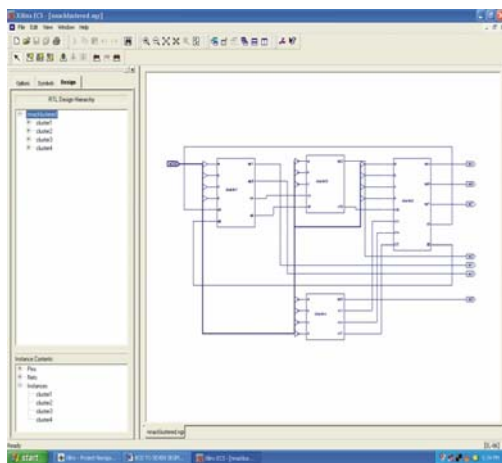


Fig 10. b. Screen Shot Depicting the Circuit After Application of K-means Algorithm Consisting of 4 Clusters

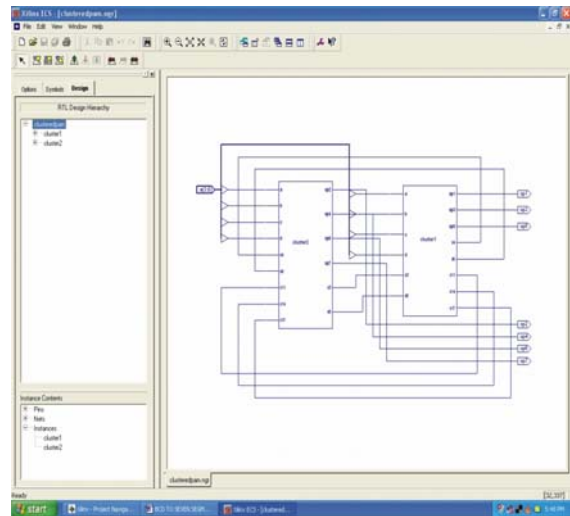


Fig 10. c. Screen Shot Depicting the Circuit After Application of Pam Algorithm Consisting of 2 Clusters

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