

INP MMIC AMPLIFIERS FOR CRYOGENIC RADIOASTRONOMICAL APPLICATIONS

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Abstract

Radioastronomical observation development, pushes technology research to develop equipment working up to 100-150 GHz. This trend make heavier the Low noise Amplifiers (LNA) noise contribution. A significantly improvement comes from the Indium Phosphide (InP) Technology, that gives the best noise performances in this range. Moreover radioastronomy moves also towards array receivers configuration, this implies high integration and repeatability. In the frame of the FARADAY PROJECT we were involved in designing several kind of MMIC amplifiers in the 18 to 26 GHz range in order to approach the InP technology and the MMIC design methodology.

Keywords: Low Noise Amplifiers, InP, MMIC, Cryogenic Applications, Radioastronomical Applications.

1. INTRODUCTION

In order to extend the observation capabilities, the radioastronomy research pushes towards higher and higher frequencies. Radioastronomical receivers must have excellent sensitivity and gain fluctuation stability.

The most used semiconductor were, and in many cases actually are, based on Gallium Arsenide (GaAs) technology. For frequency higher than 30 GHz this technology, for extreme low noise applications, begin to show its final limit. Actually InP technology has the best noise performances at higher frequencies [3].

Moreover, array receivers require a great amount of devices that must have very comparable performances. For these reasons MMIC design approach allows higher integration and repeatability level compared with MIC devices, designed using discrete component [4,5].

FARADAY PROJECT [8], supported by European Community, has as a main goal, to promote research and development of receivers based on array concept. In this context is inserted the work described in the following. We will present some amplifiers designed using InP MMIC technology, their specifications and design choices in order to realize this devices.

2. AMPLIFIERS SPECIFICATIONS

Amplifiers described have been designed in order to satisfy the system requirement for a cryogenic multifeed array receiver working in the range 18 to 26 GHz frequency range. The receiver channel specification requests 2 cryogenic amplifier the first one optimized for noise performance, the second one for return loss and gain, with about 40 dB of total gain. For this reason two classes of amplifiers have been designed. In Table I and II specifications are reported.

Gain	26±1.5 dB
Input Return Loss	< -15 dB
Noise Temp.	Best effort
Working Temp.	20 °K

Table I - LNA Specifications

Gain	15±1.5 dB
I/O Return Loss	Primary constraint
Noise Temp.	Moderately Low
Working Temp.	20 °K

Table II - BOA Specifications

3. AMPLIFIER FABRICATION

Thanks to the collaboration with CSIRO-ATNF, the European Partners of FARADAY consortium have had the possibility to approach the TRW 0.1 InP process. This technology is the result of an ambitious project named CHOP, led by JPL and TRW, having aim to obtain optimized devices for cryogenic environment [1,2]. For our devices which aim is working at 20°K this is a fundamental characteristic.

Actually, TRW library model are supported only for EESOF™ LIBRA® Series IV EDA Software. They support only 290°K active device models, and electromagnetic simulation, models and S-parameters for passive devices in the band 1to 50 GHz. About HEMT devices only 60%Idss is noise modeled. A more exhaustive beta version of semidistributed device models is available, but macro layout supported by CSIRO aren't available for this MMIC.

In this context we assumed to design “hot” devices, where each stage has independent bias pad, useful as tuning element.

4. AMPLIFIER DESIGN DESCRIPTION

The active device used are 4-fingers InP HEMT, 0.1µm gate length. Gate width is 120µm (4x30). Each gate is separately biased to tune the best performances at cryogenic temperature. The chip size dimension are 3.2 x 2.25 mm.

4.1. LNA

A 3-stage cascaded low noise amplifier layout is shown in Figure 1:

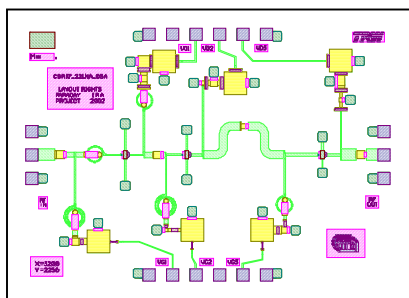


Figure 1

All matching circuits, except the first one, have been designed using distribute element like microstrip line. A one turn spiral inductor has been used in the first matching circuit as tradeoff between dimension constraints and the optimum noise matching point. This amplifier has been designed as a front end element, the first active device encountered by the

received signal. Moreover an off-chip matching network has been designed to prevent possible low frequency oscillation that could be primed through unwanted positive feedback path along the bias line.

4.2. BACK OFF AMPLIFIER

The layout of 2-stage cascade back off amplifier is shown in Figure 2:

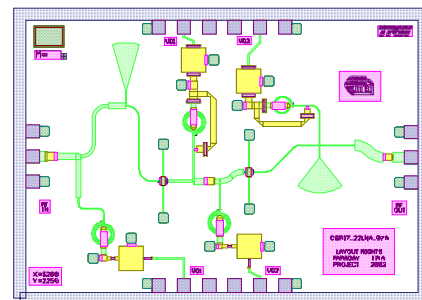


Figure 2

Matching circuit has been designed to achieve high return loss performances over the entire 18 to 26 GHz bandwidth.

Stability and RF isolation bias paths are also carefully investigated. Stability approach is conservative: every single stage has been designed to be unconditionally stable, following the indications given by K and B1 parameters. The S-probe stability check method has been tested for future applications: this method let the designer to probe the stability in every internal section of the amplifier [5].

We have considered, where applicable, twice the substrate thickness as minimum distance between two microstrip element as general design rule in order to reduce coupling effect of microstrip elements. Every critical part of microstrip circuit has also been electromagnetically simulated with EMSight®, the Microwave Office® EM-simulator, powered by AWR™, and the results have been compared with circuital simulation: only minor effect has been noted.

5. RESULTS OF THE SIMULATED AMPLIFIER

Expected results are reported in the following tables and graphics:

LNA05		S Parameters [dB]			Te @ 290 [K°]
		S11	S21	S22	
Frequency [GHz]	18	-9.5	25.6	-15.4	97
	22	-31.7	25.6	-19.4	89
	26	-15.2	25.3	-9.5	94

Table III

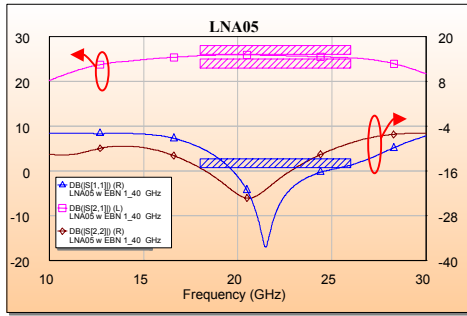


Figure 3

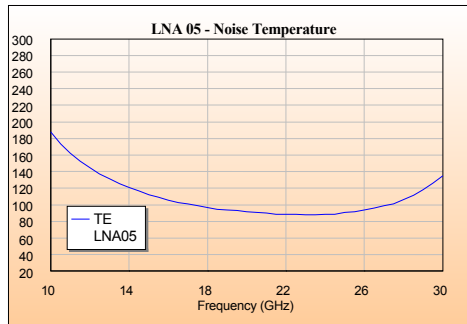


Figure 4

BOA07		S Parameters [dB]		
		S11	S21	S22
Frequency [GHz]	18	16,6	15	-10,7
	22	-25,1	16,2	-22,9
	26	-20,4	14,7	-9,5

Table IV

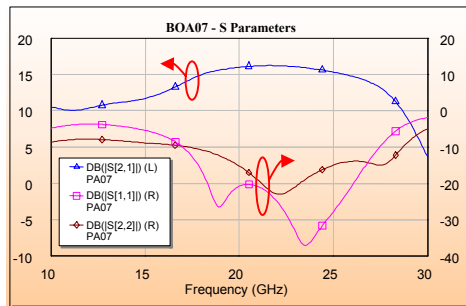


Figure 5

6. AMPLIFIERS PACKAGING

This is a critical point that could result in a irreversibly chip damaging if not carefully considered. moreover, operative condition are different if compared with on wafer testing conditions and a on carrier measurement will be necessary to discover possibly instability source coming from the carrier design.

Designed devices will operate in a 20°K cryogenic environment: cooling down the device also result in a undesirable mechanical deformation, depending on material physical propriety [6]. Semiconductors inside the carrier are usually attached by a conductive epoxy or welded. The different deformation between carrier and semiconductor may cause destructive mechanical stress. With InP semiconductor using common brass carrier results in a chip destruction during cooling down process. It has been investigated which kind of alloy could be the best trade off for us and several materials has been compared. Selected material must offer high thermal and electrical conductivity, because carrier is a ground reference and also an heat dissipating element. It's thermal Expansion Coefficient must be equal or a little bit higher than InP, because semiconductor chip offer better compression than stretching performance. A lot of time has been spent to find alloy that met our specifications:

W₉₀ / Cu₁₀ is produced using an High temperature sintering and infiltrate process. Ni/Au Metallization is possible by Electroplating or Physical Vapor Deposition (Ni metallization is necessary to avoid Gold contamination by Cu during heating process necessary for packaging). As reported in the table below this material has excellent physical and mechanical properties. Drawback of this material isn't machinable.

Si₃₀ / Al₇₀ has excellent thermal expansion coefficient and conductivity but this alloy has poor electrical conductivity. This is an specification important because carrier is our ground reference, and high losses in the carrier could produce mismatch from the expected results. The preferred candidate seems to be Silvar-K™ Alloy: It is easy machinable and it has been already cryogenically tested with InP devices from CSIRO-ATNF staff. Characteristic are specified in table V

	CTE [μm/m/°C]	Thermal Conductivity [W/m K @ 25°C]	γ [%IACS]
Cu	17.8	398	100
InP	4.5	68	
Brass	>12	>120	4
Kovar	5.3	17	2.2
Silvar-K™	7	110	18
W ₉₀ / Cu ₁₀	6.5	202	42
Si ₃₀ / Al ₇₀	6.5	180	1.7

Table V

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