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Multi-Standard Mobile Terminals

Ralf E. Schuh, Peter Eneroth and Peter Karlsson

Telia Research AB, Hjälmaregatan 3
201 20 Malmö, Sweden.
Tel: +46 40 105139, email: Ralf.x.Schuh@telia.se

ABSTRACT

This paper presents an investigation of a radio receiver architecture to enable multi-standard (GPRS, WCDMA, HiperLAN2) implementation in mobile terminals. The architecture uses partial radio band digitisation at an intermediate frequency. Following circuit progress and industry trends (e.g. Moore's law) we estimate components for the proposed architecture with acceptable power consumption to be available within the next 5 years.

I. INTRODUCTION

There is a need for multi-standard capable mobile terminals (MTs) as new radio systems arrive on the market, e.g. UMTS and HiperLAN2. Multimode and multi-band terminals, including e.g. GSM 900/1800/1900 with GPRS and Bluetooth, are already on the market with low power consumption. Extended multimode MTs will enable the user to access different existing and new radio systems with one single terminal. This way, the available radio spectrum can be used in a very efficient way.

Multi-standard MTs can be implemented by integrating different radio chipsets in a single radio module (hardware, ASIC solutions) or by using future software defined radio (SDR) technology. SDR will allow the user to reconfigure the terminal to the required radio mode by e.g. selecting the software code from a RAM or even downloading the relevant code from the network. For base stations (BSs), where power consumption and size is less restricted than in MTs, SDR components are already available on the market, e.g. for WCDMA.

The aim of this paper is to show that multi-standard GPRS/WCDMA/HiperLAN2 MTs built on SDR technology will be feasible within the next 5 years, with acceptable power consumption. Note that the IEEE802.11a standard has similar transceiver requirements as HiperLAN2.

II. SDR MOBILE TERMINAL FOR GPRS, WCDMA AND HIPERLAN2

Current receivers in MTs are normally based on the traditional superheterodyne (SH) scheme using narrowband reception although homodyne receivers exist. Ideal SDR, with broadband radio (to support multiple radio bands) and signal digitising directly at the antenna is far in the future, due to performance requirements, power consumption and practical implementation issues on e.g. the analogue-to-digital converter (ADC) and the digital signal processor (DSP) [1] - [3]. The focus of this paper is mainly on the receiver, as components requirements and commercial availability are more critical than for the transmitter.

Figure 1 shows the proposed receiver architecture for GPRS/WCDMA/HiperLAN2 radio reception. The radio frequency (RF) front-end consists of one analogue mixer stage, filters and low noise amplifiers (LNAs). The passband surface acoustic wave (SAW) filters are used in order to relax the digital filter / ADC requirements for blocking. The controllable amplifier/attenuator in front of the ADC will give some increase in the receiver dynamic range. The radio signals are digitised at a common intermediate frequency (IF) using a fast - high resolution ADC. The digital-downconverter (DDC) performs some of the more intensive digital processing tasks, like e.g. digital down-mixing, filtering and sample rate adaptation. In the transmit path digital-upconverters (DUC) are used for tasks like e.g. resampling, pulse shaping and digital up-mixing. Dedicated ASIC / FPGA chipset solutions exist from various manufacturers for DDC and DUC. These DDC and DUC can be programmed for usage in different radio standards, and have lower power consumption than DSPs doing the same tasks. The DSP has to perform tasks like equalising, channel and source coding/decoding, etc. The WCDMA/GPRS receiver may be implemented in a single path as analogue components, e.g. mixers, covering this frequency range are already on the market.

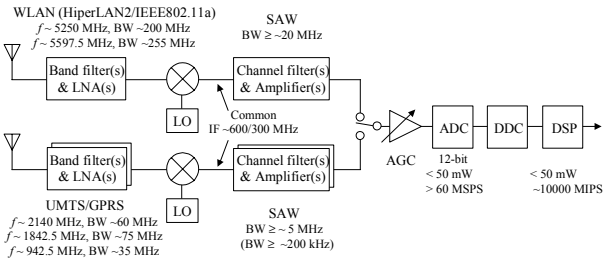

Figure 1: Block diagram of the multi-standard digital receiver

In reference [3], the principle of SDR with bandpass signal digitising at an IF is shown for a GSM BS application using existing components. Bandpass sampling can be used to down-convert a signal from an RF/IF to a bandpass signal at a lower IF. The author used an 11-bit ADC (AD6600 from Analog Devices) with a sample rate of 6.5 MSPS at an IF of 170 MHz. In order to fulfil the GSM requirements [4] (e.g. blocking) narrowband filtering (~180 kHz) at IF is used. The AD6600 also includes automatic gain ranging of 30 dB in order to increase the signal receive range. Since our interest is in MTs, power consumption is an important design issue. Therefore we first analyse the power consumption for such a SDR receiver implementation.

A. GPRS MT power consumption considerations

Figure 2 shows the estimated power consumption for a GPRS MT using components (chipsets from various manufacturers) currently available on the market for: (*i*) conventional superheterodyne baseband architecture and (*ii*) the IF sampling SDR implementation [3] (GPRS receiver path in Figure 1). The following components are considered in the power consumption comparison:

- RF/IF front-end and IQ demodulation, considering mixers, LNAs and IQ-demodulator for the SH receiver. For SDR, only one mixer stage is needed.
- Analogue-to-digital conversion for analogue baseband (SH) and at IF (SDR). For the SH receiver sigma-delta converters are often used in current mobiles (e.g. 10-bit, ~6 MSPS). For SDR we considered the AD6600 from Analog Devices, which has a multistage converter "flash" architecture [3]. The power consumption also considers DACs for analogue monitoring e.g. AGC, AFC and the corresponding amplifiers.
- Digital baseband (BB) signal processing using DSPs and ASICs/FPGAs for the source coding, channel coding, encryption, interleaving and the equaliser. For the SH and SDR GPRS receiver we considered the DSPs TMS320VC5402 (100 MIPS) from Texas Instruments designed for MT applications. The processor's performance should be sufficient for both receiver architectures in order to perform all the radio processing tasks (transmit and receive) for GPRS implementation [7]. For SDR we considered the power consumption of DDC, from various manufacturers (e.g. Grayship/Texas Instruments GC4016, 6.5 MSPS), which can handle the digital down-mixing, filtering and sample rate adaptation as required for the GPRS radio signal reception.

The following observations can be made from the figure:

- For the SH architecture the major power consumers are the RF / IF front-end and IQ-demodulation. For SDR the main power consumption is from the ADC.
- The SDR RF / IF front end uses less power than the SH receiver as only one mixer stage is used and the IQ-demodulation is done in the digital domain.
- The SDR has a ~4 times higher power consumption than the SH receiver.

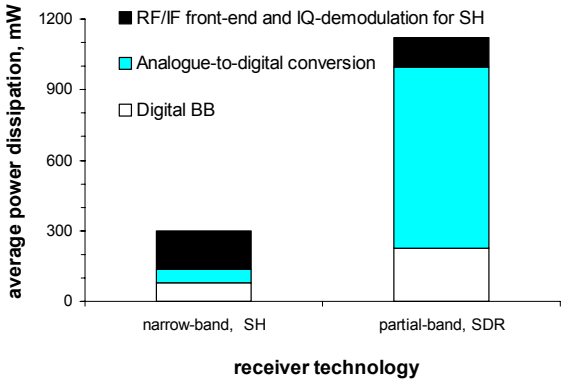

Figure 2: Power consumption estimation for GPRS MT using conventional SH and SDR receiver architecture

The power consumption estimates do not consider the display, application, and other higher layer related tasks. However, the power consumption for these tasks would be about the same for both receiver architectures in the above scenario. Considering the power consumption in transmit and receive paths together it was found that the power difference was a factor of ~3 (not considering the power amplifier). One of the reasons for this smaller relative power difference is that digital-to-analogue converters with similar performance (sampling speed, resolution) as ADCs consume less power.

Reduction in power consumption due to future enhanced process technologies (higher integration, lower voltage) applies to both the hardware (ASIC) and the software (SDR) approach. Therefore the factor of 4 as estimated above for the two receiver architectures we would not expect to change significantly in the future. However, as the software approach allows faster implementation of new algorithms e.g. allowing better power savings (sleep/power-down mode of the analogue and digital components), this ratio may be reduced.

B. Radio requirements

The SDR receiver for GPRS, WCDMA and HiperLAN2 has to confirm to the individual radio standard requirements such as: blocking, receiver sensitivity, etc [4] - [6]. The ADC availability with sufficient dynamic range, sampling speed and low power consumption, are among the most critical points for a SDR MT implementation. Table 1 shows the dynamic range (DR) requirements for the ADC considering blocking (BL)

and minimum SNR for GPRS/WCDMA/HiperLAN2 [4] - [6]. The blocking values given in Table 1 are only for MTs (less strict than for BSs in GPRS/WCDMA). The blocking of the interference from neighbourhood channels is one of the most stringent requirements on the ADC performance as we use partial band digitisation. The blocking values do not include out-of band interference, as we are only interested in in-band digitisation (e.g. WCDMA ≤ 60 MHz). The headroom (HR) considers ADC operation below full scale (e.g. 3 dB) and the maximum peak-to-average power ratios for the different radio signals (e.g. WCDMA CREST factor up to ~10 dB). The controllable amplifier/attenuator in front of the ADC (see Figure 1) will increase the receiver signal receive range (MT near/far from the BS). The bandwidth (BW) of a single channel determines the minimum sampling rate (normally > 2×BW). The RFs for GPRS, WCDMA and HiperLAN2 are given in Figure 1.

SDR should perform as much as possible of the digital processing in the DSP in order to have the highest flexibility. However, for some of the intensive processing tasks like: digital down-conversion, channelisation - filtering and sample rate adaptation, dedicated DDC chipset solutions can be used. The DDC can be used for different radio standards by changing some parameters. The DSP has to perform tasks like: pulse shaping, searcher, Rake receiver (WCDMA), equaliser, FFT, IFFT (HiperLAN2), source and channel coding/decoding, etc. Following up various references, [7] - [9], we found that WCDMA requires most DSP processing power. For WCDMA, a DSP with at least ~10000 million instructions per second (MIPS) is needed (transmit and receive) in order to perform all the processing for one user channel. In MIPS, one instruction equals 2 memory operations and 1 arithmetic operation. In the value above, we have also added some safety margin to compensate for DSP code inefficiency and to account for the variation in MIPS definition from different manufacturers. The estimated MIPS for the DSP may be relaxed when specially designed co-processors arrive on the market, trimmed for special task like e.g. turbo coding – decoding.

Table 1: Radio requirements for the triple-standard MT

	DR, dB BL+HR+SNR	Channel BW, MHz	Radio BW, MHz
GPRS	78+6+10 = 94	0.2	35 / 75
WCDMA	70+13+0 = 83	5	60
HiperLAN2	55+9+6 = 70	20	200+255

III. INDUSTRY SDR COMPONENT TRENDS

In this section we look for the industrial availability on ADCs and DSPs, as these are the most critical devices in the proposed architecture considering: performance, power consumption and commercial availability in the near future. We assume that DDCs and the SDR components for the transmit path (e.g. DAC, DUC) with the required performance and acceptable power consumption will be available before ADC and DSP. In order for SDR based MTs to have similar active call time as current GSM MTs, we restricted the maximum power usage in both the DSP and the ADC to be ≤ 50 mW each.

A. Fast ADCs

In order to relax the blocking requirements on the ADC the use of passband SAW filters with relatively narrow bandwidths are suggested as shown in Figure 1. Considering performance and power consumption, sigma-delta converters with bandpass sampling would be the ideal choice. In GSM MTs sigma-delta baseband converters have been used over the last few years in order to reduce power consumption. Early GSM MTs used 4-bit Nyquist ADCs in combination with "large" automatic gain control (AGC) in order to give sufficient total signal receive range. For UMTS, bandpass sampling (BW ~5 MHz) sigma-delta converters promise low power consumption but they are currently still in the research stage. Furthermore, for HiperLAN2 the channel BW is 20 MHz and we do not expect sigma-delta converters to be commercially available to cover this BW within the next 5 years.

Nyquist converters offer a SNR of

$$SNR \sim 6.02 \cdot ENOB + 10\log\left(F_S / 2BW\right), \qquad (1)$$

where ENOB denotes effective number of bits (e.g. including noise and distortion) and the last term gives the processing gain where F_S is the sampling speed. In Figure 1 we assume bandpass sampling at IFs of ~600/300 MHz. The IF after the analogue mixer is set by the HiperLAN2 radio BW (see Table 1). Current converters with ≥ 10-bit can offer sampling rates up to ~200 MSPS and can have analogue input BW up to ~1 GHz with acceptable ENOB over this frequency range. For bandpass sampling, the sample rate only needs to be twice as high as the signal bandwidth to achieve the Nyquist sampling rate. The passband of the SAW filters in our receiver design are greater or equal to the channel BWs of the corresponding radio signal. Relaxation on the SAW filters can be obtained by increasing the sample rate, which softens the transition band requirements of the filters (lower costs). The blocking is mainly achieved by the digital filter after the ADC, and additionally from the SAW filters. For out-of–band blocking the filters at the RF front end have to give sufficient additional attenuation.

Figure 3 shows the power dissipation per mega samples per second (MSPS) for 12-bit Nyquist sampling converters (e.g. flash) over the last decade. Information for the various ADCs is obtained from data sheets of

various manufacturers or e.g. from reference [1]. Only ADCs, which are on the market, are considered. The power consumption per MSPS halves about every 2 years due to enhanced process technology and new architectures, as indicated by the slope of the first order best fit. The power consumption in general depends on sampling speed, number of bits, architecture and process technology.

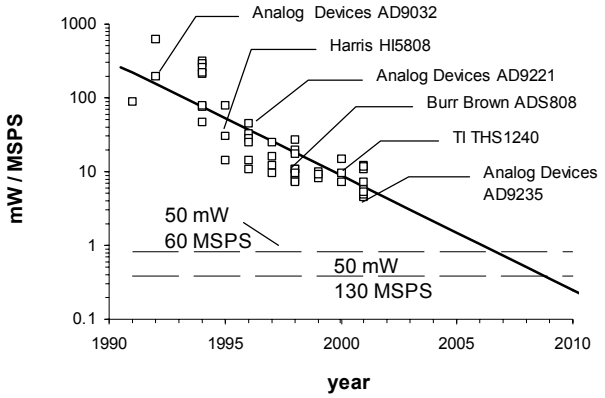

Figure 3: Power dissipation per MSPS for 12-bit ADCs over the last 10 years

ADC converters designed for SDR applications (BS) appeared on the market from about 1996 (e.g. the AD9221 from Analog Devices in Figure 3). For current 12-bit converters, ENOB is approximately 11. Using Equation (1) the effective SNR of 12-bit converters is ~66 dB. For a sampling speed of 60 MSPS the gain due to oversampling is ~22/8/2 dB for GPRS/WCDMA/ HiperLAN2, respectively. The SNR plus the gain due to oversampling has to fulfil the DR requirements in Table 1. The difference in the required blocking to the achieved blocking (~3/9/2 dB for GPRS/UMTS/ HiperLAN2, respectively) has to be obtained from the SAW filters in the IF receiver stage. The additional blocking over the radio band of interest should be easily obtainable with SAW filters, especially for the GPRS/HiperLAN2 radio paths. Using the data presented in Fig. 3, we estimate that 12-bit ADCs with sample rates > 60 MSPS and power consumption ≤ 50 mW should be available around the year 2007 (see crossing point of the straight line calculated for 50 mW/60 MSPS and the ADC development prediction).

Increasing the sampling rate to > 130 MSPS would allow sampling over the whole GPRS radio band as the ADC DR would fulfil the blocking requirements. This would also allow the GPRS signal to be within the WCDMA receiver path. However, from Fig. 3 it can be seen that 12-bit converters with such sampling speeds and low power consumption are not expected to be available before the year 2009 (see crossing point of the straight line calculated for 50 mW/130 MSPS and the ADC development prediction).

We have also investigated 14-bit Nyquist converters, the same way as for 12-bit converters in the sections above. We found that 14-bit converters with sufficient sampling speed (> 40 MSPS) and power consumption below 50 mW are not expected to be on the market before the year 2009. Using lower bit converters (e.g. 10-bit) the sampling speed would be too high in order to fulfil the blocking requirements in combination with reasonable "cheap" passband SAW filters. Therefore we could conclude that 12-bit converters are the best compromise considering sampling speed, power consumption and future availability on the market.

B. Low cost DSPs

Figure 4 shows the power consumption per MIPS as a function of time for "low cost" DSPs on the market (see also e.g. reference [10]). The trend basically follows Moore's law, which states that the capacity or energy efficiency of DSPs doubles every 18 months. The power consumption per MIPS halves about every 18 months as indicated by the slope of the first order best fit. DSP power consumption is proportional to the number of gates, gate capacitance, clock frequency and the operating voltage to the power of two.

The DSP MIPS used in the figure assume maximum use of all execution units. Accounting for this and other inaccuracies for MIPS estimation we estimated an upper value of ~10000 MIPS to be sufficient for the triple-standard mobile terminal considered in this paper. The value is given by the required WCDMA radio signal processing (transmit and receive). Low-cost DSPs with such a performance and power consumption < 50 mW (see straight line in Figure 4 calculated for 50 mW / 10000 MIPS) could arrive in the market at ~2006, assuming industrial trends continue as indicated in the best fit first order slope given in Figure 4.

In general the performance of DSPs will continue to increase as the chip sizes are reduced and the number of gates are increased. Also, fundamentally new structures may have significant impact on the DSP performance, e.g. the development of fully asynchronous and globally asynchronous locally synchronous circuits [11].

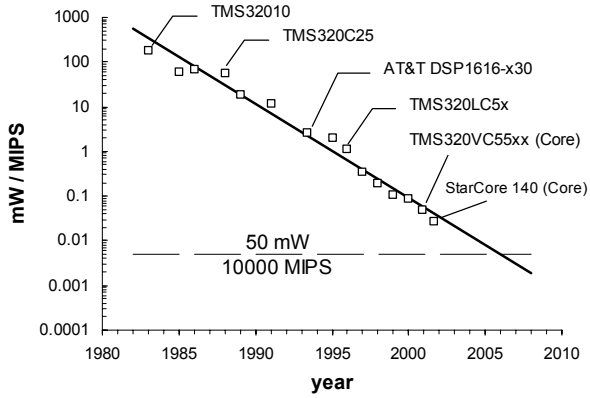

Figure 4: Power dissipation per MIPS for low cost DSPs over the last 18 years

IV. SUMMARY

Multi-standard mobile terminals (e.g. GPRS, WCDMA, HiperLAN2 and 2.4 GHz Bluetooth and WLAN) are of interest to operators as the available radio spectrum can be used in a very efficient way. Radio signal digitisation at an IF can be used to enable such mobile terminals in the near future by using partial band digitisation with passband SAW filters in order to fulfil radio requirements such as blocking.

Comparing the power consumption of a conventional superheterodyne GPRS MT receiver (ASCIs) with the proposed IF sampling SDR architecture we found that the power consumption in an SDR GPRS receiver is ~4 times higher using currently existing components. The ADC is the main power consumer for SDR. This power consumption difference will not change much in the future as advances in areas such as process technology and/or lower voltage operation applies to both receivers. However SDR, due to its flexibility, allows new power saving algorithms to be employed faster, which may offset the power consumption difference.

For the proposed IF digitising receiver architecture we could estimate by following industry trends (e.g. Moore's law) that SDR components (DSPs and ADCs) with reasonable power consumption (as observed in current MTs) should be available within the next 5 years in order to fulfil the GPRS/WCDMA/HiperLAN2 standard requirements as e.g. for blocking and processing power. ADCs with 12-bit resolution are the better choice compared e.g. to 14-bit converters regarding power dissipation, required sampling rate and future commercial availability. Further in the future (> 5 years) we believe that bandpass sampling sigma-delta converters are the ideal choice considering performance and power consumption, as observed in GSM MT implementations over the last few years. WCDMA, regarding blocking and ADC performance and DSP MIPS, sets the upper performance requirements. A GPRS and HiperLAN2 solution could work with relaxed requirements.

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