Packet clock recovery using a bismuth oxide fiber-based optical power limiter

Ch. Kouloumentas[1*], N. Pleros[1], P. Zakynthinos[1], D. Petrantonakis[1], D. Apostolopoulos[1], O. Zouraraki[1], A. Tzanakaki[2], H. Avramopoulos[1], I. Tomkos[2]

[1]National Technical University of Athens – Department of Electrical Engineering and Computer Science, 9 Heroon Polytechniou Street, Zografou 15773 – Athens, Greece.
[2]Athens Information Technology Center (AIT), 19.5 km Markopoulou Av., 19002, Peania, Greece
**Corresponding author: ckou@mail.ntua.gr*

Abstract: We demonstrate an optical clock recovery circuit that extracts the line rate component on a per packet basis from short data packets at 40 Gb/s. The circuit comprises a Fabry-Perot filter followed by a novel power limiting configuration, which in turn consists of a 5m highly nonlinear bismuth oxide fiber in cascade with an optical bandpass filter. Both experimental and simulation-based results are in close agreement and reveal that the proposed circuit acquires the timing information within only a small number of bits, yielding a packet clock for every respective data packet. Moreover, we investigate theoretically the scaling laws for the parameters of the circuit for operation beyond 40 Gb/s and present simulation results showing successful packet clock extraction for 160 Gb/s data packets. Finally, the circuit's potential for operation at 320 Gb/s is discussed, indicating that ultrafast packet clock recovery should be in principle feasible by exploiting the passive structure of the device and the fsec-scale nonlinear response of the optical fiber.

OCIS codes: (060.4370) Nonlinear optics, fibers; (070.4340) Nonlinear optical signal processing

References and links

1. R. Ludwig, W. Pieper, E. Jahn, N. Agrawal, A. Ehrhardt, L. Kuller, H.G. Weber, "10GHz all-optical clock recovery using a mode-locked semiconductor laser in a 40Gbit/s, 100-km transmission experiment," in Proceedings of IEEE Conference on Optical Fiber Communications, (Institute of Electrical and Electronics Engineers, Anaheim, 1996), 167-168, WH2.
2. O. Kamatani, S. Kawanishi, "Ultrahigh speed clock recovery with phase locked loop based on four-wave mixing in a travelling-wave laser diode amplifier," J. Lightwave Technol. **14**, 1557-1568 (1996).
3. Y. Yang, Y. J. Wen, A. Nirmathalas, H. F. Liu, and D. Novak, "Optical clock recovery at line rates via injection locking of a long cavity Fabry-Pérot laser diode," IEEE Photon. Technol. Lett. **16**, 1561-1563 (2004).
4. B. Sartorius, C. Bornholdt, S. Bauer, and M. Möhrle, "40 GHz optical clock recovery for application in asynchronous networks," in Proceedings of the 2001 European Conference on Optical Communications (ECOC, Amsterdam, 2001), 442-443, We. P.32.
5. N. Pleros, K. Vyrsokinos, C. Bintjas, K. Yiannopoulos, K. Vlachos, H. Avramopoulos, and G. Guekos, "All-Optical Clock Recovery from Short Asynchronous Data Packets at 10 Gb/s," IEEE Photon. Technol. Lett. **15**, 1291-1293 (2003).
6. E. Kehayas, L. Stampoulidis, H. Avramopoulos, Y. Liu, E. Tangdiongga and H.J.S. Dorren, "40 Gb/s all-optical packet clock recovery with ultrafast lock-in time and low inter-packet guardbands," Opt. Express **13**, 475-480 (2005).
7. Ch. Kouloumentas, A. Tzanakaki, and I. Tomkos, "Clock Recovery at 160 Gb/s and beyond, using a Fiber Based Optical Power Limiter," IEEE Photon. Technol. Lett. **18**, 2365-2367 (2006).
8. G. V. Agrawal, *Nonlinear Fiber Optics*, *3rd Ed.* (Academic Press, Inc., 2001).

1. Introduction

Optical packet switching has been introduced as the main concept for improving the

#77088 - $15.00 USD Received 15 Nov 2006; revised 21 Mar 2007; accepted 21 Mar 2007; published 24 Jul 2007

utilization of the network resources offering increased bandwidth efficiency and reducing latency in future optical networks. The realization of optical packet switched networks relies strongly on the development of intra-node signal processing subsystems capable of handling the incoming information on a per packet basis directly in the optical domain. In the case of clock extraction procedures, these requirements necessitate the implementation of all-optical clock recovery circuits capable of immediately acquiring the timing information whereas retaining the synchronization signal only for a duration similar to that of the data packets.

So far, several all-optical clock recovery techniques have been demonstrated, including mode-locked ring lasers [1], optical phase-locked loops [2], Fabry-Pérot lasers [3], self-pulsating lasers [4] and circuits based on a Fabry-Pérot filter (FPF) [5-6]. Among these configurations, only the self-pulsating lasers and the FPF-based schemes have performed successfully with packet-formatted optical traffic. However, both schemes employ active semiconductor-based materials for successful packet clock extraction, implying that the operational bit-rates of these configurations depend on the carrier dynamics of the active elements. In order to avoid this dependence and the associated operational bit-rate limitations, a new concept has been recently introduced that utilizes fiber-based power limiting designs after an FPF, allowing for data processing at the fibers' nonlinearity time parameters [7].

In this article, we provide for the first time to our knowledge the experimental proof-of-principle of this concept, demonstrating successful packet clock recovery at 40 Gb/s using an FPF and a fiber-based power limiter. The power limiter incorporates a 5-m long bismuth oxide fiber with high nonlinearity followed by an optical bandpass filter (OBPF), tuned at the central wavelength of the inserted data. The properties of this device arise from the self-phase modulation (SPM)–induced spectral broadening of the signal during its propagation in the fiber and its subsequent filtering. A simulation model of the scheme has been developed, and its validity has been verified by simulation results for the clock extraction process at 40 Gb/s, which appear in close agreement with the experimental results. In addition, a theoretical investigation of the scaling laws for the circuit parameters towards higher operational bit-rate is presented, and the application of this study for clock extraction even for 160 Gb/s data packets is demonstrated through simulation results. Finally, the circuit potential for operation at 320 Gb/s is discussed and parameters for clock recovery at this rate are extracted, revealing that ultrafast timing extraction could be in principle feasible by exploiting the passive structure of the device and the practically instantaneous response of the Kerr nonlinearity.

2. Operating principle of the clock recovery circuit

The packet clock recovery circuit encompasses two main subsystems, i.e. the FPF and the optical power limiter. If the FSR of the FPF equals to the line rate, the FPF partially fills the spaces of the incoming data stream from the preceding marks and creates an output that resembles the packet clock signal but suffers from strong intensity modulation. The FPF finesse defines the intensity modulation at its output, as well as the required time for the loss of the clock synchronization after each data packet. The optical power limiter follows the FPF in order to remove the intensity modulation of the FPF output. Its operation is based on the spectral broadening of the optical signal during its propagation in a highly nonlinear fiber operating in the normal dispersion regime, and its subsequent optical filtering around the central wavelength. Spectral broadening of optical pulses in the fiber, induced by the SPM effect varies with the pulse peak power. As such, the high peak power pulses at the output of the FPF experience enhanced spectral broadening compared to the low peak power ones, and the spectral density of both high and low peak power pulses tends to be equalized in the spectral region around the central wavelength. To this end, the tuned OBPF at the output of the fiber yields a power equalized pulse sequence at its output.

The power limiting properties of this subsystem have been verified by extracting the experimental output vs. input power transfer function characteristics using the setup shown in

#77088 - $15.00 USD Received 15 Nov 2006; revised 21 Mar 2007; accepted 21 Mar 2007; published 24 Jul 2007

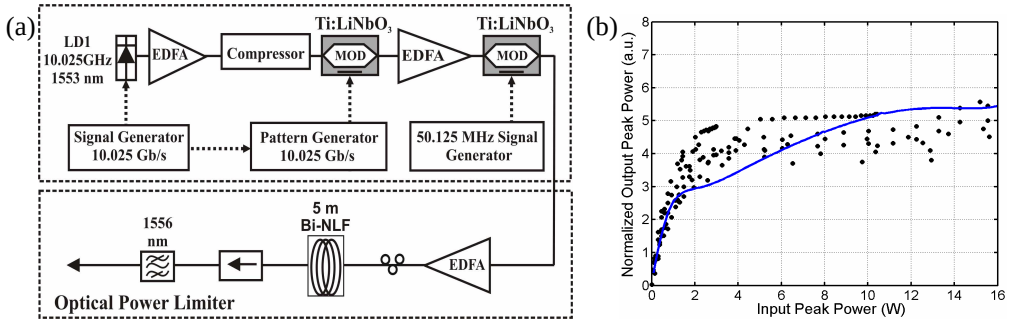

Fig. 1. a) Experimental setup for the derivation of the optical power limiter's transfer function using input pulses of 3 ps pulse width. b) The experimental (black dots) power-limiting output vs. input peak power transfer function. The blue line corresponds to the simulated transfer function.

Fig. 1(a). It consists of a 10 Gb/s optical packet generator, a sinusoidally modulated clock packet generator and the power limiter, consisting of a 5-m long bismuth oxide fiber and an OBPF of 0.6 nm bandwidth around the central wavelength of 1553 nm. The pulse width is 3 ps whereas the attenuation, the dispersion and the nonlinear parameter of the bismuth oxide fiber are 1.3 dB/m, -270 ps/nm/km and 950 $W^{-1}km^{-1}$, respectively. The sinusoidal modulation of the 10 Gb/s packet clocks provides a controllable way for calculating the peak power of every pulse for a given average power of the signal inserted into the power limiter, whereas the amplitude modulation of the output pulses for the same input average power yields the corresponding normalized output pulse peak powers. By repeating this measurement procedure for various average powers of the input signal, the experimental output vs. input power transfer function of the device has been obtained and is illustrated by the black dots in Fig. 1(b). The blue line illustrates the corresponding simulated transfer function obtained by a model described in more detail in section 4. As can be recognized, the combination of the highly nonlinear fiber and the OBPF yields a step-like output vs. input power transfer function with low threshold and extended plateau, demonstrating that power equalization within 2 dB is obtained even when input pulses with amplitude modulation greater than 9 dB are used.

3. Experimental setup for clock recovery at 40 Gb/s and results

The experimental validation of the proposed clock recovery circuit has been based on the experimental setup illustrated in Fig. 2. It consists of a 40 Gb/s optical data packet generator, a hybrid integrated SOA-based Mach Zehnder interferometer (HMZI) acting as a wavelength converter, and the clock recovery unit that employs a fiber FPF followed by the fiber-based power limiter. The 40 Gb/s packet traffic is generated as follows: a 1553 nm DFB laser is gain switched at 10.025 Gb/s in order to produce 3 ps pulses after both linear and nonlinear compression. After exiting the compression stage, the pulse train enters a $Ti:LiNbO_3$ electro-optical modulator driven by a 10.025 Gb/s pattern generator and is inserted into a fiber-based bit-interleaver to form 2^7-1 PRBS data packets at 40.1 Gb/s. The packet-formatted data traffic is subsequently used as the control signal in the HMZI-based wavelength converter that operates in a push-pull configuration, providing at its output a 40.1 Gb/s signal at 1556 nm with 7 ps pulse width. The wavelength conversion stage is required for assigning a local phase and a fresh wavelength to the data signal in order to ensure successful pulse addition by the FPF and perfect matching with one of the filter transmission peaks, respectively. The wavelength converted signal enters the clock recovery unit and specifically the fiber FPF, which has an FSR equal to the line rate and a finesse of 39. Subsequently, the FPF output is amplified by a high-power EDFA with 21 dBm average power and 7 dB noise figure, and is coupled in the 5 m long bismuth oxide fiber with its parameters as given in the previous section. Finally, the fiber output is filtered around the 1556 nm wavelength by an OBPF of 0.6 nm bandwidth, and it is detected. Fig. 3 illustrates the experimental results through traces and eye diagrams. Fig. 3(a) shows a typical sequence of two incoming data packets at 40 Gb/s and Fig. 3(b) depicts the respective wavelength converted signal before entering the FPF. The FPF

#77088 - $15.00 USD Received 15 Nov 2006; revised 21 Mar 2007; accepted 21 Mar 2007; published 24 Jul 2007

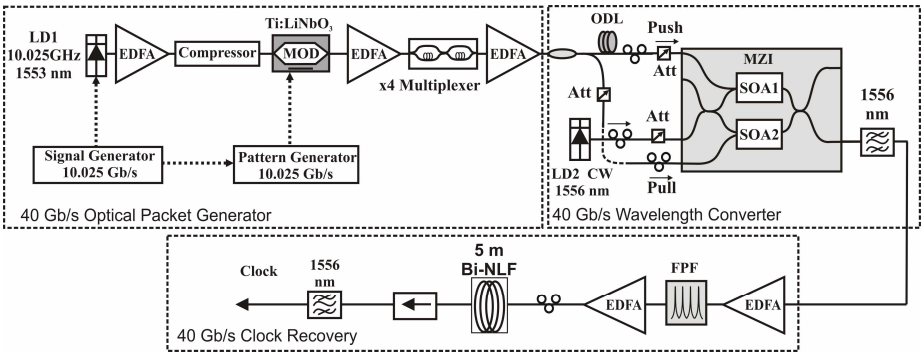

Fig. 2. Experimental setup for packet clock recovery at 40 Gb/s.

transforms the data packet sequence into a packet clock resembling signal utilizing its "memory" properties. Fig. 3(c) shows the respective packet clocks obtained at the FPF output, revealing intense peak power variation between the clock pulses, and clock signal duration similar to the duration of the original packets. Finally, Fig. 3(d) illustrates the recovered clock packets obtained at the output of the circuit showing that peak power variation has been removed as a result of the power limiting properties of the nonlinear fiber- and OBPF-based configuration. The width of the clock pulses has been found equal to 6.5 ps, well below the pulse width of the signal launched in the clock recovery module. Comparing the eye diagrams of Fig. 3(c) and 3(d) no additional timing jitter is observed to be induced by the optical power limiter. This attractive property arises from the fact that the OBPF is tuned around the central wavelength, and hence its pass-band always corresponds in the time domain to the low-chirp

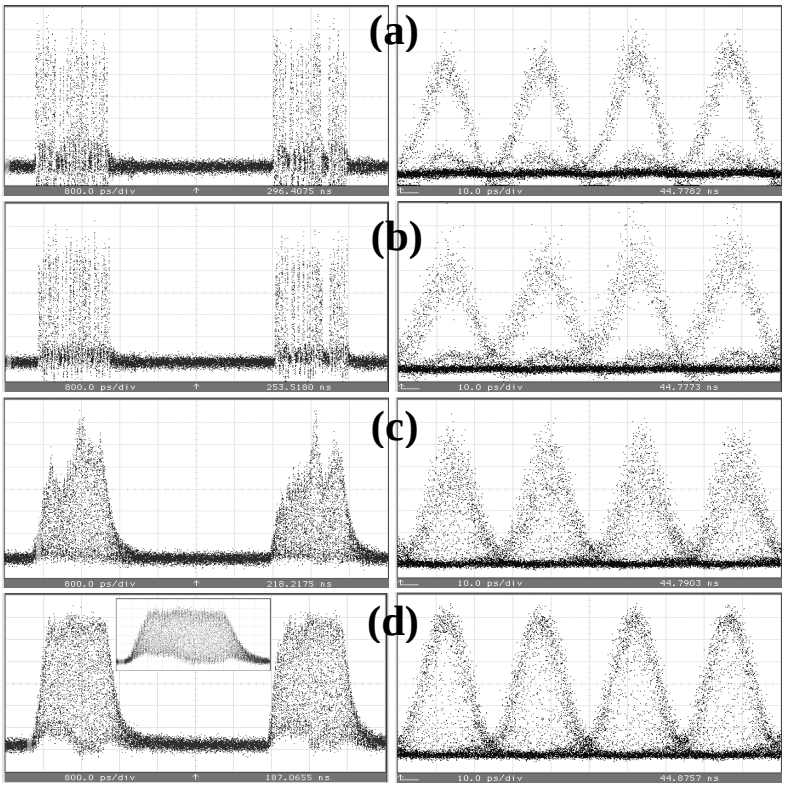

Fig. 3. Traces and eye diagrams of a) the input signal, b) the wavelength converted signal, c) the signal at the output of the FPF, and d) at the output of the clock recovery unit. Time base is 800 ps/div for the traces and 10 ps/div for the eye diagrams. In the inset of Fig. 3(d) a detailed representation of the first packet clock is given.

#77088 - $15.00 USD Received 15 Nov 2006; revised 21 Mar 2007; accepted 21 Mar 2007; published 24 Jul 2007

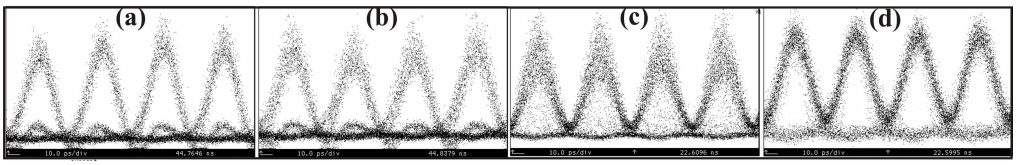

Fig. 4. Eye diagrams of the a) input signal, b) wavelength converted signal, c) output of the FPF, and d) output of the clock recovery unit, when longer packets serve as input. Time base is 10 ps/div.

region around the peak power of each pulse. Finally, clock acquisition and synchronization loss are achieved within only 6 and 12 bits respectively, leading to ultra-fast clock rise- and fall-times that appear as hits inside the eye diagram of Fig. 3(d). These hits are almost vanished and the high quality of the extracted clock pulses becomes more evident when longer data packets are used as input signal. In this case, the sum of the leading and trailing edge bits remains constant whilst the total number of the acquired clock bits increases with the packet size, yielding a clearer eye for the output signal. This is confirmed by Fig. 4 that shows the signal evolution when packets of longer duration are inserted into the circuit. As illustrated in Fig. 4(d), an open eye for the recovered packet clock signal is obtained, proving that the hits inside the eye diagram of Fig. 3(d) are a result of the non-perfect rise- and fall-pulses.

4. Simulation results and extension of the concept at higher data rates

A model has been developed using the commercially available VPI simulation platform in order to simulate the operation of the clock recovery circuit for various bit patterns. The reported experimental values outlined in section 3 have been assigned to the parameters of the pulse width at the wavelength converter output, the FPF, the optical amplifier, the highly nonlinear fiber and the OBPF. The amplified output of the FPF and the derived clock packets at the output of the power limiter for 40 Gb/s input data packets are illustrated in Fig. 5(a) and 5(b), respectively, showing good agreement with the experimental results depicted in Fig. 3(c) and 3(d), verifying in this way the validity of the model. In the insets of Fig. 5(a) and 5(b), the respective eye diagrams and a detailed representation of the first packet clock are depicted.

Given that the fiber-based power limiter does not impose any speed limitations due to the fast response of the fiber Kerr nonlinearity, operation of the circuit at rates beyond 40 Gb/s is envisaged by applying simple scaling laws. The starting point of the theoretical analysis is the normalized nonlinear Schrödinger equation that models the longitudinal evolution of the complex electric field $u(\tau,\xi)$ of a pulse in a lossless normally dispersive fiber [8]:

$$i\frac{\partial u}{\partial \xi} = \frac{1}{2}\frac{\partial^2 u}{\partial \tau^2} - N^2|u|^2 u \tag{1}$$

ξ, τ and N are the normalized distance and time variables, and the "soliton number" respectively, introduced as follows:

$$\xi = z/L_D = z|\beta_2|/T_0^2, \quad \tau = T/T_0, \quad N^2 = L_D/L_{NL} = (\gamma P_0)\cdot T_0^2/|\beta_2| \tag{2}$$

where L_D and L_{NL} are the dispersion and the nonlinear length, β_2 and γ are the second order dispersion and the nonlinear coefficient of the fiber, and finally T_0 and P_0 denote the characteristic temporal width and the peak power of the input pulse. Scaling the demonstrated case to 160 Gb/s, the temporal width of the pulses launched in the bismuth oxide fiber is reduced by a factor of 4 from 7 ps to 1.75 ps. According to Eq. 2 increasing the peak power of the input pulses by a factor of 16, the "soliton number" retains its value, and consequently the same solutions apply for Eq. 1. Taking into consideration that the normalized distance and time variables participate in Eq. 1, the same power limiting characteristics are obtained at 160 Gb/s, if the fiber is 16 times shorter and the bandwidth of the OBPF is 4 times wider.

By applying these scaling laws to the simulation model, the scalability of the concept at 160 Gb/s has been investigated. The bit pattern of the data packets entering the FPF is the one used in the experimental demonstration at 40 Gb/s, whereas the pulse width is 1.75 ps. The FPF has 160 GHz FSR and finesse equal to 39, while its output is amplified up to 30.3 dBm average power, and it is launched in a 0.3 m long bismuth oxide fiber. The peak powers of the

#77088 - $15.00 USD Received 15 Nov 2006; revised 21 Mar 2007; accepted 21 Mar 2007; published 24 Jul 2007

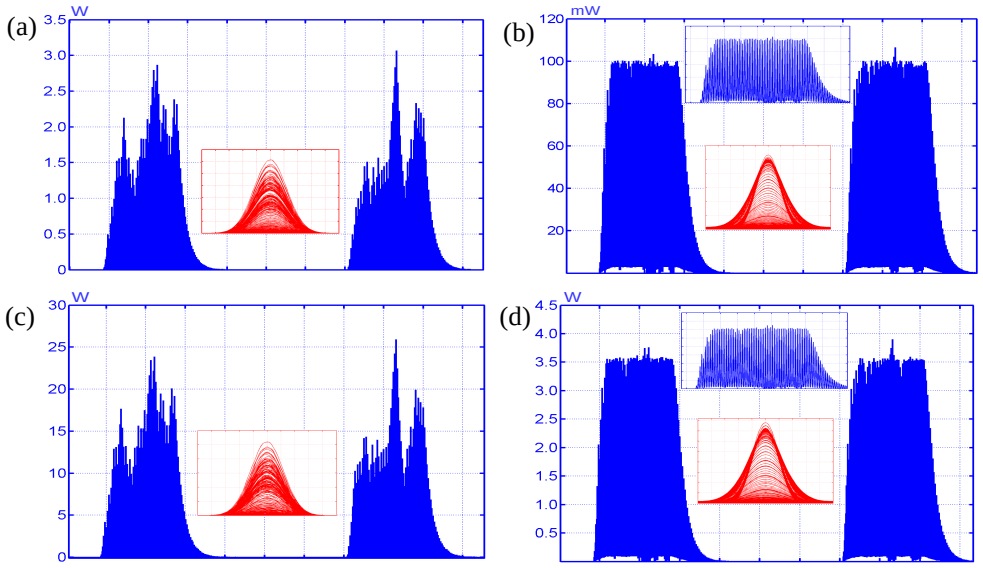

Fig. 5. Simulation traces (eye diagrams as insets) of a) the input of the fiber at 40 Gb/s, b) the output of the clock recovery circuit at 40 Gb/s, c) the input of the fiber at 160 Gb/s, and d) the output of the clock recovery circuit at 160 Gb/s. Time base is 200 and 800 ps/division for traces at 40 and 160 Gb/s, respectively. In upper insets of fig. 5(b) and 5(d) detailed representations of the first packet clock are given.

pulses are not actually 16 times higher compared to the 40 Gb/s case, but significantly lower, since the pulses propagate in a shorter piece of fiber, and thus undergo lower attenuation. Finally, the output of the fiber is filtered by a 2.4 nm OBPF and is detected. In Fig. 5(c) the amplified output of the FPF is given, having the same intensity modulation characteristics as in the 40 Gb/s case. In Fig. 5(d) the illustrated 160 GHz recovered clock signal resembles the respective 40 GHz clock signal (Fig. 5(b)) and exhibits the same qualitative characteristics as far as the rise and fall times and the residual peak power variation are concerned.

In case the circuit operation at even higher bit rate is targeted, the same scaling laws should be followed. At 320 Gb/s for example, the pulse width should be further reduced by a factor of 2. In order to avoid an increase of the pulses' peak power, which would necessitate an extremely high power of the optical amplifier at the input of the fiber, a fiber exhibiting the same nonlinearity but 4 times lower dispersion could be employed, thus leaving the "soliton number" unaffected. Consequently, the same traces and eye diagrams of Fig. 5(b) and 5(d), could be obtained if the input pulses have 0.875 ps pulse width, the output of the FPF is amplified up to 30.3 dBm, a 0.3 m long fiber with nonlinearity of 950 $W^{-1}km^{-1}$ and dispersion of -67.5 ps/nm/km is used, and finally if the subsequent, tuned OBPF has 4.8 nm bandwidth.

5. Conclusions

We have experimentally demonstrated the proof-of-principle operation of a clock recovery module consisting of a FPF and a bismuth oxide fiber-based optical power limiter with 40 Gb/s input data packets. The proposed concept relies on the memory properties of the FPF in combination with SPM-induced spectral broadening of the pulses in the nonlinear fiber and subsequent bandpass filtering. Taking advantage of the ultra-fast fiber Kerr-nonlinearity, we present simulation results of the circuit operation at 160 Gb/s and investigate its requirements for clock extraction at 320 Gb/s, highlighting the potential of the technique to provide packet processing capabilities required by optical packet switched nodes at extremely high data rates.

Acknowledgments

This work has been supported by the European network of excellence e-Photon/ONe and the EU COST 291 action. The authors would like to acknowledge Dr. N. Sugimoto for providing the bismuth oxide fiber and Exelite Innovations Ltd for the supply of the high-power EDFAs.

#77088 - $15.00 USD Received 15 Nov 2006; revised 21 Mar 2007; accepted 21 Mar 2007; published 24 Jul 2007