New Layout Scheme to Improve ESD Robustness of I/O Buffers in Fully-Silicided CMOS Process

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Abstract – Silicidation used in CMOS processes has been reported to result in substantial degradation on ESD robustness of CMOS devices. In this work, a new ballasting layout scheme for fully-silicided I/O buffer is proposed to enhance its ESD robustness. Experimental results from real IC products have confirmed that the new ballasting layout scheme can successfully increase HBM ESD robustness of fully-silicided I/O buffers from 1.5kV to 7kV without using the additional silicide-blocking mask.

I. Introduction

To increase the driving capability and the maximum operating frequencies of MOS field-effect transistors (MOSFETs), silicidation has been widely adopted in chip fabrications since deep-submicron CMOS era. Although the low resistivity from silicides is advantageous to the driving capability and operating frequencies of MOSFETs, it has been reported that silicidation results in precipitous degradation on ESD protection levels of CMOS ICs in advanced CMOS technologies [1], [2].

To recover the silicidation-induced degradation on ESD robustness, CMOS processes with additional silicide blocking (SB) has been proposed. However, additional mask and process steps are required for silicide blocking. As a result, introducing SB into the CMOS manufacturing processes will increase the fabrication cost. To compromise with the fabrication cost, or owing to the inaccessibility of SB in some given process technologies, some cost-effective ballasting techniques have been proposed to improve ESD robustness of fully-silicided MOSFETs [3]-[8].

II. Ballasting Techniques to Fully-Silicided I/O Buffers

Due to the huge discharging current in ESD events, current crowding has been known to cause serious impact on ESD protection devices. By increasing the ballast resistance in the ESD protection MOSFETs, ESD current path can be spread deeper into the substrate of large volume, which in turn improves ESD robustness [9]. Moreover, sufficient ballast resistance can improve the turn-on uniformity of ESD protection NMOS with multi-fingers in layout.

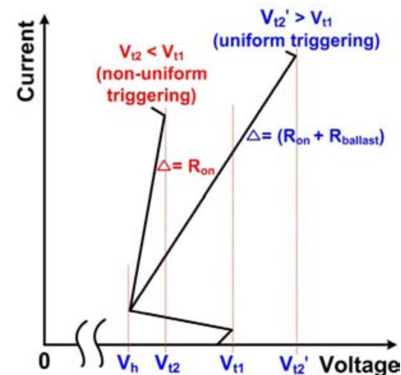


Figure 1: Current-voltage (I-V) characteristics of gate-grounded NMOS for ESD protection, indicating the relation between V_{t2} and V_{t1} values to the uniform or non-uniform triggering.

In a multi-finger NMOS, different distances from the drain region of each finger to the grounded guard ring result in asymmetry of substrate resistance to cause the central fingers of NMOS more easily triggered on under ESD stresses [10]. After the triggering of the multi-finger NMOS under ESD stresses, the ESD overstress voltage is clamped to its holding voltage (V_h) plus the product of ESD current (I_{ESD}) and the turn-on resistance (R_{on}). The typical I-V curve of gate-grounded NMOS under ESD stress is illustrated in Fig. 1. Without sufficient ballast resistance, ($I_{ESD} \times R_{on}$) is not large enough to make the secondary breakdown voltage (V_{t2}) higher than the trigger

voltage (V_{t1}). As a result, ESD current is concentrated in some earlier turned-on area to cause local damages but the rest area cannot be triggered on in time to discharge ESD current. Such non-uniform turn-on behavior among the multiple fingers of NMOS limits its ESD robustness, even if the NMOS was drawn with a large device dimension. By introducing the ballast resistance $R_{ballast}$, turn-on resistance of the multi-finger NMOS can be increased from R_{on} to (R_{on} + $R_{ballast}$). As long as the V_{t2}' can be increased greater than V_{t1}, the multi-finger NMOS can be uniformly triggered on during ESD stresses [11]. As a result, sufficient ballast resistance can force ESD current being conducted into the deeper substrate, and also increase the ESD robustness due to the improvement of turn-on uniformity among the multiple fingers of gate-grounded NMOS.

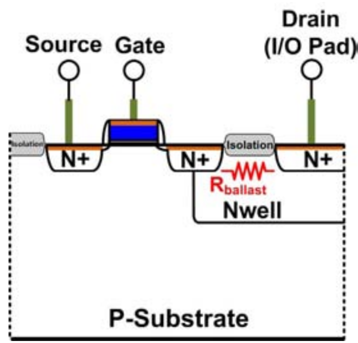


Figure 2: Ballast Nwell to increase the ballast resistance of NMOS.

To realize the ballast resistance in fully-silicided NMOS, one of the layout methods is to use the high sheet resistance from Nwell. Fig. 2 shows the device cross-sectional view of an NMOS with the Nwell ballasting technique. The ballast Nwell electrically shorts the separated diffusions and contributes the desired $R_{ballast}$ to the overall turn-on resistance of NMOS [3], [4]. For the facility of description, the separated diffusion that connects to the input/output (I/O) pad is labeled as the island diffusion in this paper. The other separated diffusion, which is closer to the gate of MOSFET, is labeled as the drain diffusion. Isolation in the drawing of figures in this paper represents either field oxide (FOX) or STI.

Although the Nwell ballasting technique is useful and easy to be utilized on fully-silicided NMOS, it cannot be applied to fully-silicided PMOS which is implemented in the Nwell. In this work, whole-chip ESD robustness of fully-silicided I/O buffers without ballasting and with Nwell ballasting technique in a 0.35-μm fully-silicided CMOS process are studied in section III and section IV, respectively. A new ballasting layout scheme is proposed in section V to effectively improve ESD robustness of I/O buffers with fully-silicided NMOS and PMOS transistors. Experimental results from real IC products fabricated in the 0.35-μm fully-silicided CMOS process have confirmed that the new ballasting layout scheme can successfully increase HBM ESD robustness of fully-silicided I/O buffers from the original 1.5kV to 7kV without using the additional silicide-blocking mask.

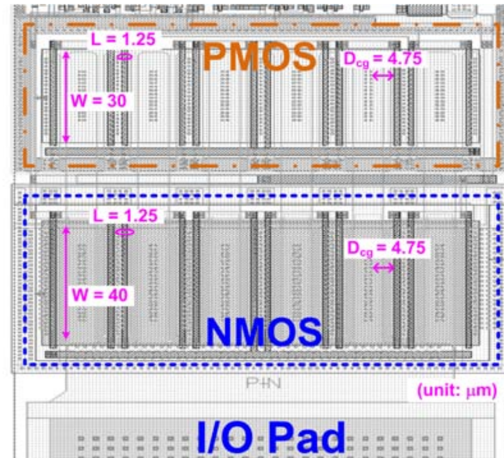


Figure 3: Layout top view of the self-protecting fully-silicided I/O buffer in a CMOS IC product.

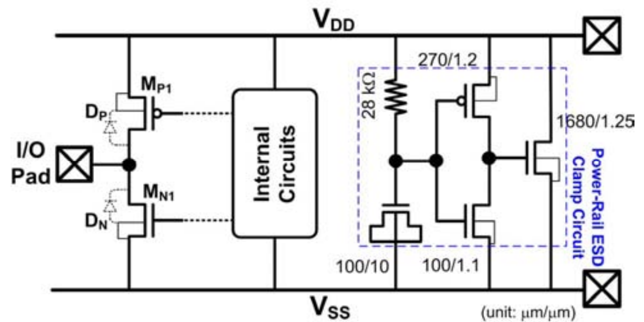


Figure 4: Whole-chip ESD protection scheme and the corresponding device dimensions of the power-rail ESD clamp circuit used in this work.

III. Fully-Silicided I/O Buffer without Ballasting

In nowadays CMOS ICs, to minimize the required layout area for I/O buffers, self-protecting I/O design (I/O buffer without additional ESD protection devices) is usually adopted. In the self-protecting fully-silicided I/O buffer without ballasting investigated in this work, device dimension (W/L) for buffer NMOS is 480μm/1.25μm with each finger width of 40μm, and device dimension for buffer PMOS is 360μm/1.25μm with each finger width of 30μm. The spacing for drain contact to poly gate edge (D_{cg}) is 4.75μm for both buffer NMOS and PMOS, which is originally drawn for silicide-blocking rules.

However, to reduce the fabrication cost, no silicide-blocking is adopted in the given CMOS process for IC production. Layout top view of fully-silicided I/O buffers is shown in Fig. 3. There is an on-chip active power-rail ESD clamp circuit for whole-chip ESD protection [12], where the main ESD protection NMOS has total device dimension of 1680µm/1.25µm with gate-driven technique, as shown in Fig. 4. Target for ESD robustness of those IC products requested by customers is to pass 6kV human body model (HBM) ESD test. To verify ESD robustness, the starting voltage of HBM ESD test is 0.5kV, and the step for the HBM ESD tests is 0.5kV. Each pin is stressed three times at an HBM ESD level and the failure criterion is I-V shift over 20% compared to the original I-V curve before ESD stress. The test will stop when ESD failure happens on one or more I/O (including power) pin(s).

Without ballasting design, the fully-silicided I/O buffers failed to pass the essential ESD specification of 2kV HBM ESD stresses. Among the ESD measurements of the un-ballasted I/O buffers, positive I/O-to-V_{SS} (PS-mode) ESD test showed the lowest ESD protection level. Under the PS-mode ESD stresses, the ESD current is first discharged to V_{DD} through the P+/Nwell forward diode inherent in buffer PMOS, and to the grounded V_{SS} through the power-rail ESD clamp circuit. In spite of the gate driven technique to enhance turn-on speed of power-rail ESD clamp circuit during ESD stresses [13], the voltage overshoot on the I/O pad cannot be completely suppressed due to the inevitable turn-on resistance of devices and interconnects. Consequently, due to the lack of proper ballasting design, as long as the voltage overshoot on the I/O pad induces breakdown of the fully-silicided buffer NMOS, it is easily filamented due to severe current crowding and non-uniform triggering.

Scanning electron microscope (SEM) image of the un-ballasted I/O buffer after 2kV PS-mode ESD stress is shown in Fig. 5, where the trace of current filamentation is found on the buffer NMOS. The failure analysis (FA) result has verified that the buffer NMOS is driven into breakdown during the 2kV PS-mode ESD test. Non-uniform triggering among the multiple fingers of the un-ballasted buffer NMOS can be clearly observed in Fig. 5, since ESD failure only locates on one of the fingers. The burned-out trace from drain to the grounded source through silicon surface further indicates that insufficient ballast resistance makes the ESD current to crowd on the surface with limited shallow depths. Accordingly, the D_{cg} spacing of 4.75µm in a fully-silicided NMOS is insufficient to provide adequate ballast resistance due to the small sheet resistance from silicides.

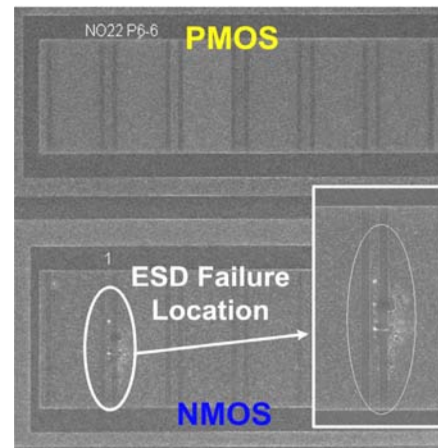
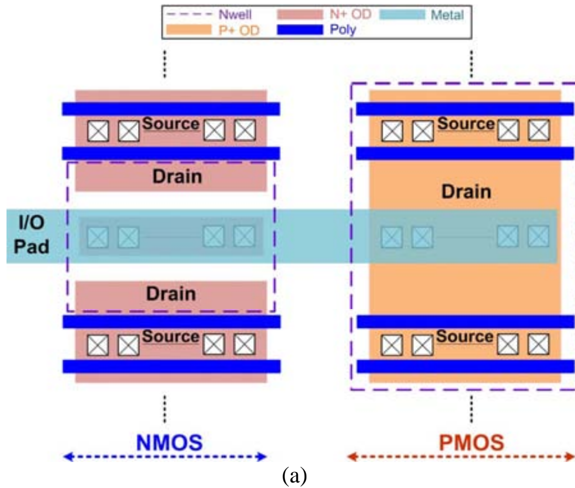


Figure 5: SEM image of the fully-silicided I/O buffer without ballasting after 2kV PS-mode ESD stress.

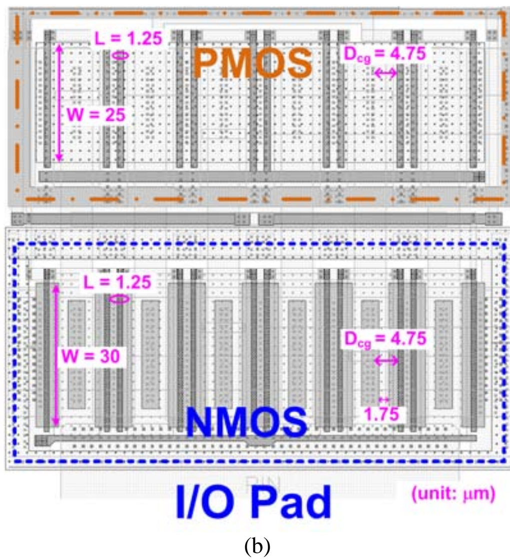
IV. I/O Buffer with Nwell Ballasting Technique on Buffer NMOS

Without ballasting design to the fully-silicided I/O buffer, the buffer NMOS is easily burned-out under the PS-mode ESD test. To enhance the PS-mode ESD robustness, the Nwell ballasting technique was applied to the buffer NMOS of I/O buffer [3], [4]. The main ESD protection NMOS in the active power-rail ESD clamp circuit was also implemented with Nwell ballasting. The buffer PMOS was still left un-ballasted in this test. Fig. 6(a) illustrates the I/O buffer with Nwell ballasting technique on buffer NMOS and the metal connection to the I/O pad. To keep the same cell width of I/O buffers in IC chips, both D_{cg} spacing and gate length are kept the same as those in the I/O buffers without ballasting. In the I/O buffers with Nwell ballasting, each finger width of buffer NMOS is 30µm, and each finger width of buffer PMOS is 25µm. Fig. 6(b) shows the layout of the I/O buffer and the corresponding device parameters. The total device dimension (W/L) of NMOS (PMOS) in I/O buffer drawn in the layout of Fig. 6(b) is 360µm/1.25µm (300µm/1.25µm). Buffer NMOS with ballast Nwell in this test was laid out with truncation to the island diffusions to prevent ESD damage from the tips of N+ island diffusions to the P+ guard ring.

With the Nwell to ballast buffer NMOS, the PS-mode ESD robustness of I/O buffers are substantially increased to over 4.5kV. However, the I/O buffers with Nwell ballasting failed at 4.5kV negative I/O-to-V_{DD} (ND-mode) test, which becomes the bottleneck



(a)



(b)

Figure 6: (a) Illustration of the metal connection to the I/O pad for the buffer NMOS with ballast Nwell but the buffer PMOS without ballasting. (b) Layout top view of the fully-silicided I/O buffer with Nwell ballasting technique on the buffer NMOS.

for the I/O buffers to attain the performance target of the IC product, 6kV HBM ESD robustness.

During the ND-mode ESD tests, ESD current is discharged through the power-rail ESD clamp circuit and the forward diode D_N inherent in the buffer NMOS. As a result, the voltage across the V_{DD} and I/O pad is

$$\Delta V_{ND} = I_{ESD} \times (R_{on,Power\text{-}Rail} + R_{VSS} + R_{on,DN}) + V_{t,DN}, \qquad (1)$$

where the $R_{on,Power\text{-}Rail}$ and $R_{on,DN}$ denote the turn-on resistance of power-rail ESD clamp circuit and the diode D_N during ESD stresses, R_{VSS} denotes the effective resistance of the V_{SS} interconnection, and $V_{t,DN}$ denotes the forward voltage drop of the diode D_N. At high I_{ESD} level, i.e. high ESD stress voltage, the ΔV_{ND} can exceed V_{t1} of the buffer PMOS, which in turn induces the parasitic p-n-p bipolar junction transistor (BJT) in the PMOS to be turned on. As a result, part of the ESD current is discharged through the buffer PMOS under high ESD current conditions. Due to the lack of proper ballasting, ESD current discharged through the buffer PMOS is crowded within the shallow surface, which further deteriorates the ESD robustness of buffer PMOS.

SEM image of the I/O buffer after 4.5kV ND-mode ESD stress is shown in Fig. 7. Current traces from source of buffer PMOS toward its drain regions are observed, which confirms that breakdown of the un-ballasted buffer PMOS is the limitation to ESD robustness of I/O buffer with Nwell ballasting technique. Failure spots are found within more than one of the PMOS fingers because PMOS devices barely exhibit snapback phenomenon in deep-submicron CMOS technologies [9].

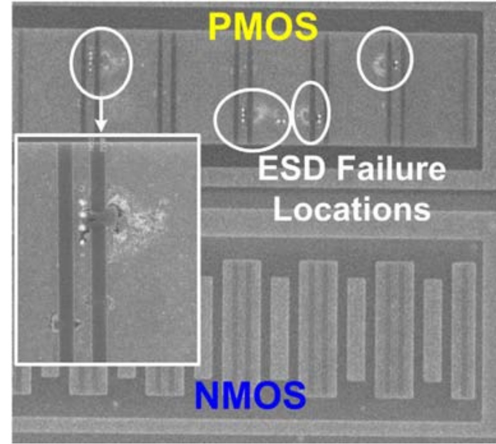
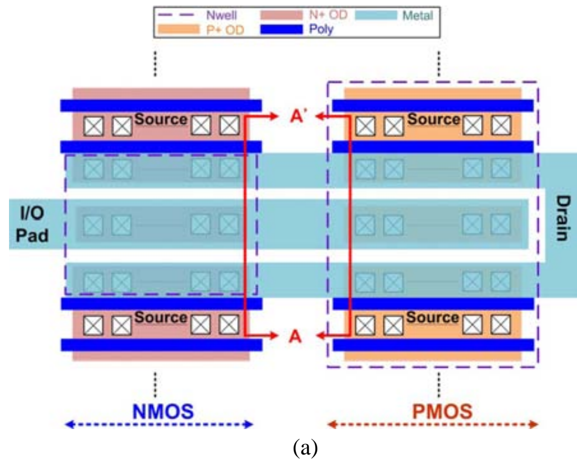


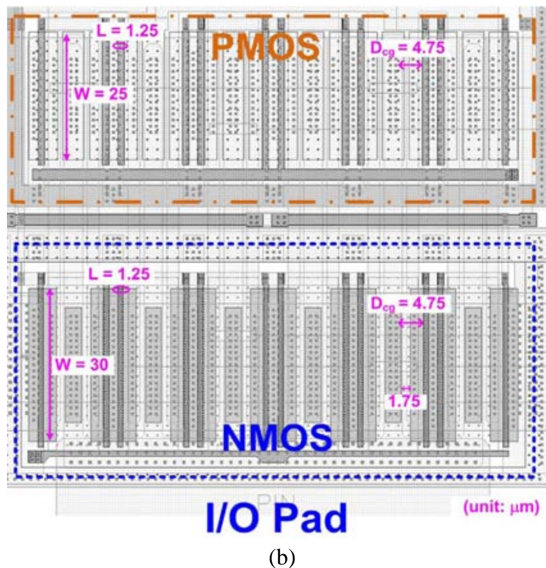
Figure 7: SEM image of the fully-silicided I/O buffer with Nwell ballasting technique on the buffer NMOS after 4.5kV ND-mode ESD stress.

V. I/O Buffer with the New Proposed Layout Scheme

Though the Nwell ballasting technique prevents PS-mode ESD failure on the buffer NMOS and increases the whole-chip ESD protection level from 1.5kV to 4kV, it still cannot achieve the adequate performance target of 6kV HBM ESD robustness. From the ESD measurement and FA results, ballasting technique on the buffer PMOS is vital to the improvement of ESD robustness on fully-silicided I/O buffers. To provide efficient ballast on both NMOS and PMOS devices in the I/O buffer, Fig. 8(a) shows the illustration of the new proposed layout scheme. Drain of the buffer PMOS is separated into drain diffusion and island diffusion by FOX. Drain diffusions of buffer PMOS and NMOS are connected to each other, and island diffusions of both buffer PMOS and NMOS are directly connected to the I/O pad.



(a)



(b)

Figure 8: (a) Illustration of the metal connection to the I/O pad for buffer NMOS and PMOS in the new proposed layout scheme. (b) Layout top view of fully-silicided I/O buffer realized with the new proposed layout scheme.

The layout of I/O buffers with the new proposed layout scheme is shown in Fig. 8(b) with the information of device dimensions. The buffer NMOS and PMOS in the new proposed layout scheme have the same device dimensions as those in the I/O buffers with Nwell ballasting technique on buffer NMOS in Fig. 6(b). The main ESD protection NMOS of the power-rail ESD clamp circuit was also Nwell ballasted. Device cross-sectional view along A-A' line of Fig. 8(a) is shown in Fig. 9. During normal circuit operating conditions, with the shorted drain diffusions of buffer NMOS and PMOS, PMOS can pull high the I/O pad through the ballast Nwell in the buffer NMOS.

Under the ND-mode ESD tests, though the ΔV_{ND} can exceed V_{t1} of the buffer PMOS under high ESD stress voltage, the Nwell ballast resistor suppresses the

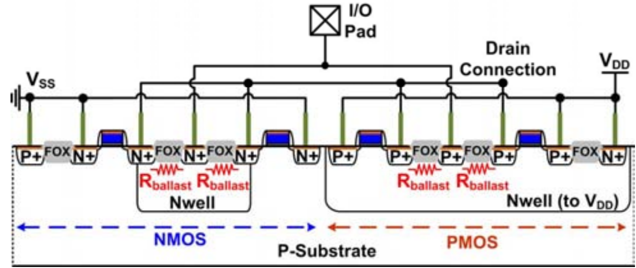
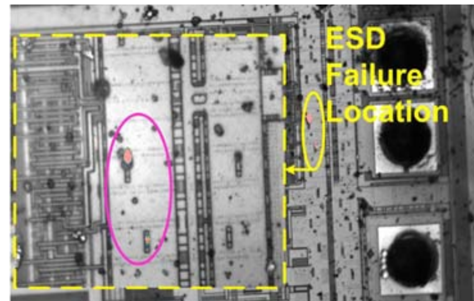
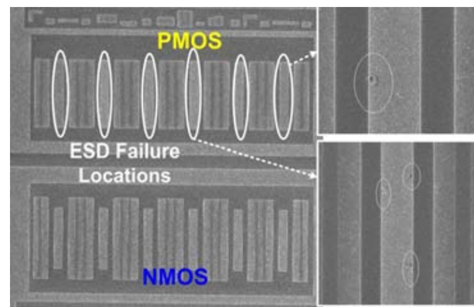


Figure 9: Cross-sectional view along A-A' line of the fully-silicided I/O buffer realized with the new proposed layout scheme.



(a)



(b)

Figure 10: (a) EMMI, and (b) SEM, images of the fully-silicided I/O buffer realized with the new proposed layout scheme after 7.5kV PS-mode ESD stress.

ESD current discharged through the PMOS. Accordingly, with the ballast Nwell on buffer NMOS to enhance the ESD robustness of buffer NMOS, and with the ballast Nwell on buffer PMOS to avoid ND-mode ESD failure on buffer PMOS, positive I/O-to-V_{DD} (PD-), negative I/O-to-V_{SS} (NS-), and ND- modes ESD robustness of the fully-silicided I/O buffers with the new proposed layout scheme are higher than 7.5kV. I/O buffers with the new proposed layout scheme failed under 7.5kV PS-mode ESD test.

Emission microscope (EMMI) analysis of the I/O buffer with new proposed layout scheme after 7.5kV PS-mode ESD stress is shown in Fig. 10(a), where failure locations are found on the buffer PMOS. The corresponding SEM image of the failure on buffer PMOS in Fig. 10(a) is shown in Fig. 10(b). Without the ESD damage on source but silicides meltdown on island diffusions, SEM image reveals the PS-mode ESD failure on the P+/Nwell diode (D_P) of buffer

PMOS, which has further confirmed that the new proposed layout scheme has taken advantage of the highest whole-chip ESD protection capability from the I/O buffers. ESD protection levels of the I/O buffers without ballasting, with Nwell ballasting on NMOS, and with the new proposed layout scheme are summarized in Table I.

Table I: ESD Robustness Among The I/O Buffers Studied in This Work

HBM ESD Robustness (unit: kV)	I/O-to-V_{DD}		I/O-to-V_{SS}		V_{DD}-to-V_{SS}
	(+) PD-mode	(–) ND-mode	(+) PS-mode	(–) NS-mode	
Fully-Silicided I/O Buffer without Ballasting	> 2	> 2	1.5	> 2	> ±2
I/O Buffer with Nwell Ballasting on NMOS	> 4.5	4	> 4.5	> 4.5	> ±4.5
I/O Buffer with the New Proposed Layout Scheme (This Work)	> 7.5	> 7.5	7	> 7.5	> ±7.5

VI. Conclusion

Silicidation used in CMOS processes has been reported to cause substantial degradation on ESD robustness of CMOS devices. To mitigate the negative impact on ESD robustness from silicidation, a new ballasting layout scheme for fully-silicided I/O buffers is proposed in this work. The new proposed ballasting layout scheme has been verified on a real IC product fabricated in a 0.35-μm fully-silicided CMOS process. Without adequate ballasting technique in the original layout, the fully-silicided I/O buffer has a very poor ESD level of 1.5kV in HBM ESD tests. With the new proposed layout scheme, the whole-chip ESD protection level has been improved to 7kV HBM ESD robustness. No additional mask or process step are required to fulfill the new proposed layout scheme. The new proposed ballasting layout scheme is portable to different technologies, so that the additional mask and process steps for silicide blocking can be saved to reduce the fabrication cost without sacrificing the ESD robustness of IC products.

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