

# Novel Multi-layer Wiring Build-up using Electrochemical Pattern Replication (ECPR)

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## Abstract

This paper discloses a novel, high accuracy and low cost integration method based on an Electrochemical Pattern Replication (ECPR) technology for multi-level stacking applications such as integrated passives, multi-level redistribution layers and top level IC interconnect structures.

It is demonstrated how a first copper layer is coated with BCB (Bisbenzocyclobutene), which is planarized with CMP (Chemical Mechanical Polishing) to uncover the first layer, where after a second patterned copper layer is fabricated with ECPR. This approach shows the feasibility of fabricating highly accurate multi-level wiring layers and still avoiding the issues related to increasing topography, which are particularly severe for thick metal layers. In addition, the constraints for the dielectric material is significantly reduced, since it does not have to be photosensitive or planarizing, which in turn opens up for the use of alternative dielectric materials, which may have better electrical and physical properties, that have not been usable with the traditional multi-level fabrication methods.

## Introduction

The integration of more and more complex functions such as wireless communication capabilities on chips or packages puts new demands on the manufacturing methods for top metal layers. High density interconnects and integrated passives require a combination of resolution, accuracy, thickness uniformity typically offered only by dual damascene processes. At the same time there is a need for thicker metal, high deposition rates and low cost per layer, which is typically offered only by through mask plating processes. These combined requirements are difficult to address by most existing methods of today.

The increasing demand for further miniaturization and functionality for electronic systems, particularly for mobile and wireless applications, has been driving the trend of fabricating multi-layer wiring, such as integrated passives and redistribution layers for Wafer Level Packaging (WLP) applications [1]. By utilizing multi-layer build-up, increased functionally is achieved, without drastic increase in chip-size.

Particular for above-IC integrated passives and Integrated passive devices (IPDs) there has been a trend of fabricating thicker metal (copper circuits) since it lowers the series resistance of the devices, which in turn results in better performance (e.g higher capacitance or inductance value per area) [2]. However, the maximum copper thickness used in multi-layer applications is limited both by the aspect ratio capabilities of today's lithography processes and by the increasing topography for each wiring layer.

High topography from the previous layers increases variation on linewidth, space and thickness for the top layer. The electrical behavior of integrated passive devices are highly effected by the dimensions of the wiring layers; and increased variation, due to underlying topography, may significantly reduce performance [3]. The dielectric constant of the insulating material separating multiple stacked wiring layers can also have a strong effect on parasitic capacitive loss to the ground plane [3].

BCB is a commercially dielectric material developed by the Dow Chemical Company (Midland, MI, USA) and is commonly used in above-IC multi-layer applications. The material has a low dielectric constant and high degree of planarization (DOP) properties. But the cured BCB is mechanically less stable than most of the polyimides. A comparison is given in table 1.

	<b>BCB 4000</b>	<b>DURIMIDE 7510</b>	<b>HD 4100</b>	<b>HD 8820</b>
<b>Polymer</b>	BCB	Polyimide	Polyimide	PBO
<b>Formulation</b>	DOW Chemicals	Fujifilm	HD Micro.	HD Micro.
<b>Manufacturer</b>	Negative	Negative	Negative	Positive
<b>Tone</b>	2,65	3,2-3,3	3,36	2,94
<b>Dielectric constant 1 Mhz</b>	0.0008 - .002	.003-.008	0,001	0,0089
<b>Dissipation factor</b>	550 V/μm	345 V/μm	250 V/μm	470 kV/mm
<b>Breakdown voltage MV/cm</b>	1 · 10 <sup>19</sup>		2,40E+16	3,40E+16
<b>Volume resistivity (Vcm)</b>	<0.2%	1.08 @50%RH	1% (50%RH)	<0.5%
<b>Water absorption</b>	28 +- 2 MPa	33	34	37
<b>Residual stress on Si (MPa)</b>	87 +- 9	215	200	168
<b>Tensile strength (MPa)</b>	8	85	45	87
<b>Elongation %</b>	2,9	2,5	3,5	2
<b>Elastic modulus (GPa)</b>	< 5%			
<b>Curing Shrinkage</b>	42	55		
<b>Thermal expansion coefficient (ppm/°C)</b>			35	67
<b>Decomposition (C)</b>	> 350°C	525	600	
<b>Glass transition temp (C)</b>		285		299

Table 1. Comparison of thin film polymers (selection) used for WLP and IPD [16].

Stress-related cracking has been observed in mechanically and thermally shocked BCB films. [4]

The planarization properties of BCB have been studied extensively prior to this study. The DOP depends highly on the thickness and pitch of the underlying metal and the thickness of the BCB film. The degree of planarization will also vary depending on the wiring layout, from zero DOP over large isolated lines to >90% DOP for smaller lines in areas with high pattern density. [4, 5, 13]

Polyimide is widely used in microelectronic packaging applications. It is more reliable in applications where temperature changes/cycling can induce failures [4].

In fabrication of RDL (redistribution layers), commonly used in WLCSP (wafer level chip scale package) applications, good reliability in drop tests has been demonstrated with polyimide [14]. Drop test is the one of the most popular testing method for evaluating the shock response of electronic components or portable electronic devices, such as mobile phones or notebook computers [15]. But due to significantly lower degree of planarization properties of polyimide compared to BCB, which has been demonstrated in previous works [5], it is more suitable for single layer applications while BCB is widely used for multi-layer wiring. Also, the dielectric constant of polyimide is significantly higher and it therefore less used in integrated passive devices such as RF applications [4].

With the fabrication process used today, the dielectric material must have a sufficiently low dielectric constant, enough degree of planarization, required mechanical properties and at the same time being photosensitive for lithographic patterning.

In this paper a novel integration scheme is demonstrated using an Electrochemical Pattern Replication (ECPR) method which enables fabrication of a multiple layer of thick copper build-up without increasing topography. In addition the ECPR based process flow does not require lithographical patterning of the dielectric layer, which reduces the constraints of the dielectric materials.

### The ECPR principle

A new approach called Electrochemical Pattern Replication (ECPR) technology has been developed that combines the precision and resolution of advanced lithography with the efficiency of electrochemical deposition into one single electrochemical metal printing step [6]. ECPR offers a unique combination of resolution, dimensional accuracy, high deposition rates and low cost per layer, bridging the gap between front- and back-end metallization [7].

In the ECPR process, a template (master electrode), consisting of an electrically conducting electrode layer and a patterned layer of electrically insulating material is used. The master is firstly pre-filled with an anode material, such as copper, in the cavities of the insulating structures. During the print-step the master is put in contact with a seed layer coated substrate with an electrolyte applied between the two surfaces (figure 1a).

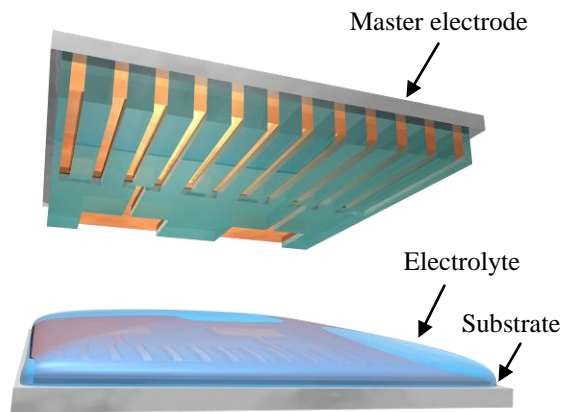


Figure 1a. Master, pre-filled with anode material, substrate with seed layer and electrolyte.

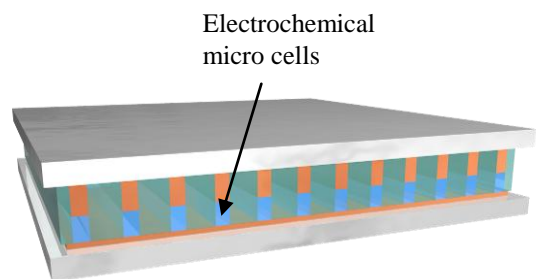


Figure 1b. Master and substrate in contact forming electrochemical micro cells.

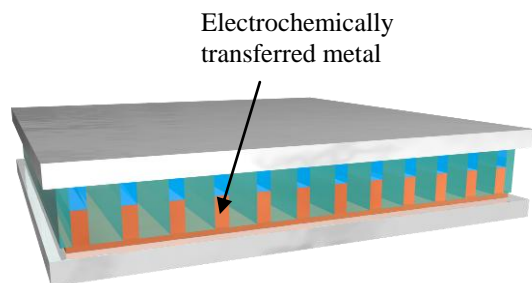


Figure 1c. Electrochemical metal transfer in micro cells.

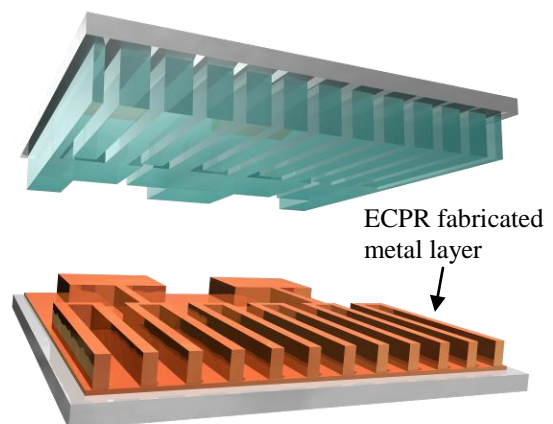


Figure 1d. Master and substrate with Electrochemical Pattern Replication (ECPR) fabricated metal layer.

When put in contact, excessive electrolyte is forced away from the master electrode and substrate interface. Local electrochemical micro cells, filled with electrolyte, are formed in the cavities defined by the pattern of the master electrode (figure 1b).

Next an external potential is applied, over the master electrode and substrate surfaces, and electrochemical material transfer takes place inside each local micro cell. Metal is dissolved into ions from the pre-filled anode material in the master and transported through the electrolyte in each micro cell and deposited on the cathodic seed layer (figure 1c).

After separation, an inverse metal replica of the master electrode pattern has been produced on the substrate (figure 1d), which will go through seed layer etch thereafter (not shown). Subsequently the master is pre-filled again, and the steps are repeated over and over for producing new replicas from the master.

The ECPR technology offers a single integrated solution, including the tool, processes and master electrode, thereby reducing overall complexity in the manufacturing flow. By removing process steps, and associated wafer transfer between multiple tools, the total cycle time to manufacture a metal layer can be reduced significantly. Comparing the ECPR flow to a conventional through-mask plating line, one single ECPR tool replaces the six tools used for resist coating, exposure, development, descum, electroplating and resist strip [7].

A unique feature of ECPR is the ability to achieve a uniform plating height, independent of the pattern density. ECPR has the advantage of maintaining a 1:1 anode-to-cathode area ratio in all of the electrochemical micro cells, formed by the cavities between the master and the substrate. In a conventional through mask plating process, local spots with low active pattern density will receive a higher current density than areas with high active pattern density due to the nature of electrolytic current distribution, known as current crowding. This results in varying deposition rates in different areas and uneven within-die thickness distribution of the plated metal [8, 9]. The problem is normally addressed by reducing the plating speed and adding organic additives to the electrolyte. Additional dummy patterns may be added to the design and repeated process optimization is typically needed when implementing new designs.

Despite these efforts, non uniform material distribution is always a problem associated with conventional electroplating processes, with various effects depending on the pattern layout, limiting the designs that can be produced and the throughput of the plating step.

The resolution of the ECPR fabricated metal pattern is determined by the geometries patterned master electrode (master) [10]. In turn, the master can be produced with a highly accurate lithography and patterning method which allows for close to vertical sidewalls, with high aspect ratio and minimum linewidth variation. Figure 2 shows a SEM image of a cross section of the master structures. When using ECPR, the metal pattern profile is no longer limited by the capabilities of the (thick) photoresist traditionally used as a mask for plating. Figure 3a and 3b show SEM images of

ECPR plated structures with 10 $\mu$ m thickness and down to 5 $\mu$ m space, with vertical side walls.

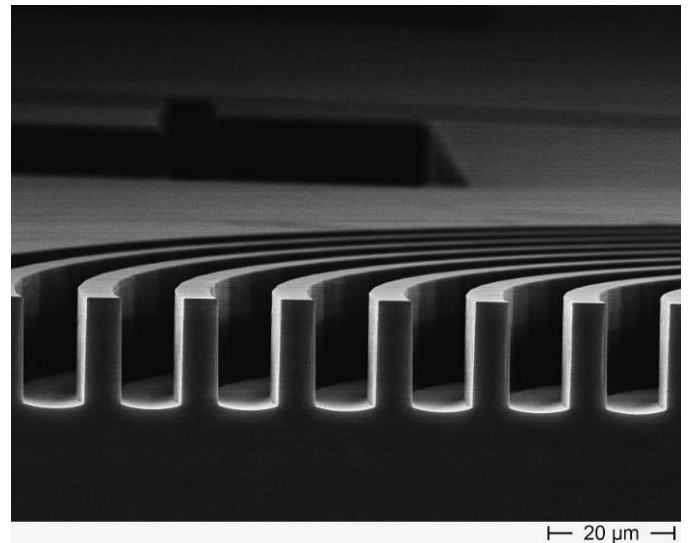


Figure 2. Cross section SEM image of a master electrode.

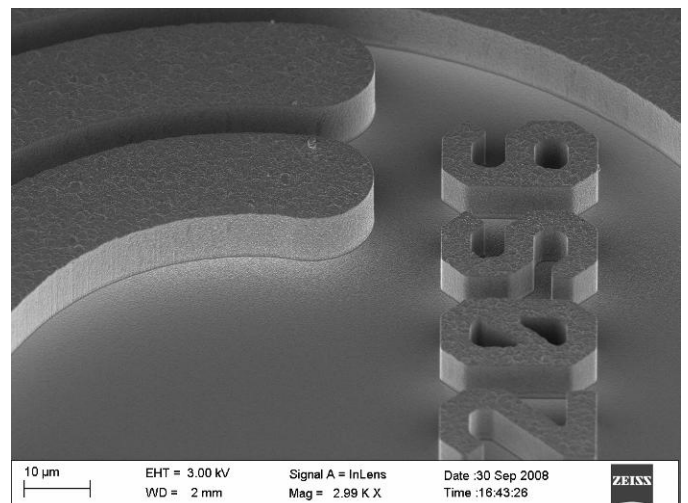


Figure 3a. SEM image of ECPR fabricated copper structures.

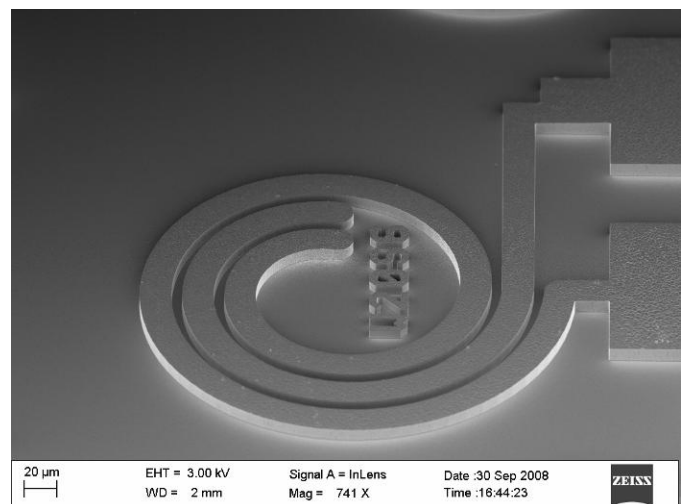


Figure 3b. SEM image of ECPR fabricated copper structures.

The combination of well defined sidewall profiles, minimal linewidth variation and highly accurate thickness uniformity, resulting from the micro cell plating principle, enable excellent control of the cross section of the fabricated patterns.

### Multi-layer wiring build-up with ECPR

The ECPR print method is a metal-first approach that enables integration of dielectric layers and metal patterns in multiple layers without the use of lithography or regular plating. Schematically, the multi-layer stack can be formed by repeating the following sequence (illustrated in figure 4):

1. ECPR printing of a via layer
2. Dielectric layer application & planarization
  - a. Coating with a dielectric material, completely covering the first via layer
  - b. CMP of dielectric layer until the top of the first via layer is uncovered
3. ECPR printing of a wire layer and a second via layer
4. Dielectric layer application & planarization
5. ECPR printing of a second wire layer and third via layer
6. Dielectric layer application & planarization

The process flow may be slightly modified depending on the application. For instance, one application is to create redistribution layers or integrated passives post the passivation layer on an IC substrate. Vias in the passivation layer are already provided to the underlying top interconnect metal pads. And, if there is no requirement for another dielectric layer such as polyimide or BCB, the ECPR multi-layer process flow starts on step 3, i.e. direct ECPR printing of a wiring layer connecting to the underlying interconnect layer through the vias in passivation layer. This process flow is illustrated in figure 5.

### Results

A first proof of concept of the ECPR multi-layer process flow has been demonstrated in this study by fabricating samples with two layers of copper integrated with a BCB dielectric layer on 200mm silicon wafers. A first layer of copper was produced by electroplating a typical redistribution layer (RDL) with 3  $\mu\text{m}$  thickness. The linewidth and space of the first layer features varied from 10 $\mu\text{m}$  to >100 $\mu\text{m}$ . The first copper layer was coated with BCB (Cyclotene 4024-40, commercially available from The Dow Chemical Company), with a thickness of 4.5 $\mu\text{m}$  after cure, completely covering the first copper layer. Subsequently, the BCB layer was planarized using a polymer CMP process (developed by Fraunhofer IZM, Berlin), based on the Rodel XSHD 3568D chemistry. The CMP process was stopped when the top of the first metal layer was completely uncovered.

Next a seed layer stack, of 20nm TiW and 100nm Cu, was deposited by DC-sputtering onto the planarized layers. On top of the seed layer, a second copper layer was fabricated using Electrochemical Pattern Replication (ECPR). Finally, the seed layer stack was etched, using a wet-etch process, isolating the ECPR fabricated structures in the second copper layer. Figure 6a to 6c show SEM images of the fabricated 2-layer structures made with ECPR.

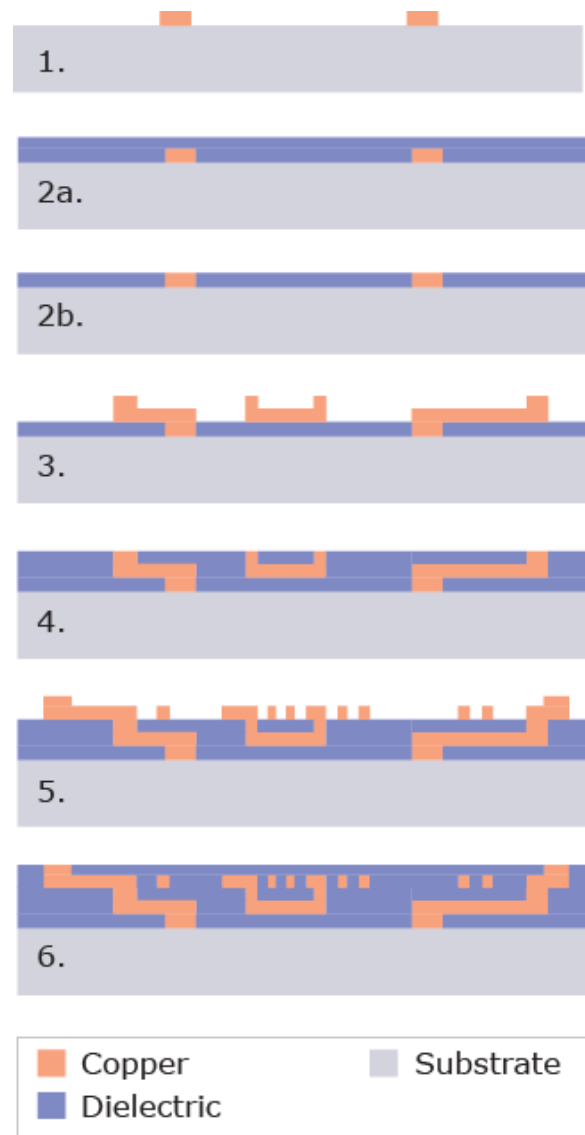


Figure 4. Schematic process flow for multi-layer wiring build-up with ECPR.

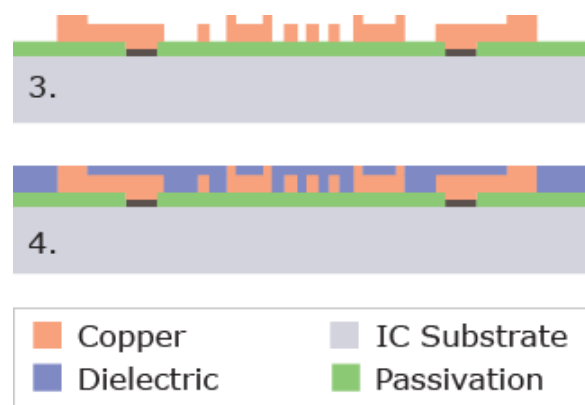


Figure 5. Schematic process flow for multi-layer wiring layer with ECPR when no additional dielectric is required on top of the passivation layer.



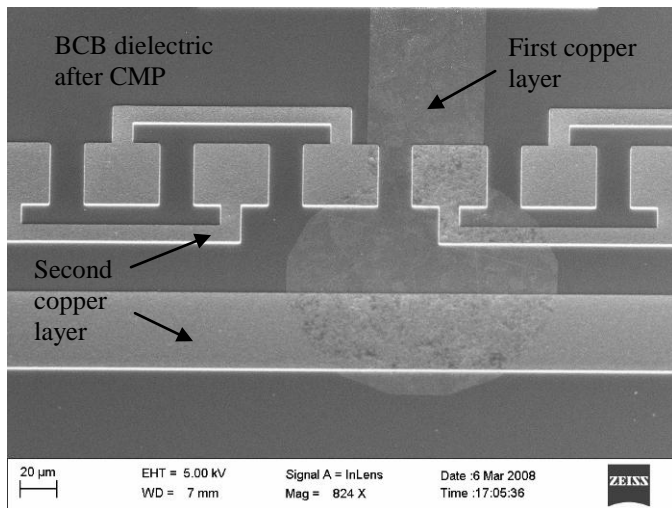


Figure 6a. SEM image of 2-layer stack with ECPR fabricated copper.

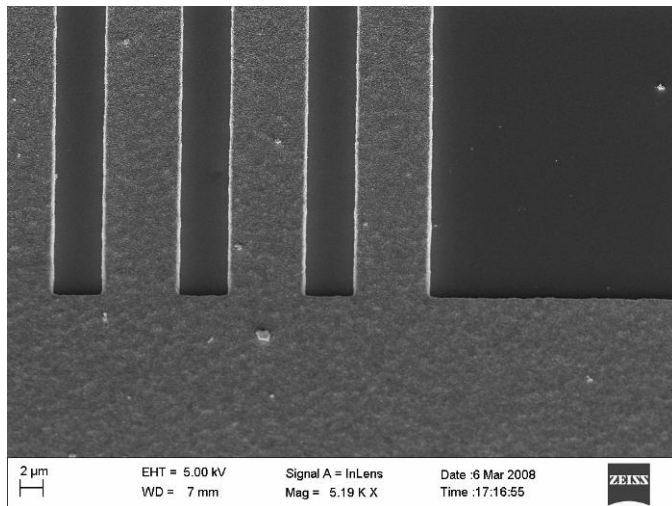


Figure 6b. SEM image of 2-layer stack with ECPR fabricated copper with 6 $\mu$ m lines and 4 $\mu$ m space.

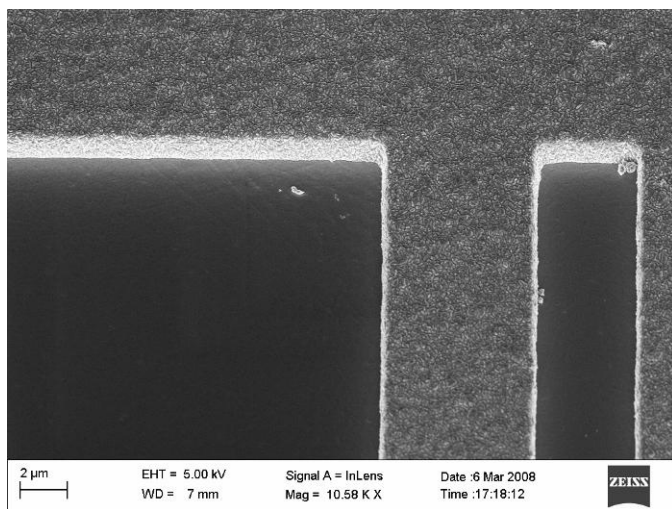


Figure 6c. SEM image close up of 2-layer stack with ECPR fabricated copper with 6 $\mu$ m lines and 4 $\mu$ m space.

The features of the second copper layer have a minimum linewidth of 6 $\mu$ m and 4 $\mu$ m space. The dimension stability of the second metal layer was proven. No change in linewidth or space, induced by the underlying layer, could be measured over the wafer.

### Conclusions

The increasing demand for more advanced electronic systems and miniaturization has driven the development of multi-layer copper wiring applications. At the same time, the trend goes towards fabricating thicker copper features, particularly for integrated passive components used in RF applications.

The thickness used for conventional multi-layer wiring is limited by the increasing topography after each added layer. BCB is commonly used in today's multi-layer wiring since it has high degree of planarization (DOP). To achieve more than 90% DOP the BCB thickness needs to be between 1.5 and 3 times the thickness of the metal layer [5]. To be able to create multi-wiring with significantly thicker copper than used today, for instance 10 $\mu$ m, this would require a BCB layer thickness of about 15 to 30 $\mu$ m. Even with 90% DOP, the remaining height difference in the dielectric will then be 1 $\mu$ m (10% of the metal thickness). In addition, the DOP will vary across the chip depending on the linewidth and space. The remaining step may be significantly higher than 1 $\mu$ m in areas with large spaces between the wiring structures. The topography will add on for each subsequent wiring layer, making it hard to achieve the uniformity required for advanced applications such as integrated passives.

Patterning such a thick BCB with lithography may also become challenging, especially when small vias (such as 10 $\mu$ m or less) are required. One solution may be to dry-etch the dielectric instead of using photo-BCB. However, this is a more expensive process which requires an extra resist patterning step and a reactive-ion dry-etch step. Due to the issues related to increasing topography, two or more layer build-up applications, such as IPDs, typically only have a metal wiring thickness up to 3-5 $\mu$ m with exception of the top layer, which may be thicker [1, 11].

The presented multi-layer wiring build-up process based on ECPR does not suffer from the limitations of increasing topography for each layer. By utilizing the ECPR metal-first and dielectric CMP approach, the underlying metal layer do not contribute to any significant increase in topography for the subsequent wiring layer, independently of the copper thickness, linewidth and spaces. This enables fabrication of (thick) multi-layer wiring, with a large number of metal stacks traditionally only being done with front-end dual damascene processing of IC interconnects.

Of course, the metal first approach may be done with regular through mask plating. But with regular plating, the challenges of varying thickness uniformity, related to within-die (WID) pattern density and feature size variation, would still remain. The advantage with the high WID thickness uniformity achievable with ECPR relates to the subsequent CMP process. If the copper thickness within-die non-uniformity (WIDNU) is high, the CMP process requires continued polishing of the metal features, in areas where the

copper is firstly uncovered, and at the same time as polishing the dielectric in other areas. The difference in CMP rate in those areas can result in dishing and erosion, similar to the challenged reported for varying CMP rates in different pattern density areas [12], which in turn can cause unwanted topography.

At the same time, compared to through mask plating (or dual damascene processes), the ECPR flow is a cost efficient solution, since lithography and plating is completely replaced by ECPR patterning and dielectric photolithography is replaced by dielectric CMP.

As mentioned, the BCB material has good dielectric properties, useful for RF-applications, but also suffers from temperature and mechanical induced failures. With the presented ECPR multi-layer wiring approach, constraints for the dielectric material is significantly reduced, since it does not have to be photosensitive or have a high DOP. It opens up for new possibilities of using alternative dielectric materials which may have better electrical properties and at the same time having more chemically and mechanically stable properties than the dielectric films used in traditional multi-level fabrication processes.

In this study, a first proof of concept of a novel multi-layer wiring process based on ECPR has been shown. Future work may include demonstrating the build-up with a larger number of wiring and via layers of thick copper integrated with various dielectric materials and studying its electrical and physical properties.

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