ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 5, May 2015

An Efficient Power Reduction in Multiplexer Based On Cordic Using Cadence-Digital IC Design

Uma.P, G.AnuVidhya

ME Student, Dept. of VLSI Design, Karpaga Vinayaga college of Engineering and Technology, Madurantakam, India

Assistant Professor, Dept. of ECE, Karpaga Vinayaga college of Engineering and Technology, Madurantakam, India

ABSTRACT: CORDIC is an iterative Algorithm to perform a wide range of functions including vector rotations, certain trigonometric, hyperbolic, linear and logarithmic functions. Both non pipelined and 2 level pipelined CORDIC with 8 stages, using two schemes was performed. First scheme was original unrolled CORDIC and second scheme was MUX based pipelined unrolled CORDIC. Compared to first scheme, the second scheme is more reliable, since the second scheme uses multiplexer and registers. By adding multiplexer the area is reduced comparatively to the first architecture, since the first scheme uses only addition, subtraction and shifting operation in all the 8 stages.8 iterations are performed and it is implemented on QUARTUS II software. The same is implemented in cadence tool and the results was compared with QUARTUS II and CADENCE TOOL. An efficient power reduction is obtained in CADENCE (Digital) implementation.

KEYWORDS: CORDIC, rotation mode, multiplexer, pipelining, QUARTUS II, CADENCE (Digital) implementation.

I INTRODUCTION

The CORDIC is a class of hardware-efficient algorithms for the computation of trigonometric and other transcendental functions that use only shifts and adds to perform. The CORDIC set of algorithms for the computation of trigonometric functions was developed by Jack E. Volder in 1959 to help in building a real-time navigational system for the B-58 supersonic bomber. Later, J. Walther in 1971 extended the CORDIC scheme to other transcendental functions.

Calculators can only perform four operations inexpensively:

1. Addition and Subtraction
2. Storing in memory and Retrieving from memory
3. Digit shift (multiplication/division by the base)
4. Comparisons

The CORDIC Algorithm is a unified computational scheme to perform

1. Computations of the trigonometric functions: sin, cos and arctan.
2. Computations of the hyperbolic trigonometric functions: sinh, cosh and arctanh.
3. It also compute the exponential function, the natural logarithm and the square root.
4. Multiplication and division.

Both non pipelined and 2 level pipelined CORDIC with 8 stages and using two schemes was done. First scheme using adders in all the stages and second scheme using multiplexers only in the second and third stages, the other stages are as same as first scheme.

The second scheme achieves less area compared to original unrolled CORDIC (first scheme). It is performed in QUARTUS II. Multiplexer has been proposed for the ASIC implementation of unrolled CORDIC (Coordinate Rotation Digital Computer) processor

The CORDIC algorithm is an iterative method of performing vector rotations by arbitrary angles using shifts and addition. In the rotation mode, CORDIC may be used for converting a vector in polar form to rectangular form. In

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 5, May 2015

the vector mode, it converts a vector in rectangular form to polar form. Both the modes are derived from the general rotation transform.

$$X_{fin} = X_{in} \cos\theta - Y_{in} \sin\theta \quad (1)$$
$$Y_{fin} = X_{in} \sin\theta + Y_{in} \cos\theta \quad (2)$$

The rotation may be achieved by performing a series of successively smaller elementaryrotations$\theta_1,\theta_2,\theta_3\ldots.\theta_N$. Rotation of the vector by an angle can be rewritten as

$$X_{i+1}=X_i \cos\theta\, i - Y_i \sin\theta \mathrm{i} \quad (3)$$
$$Y_{i+1}=X_i \sin\theta \mathrm{i} + Y_i \cos\theta \mathrm{i} \quad (4)$$
$$X_{i+1}/\cos\theta \mathrm{i} = X_i - Y_i \tan\theta \mathrm{\ i} \quad (5)$$
$$Y_{i+1}/\cos\theta \mathrm{i} = Y_i + X_i \tan\theta \mathrm{i} \quad (6)$$

The computational complexity of (5), (6) can be reduced by rewriting these equations as

$$X_{i+1}=X_i - Y_i \tan\theta \mathrm{i} \quad (7)$$
$$Y_{i+1}=Y_i + X_i \tan\theta \mathrm{i} \quad (8)$$
$$(X_{fin}, Y_{fin}) = (x_N/\pi_0^N \cos\theta \mathrm{i}, y_N/\pi_0^N \cos\theta \mathrm{i}) \quad (9)$$
$$Z_{i+1}=Z_i - \theta_i \quad (10)$$

θ_i is considered to be positive when the rotation required is anticlockwise and is negative otherwise. The direction of this rotation depends on the δi.

$$\delta_i = sgn(Z_i) \quad (11)$$

II. RELATED WORK

In rotation mode, CORDIC can simultaneously compute the sine and cosine of the input angles. In this mode, set the y component of the input vector to zero, x component to 1/k and the angle accumulator is initialized with the desired rotation angle θ. For rotation mode, the CORDIC equations are given by

$$X_{i+1}=X_i - Y_i.\delta_i.2^{-i} \quad (12)$$
$$Y_{i+1}=Y_i + X_i.\delta_i.2^{-i} \quad (13)$$
$$Z_{i+1}=Z_i - \delta_i.\tan^{-1} 2^{-i} \quad (14)$$
$$k = \prod_0^N cos\theta_i \quad (15)$$

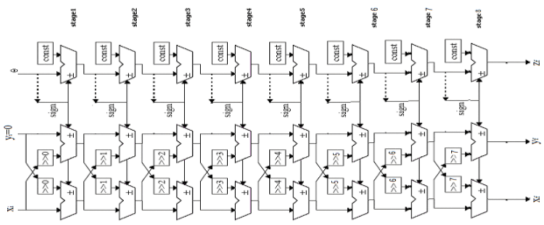


Fig1. The Unrolled CORDIC

The architecture of the eight stage unrolled CORDIC is shown , this consists of only adders,subtractors and shifters; accuracy improves as the number of stages increases. Addition or subtraction on the angle value takes place in each rotation of the vector depending on the most significant bit of previous angle. Perform division just by doing right shift using shift registers.

The scheme for reducing the area of the CORDIC using multiplexer is proposed for the ASIC implementation. This is adopted for the QUARTUS II based implementation . The area is reduced by removing some of the stages .

$$Y_1=X_i \quad (16)$$
$$X_1=X_i \quad (17)$$

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 5, May 2015

If the first stage output is positive, then

$$Y_2 = Y_1 - \frac{x1}{2} = \frac{xi}{2} \quad (18)$$
$$X_2 = X_1 + \frac{y1}{2} = 3Xxi/2 \quad (19)$$

The vector coordinates corresponding to negative output is

$$Y_2 = Y_1 + \frac{x1}{2} = 3Xxi/2 \quad (20)$$
$$X_2 = X_1 - \frac{y1}{2} = \frac{xi}{2} \quad (21)$$

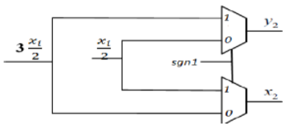


Fig 2. Mux Based CORDIC

The block diagram of the CORDIC when the adders till third stage are replaced with Mux is shown . As the adders are replaced with Mux, the area of the circuit is reduced till 3rd stage. But the replacement of adders with Mux beyond the third stage results in an exponential increase in the number of Mux as shown in Table I.

$$Y_3 = Y_2 + \frac{X2}{4} = \frac{3Xxi}{2} + \frac{xi}{8} = \frac{13Xxi}{8} \quad (22)$$
$$X_3 = X_2 - \frac{Y2}{4} = \frac{xi}{2} - \frac{3Xxi}{8} = \frac{xi}{8} \quad (23)$$

For $sgn_1 = 0, sgn_2 = 0$

$$Y_3 = Y_2 + \frac{x2}{2} = \frac{xi}{2} + \frac{3Xxi}{8} = \frac{7Xxi}{8} \quad (24)$$
$$X_3 = X_2 - \frac{y2}{4} = \frac{3Xxi}{2} - \frac{xi}{8} = \frac{11Xxi}{8} \quad (25)$$

For $sgn_1 = 1, sgn_2 = 0$

$$Y_3 = Y_2 - \frac{x2}{4} = \frac{3Xxi}{2} - \frac{xi}{8} = \frac{11Xxi}{8} \quad (26)$$
$$X_3 = X_2 + \frac{y2}{4} = \frac{xi}{2} + \frac{3Xxi}{8} = \frac{7Xxi}{8} \quad (27)$$

For $sgn_1 = 0, sgn_2 = 1$

$$Y_3 = Y_2 - \frac{x2}{4} = \frac{xi}{2} - \frac{3Xxi}{8} = \frac{xi}{8} \quad (28)$$
$$X_3 = X_2 + \frac{y2}{4} = \frac{3Xxi}{2} + \frac{xi}{8} = \frac{13Xxi}{8} \quad (29)$$

For $sgn_1 = 1, sgn_2 = 1$

No. of eliminated stages	No. of Mux Required
1	0
2	2
3	6
4	14
5	30

Table1. Multiplexers required for eliminating different stages

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 5, May 2015

III. PROPOSED ALGORITHM

The pipelined CORDIC use registers in between each iteration stage as shown.The advantage of pipelined unrolled CORDIC over the unrolled CORDIC is its higher frequency of operation. This property can be used in high speed applications. The number of registers depends on the number of stages in pipelining and there will be an increase in area. The first output of an N-stage pipelined CORDIC core is obtained after N clock cycles. Thereafter, outputs will be generated during every clock cycle. Here, pipelined registers are placed after fourth and seventh stages. Mux based pipeline unrolled CORDIC architecture in which pipeline registers are inserted at the output.

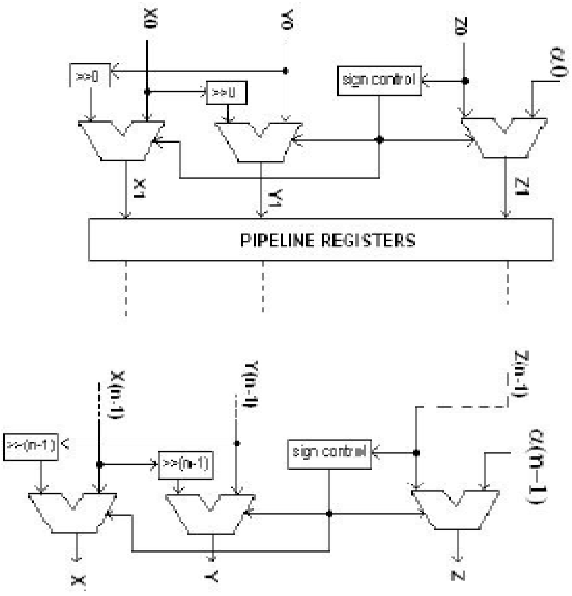


Fig 3. Pipelined CORDIC Using Registers

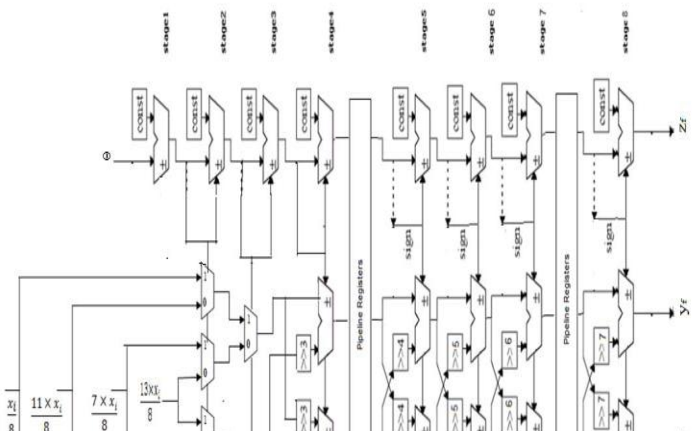


Fig 4. Pipelined MUX Based Unrolled CORDIC

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 5, May 2015

IV. SIMULATION RESULTS

A.THE RESULTS IN QUARTUS II FOR THE ORIGINAL UNROLLED CORDIC

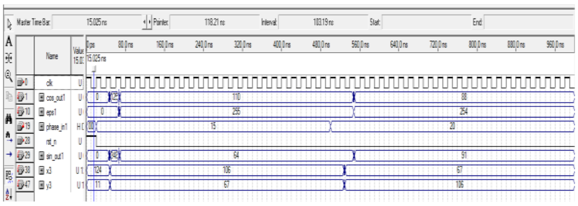


Fig 5.The Original Unrolled CORDIC Output Waveform

Phase_in1, rst_n and clk are the inputs assigned to the block diagram. Cos_out1 , sin_out1 and eps1 are the outputs obtained. For different angle value the corresponding sin and cos values are calculated. For 30˚ corresponding hexadecimal value is 15 and output obtained for sin_out1 is 64 and cos_out 1 is 255.For 45˚ corresponding value is 20 and output obtained for sin_out1 is 51 and cos_out1 is 254

INPUT ANGLE VALUE	INPUT CALCULATED VALUE	OUTPUT SIN_out1 VALUE	OUTPUT COS_out1 VALUE
30˚	15	64	255
45˚	20	51	254

Table 2. Output Waveform Calculation

B. POWER ANALYZER

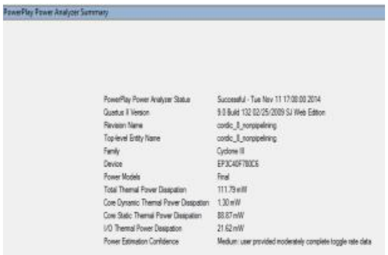


Fig 6. Power Analyzer Report

Power analyzer report says the total power thermal dissipation, core dynamic thermal power dissipation, core static thermal power dissipation and input /output power dissipation. From thisreport the static and dynamic power rate and also input/output power rate are analysed.

C.RESULTS IN QUARTUS II FOR PIPELINED MUX BASED UNROLLED CORDIC

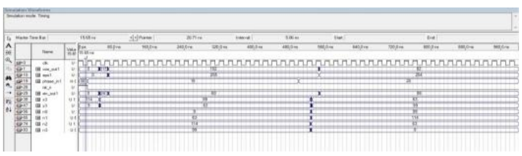


Fig 7. Output Waveform of Pipelined MUX Based Unrolled Cordic

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 5, May 2015

Phase_in1, rst_n and clk are the inputs assigned to the block diagram. Cos_out1 , sin_out1 and eps1 are the outputs obtained. For 30° corresponding hexadecimal value is 15 and output obtained for sin_out1 is 247 and cos_out 1 is 115 .For 45° corresponding value is 20 and output obtained for sin_out1 is 86 and cos_out1 is 82.

INPUT ANGLE VALUE	INPUT MEASURED VALUE	OUTPUT SIN_out1 VALUE	OUTPUT COS_out1 VALUE
30°	15	247	115
45°	20	86	82

Table 3.Output Waveform Calculation

D.POWER ANALYZER

Fig 8.Power Analyzer Report

E.RESULTS IN CADENCE TOOL FOR ORIGINAL UNROLLED CORDIC

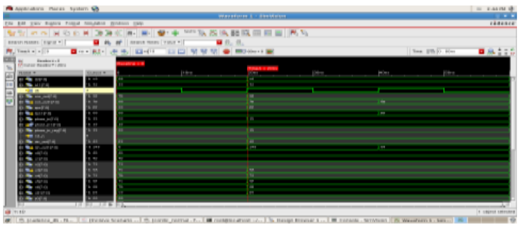
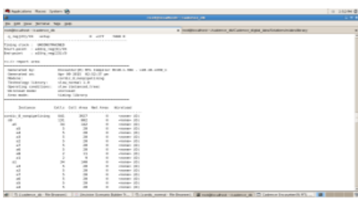


Fig 9. Output Waveform for the Original Unrolled Cordic

Phase_in1, rst_n and clk are the inputs assigned to the block diagram. Cos_out1 ,sin_out1 and eps1 are the outputs obtained. For 30° corresponding hexadecimal value is 15 and output obtained for sin_out1 is 64 and cos_out 1 is 255.For 45°corresponding value is 20 and output obtained for sin_out1 is 51 and cos_out1 is 254.

INPUT		OUTPUT	
ANGLE VALUE	CALCULATED VALUE	SIN_out1 VALUE	COS_out1 VALUE
30°	15	64	255
45°	20	51	254

Table 4.Output Waveform Calculation



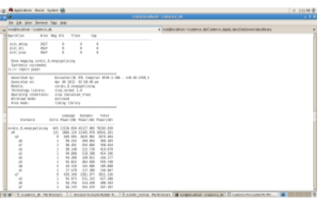


Fig 10Report for AreaFig 11. Report for Power

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 5, May 2015

From fig.10 it is easy to identify the total area consumed by the original unrolled cordic. The area consumed is about 3927.From fig 11.it is possible to identify the leakage power, dynamic power and total power obtained for the original unrolled cordic. The leakage power is 13136.856 nw ,dynamic power is 65127.083 nw and total power is 78263.939 nw.

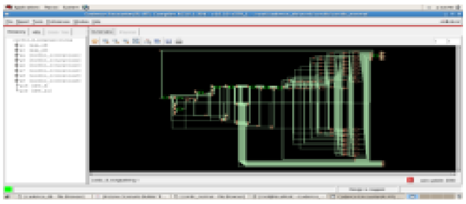


Fig.12Netlist View for the Original Unrolled Cordic

F.RESULTS IN CADENCE TOOL FOR MUX BASED PIPELINED UNROLLED CORDIC

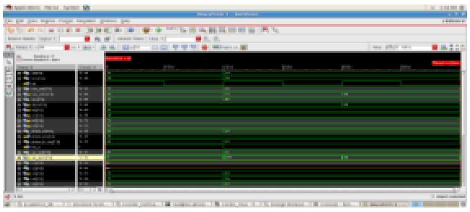


Fig 13. Output Waveform for the Mux based Pipelined Unrolled Cordic

Phase_in1, rst_n and clk are the inputs assigned to the block diagram. Cos_out1 , sin_out1 and eps1 are the outputs obtained. For 30° corresponding hexadecimal value is 15 and output obtained for sin_out1 is 247and cos_out 1 is 115 For45° corresponding value is 20 and output obtained for sin_out1 is 86 and cos_out1 is 82.

INPUT		OUTPUT	
ANGLE VALUE	CALCULATED VALUE	SIN_out1 VALUE	COS_out1 VALUE
30°	15	247	115
45°	20	86	82

Table 5 .Output Waveform Calculation

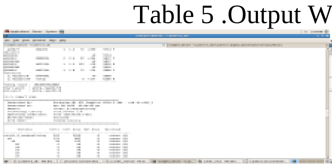



Fig 14. Report for AreaFig15. Report for power

From fig.14it is possible to identify the total area consumed by the Mux based pipelined unrolled cordic. The area consumed is about 3959.From fig.15 it is easy able to identify the leakage power, dynamic power and total power obtained for the original unrolled cordic. The leakage power is 10548.948 nw ,dynamic power is 59433.044 nw and total power is 69981.992 nw.

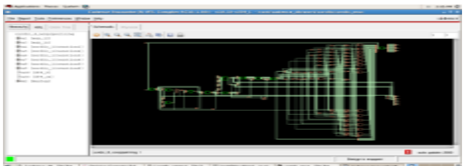


Fig 16.Netlist View for the Mux based Pipelined Unrolled Cordic

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 5, May 2015

TOOLS USED	THE POWER IN ORIGINAL UNROLLED CORDIC	THE POWER IN MUX BASED PIPELINED UNROLLED CORDIC
QUARTUS II SOFTWARE	111.79mw	115.55mw
CADENCE(DIGITAL) IMPLEMENTATION	78263.939nw	69981.992nw

Table 6 . Comparison table for QUARTUS II and CADENCE TOOL

V CONCLUSION AND FUTURE WORK

CORDIC algorithm was used to find out the trigonometric, hyperbolic, linear and logarithmic functions. In CORDIC algorithm two schemes was discussed .First scheme was original unrolled CORDIC and second scheme was MUX based pipelined unrolled CORDIC. Compared to first scheme, the second scheme is more reliable, since the second scheme uses multiplexer and registers. By adding multiplexer the area is reduced comparatively to the first architecture, since the first scheme uses only addition, subtraction and shifting operation in all the 8 stages. 8 iterations are performed and it is implemented on QUARTUS II software. The same is implemented in cadence(digital) tool and the power obtained was compared with both QUARTUS II and CADENCE TOOL. An efficient power reduction was obtained in CADENCE TOOL.For future work, the number of iterations can be increased and also increase the bit size

REFERENCES

[1] J.E. Volder, "The CORDIC Trigonometric Computing Technique", IEEE Transactions on Electronic computer, vol.EC-8, pp. 330-334, 1959.
[2] J. Walther, "a unified algorithm for elementary functions," proc. Spring joint comp. con & vol.38, pp.379-385, 1971.
[3] Vankka J; Kosunen M; Hubach J; Halonen K; "A CORDIC- based multicarrier QAM modulator," Global Telecommunications conference,1999.GLOBECOM' 99,vol.1A,no.,pp. 173- 177vol.1a,1999 .
[4] Chen A; McDanell R; Boytim M; Pogue R; "Modified CORDIC demodulator implementation for digital IF-sampled receiver," Global Telecommunications Conference, 1995. GLOBECOM '95., IEEE , vol.2, no., pp.1450-1454 vol.2, 14-16 Nov 1995.
[5] Deprettere E; Dewilde P; Udo R; "Pipelined cordic architectures for fast VLSI filtering and array processing," Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '84. , vol.9, no., pp. 250- 253, Mar 1984.
[6] SupriyaAggarwal, Pramod K. Meher, and KavitaKhare "Area-Time Efficient Scaling-Free CORDIC Using Generalized Micro-Rotation Selection"
[7]. Terence K. Rodrigues and Earl E. Swartzlander, "Adaptive CORDIC: Using parallel Angle Recoding to Accelerate",Proc.IEEE Transactions on computers,Vol.59,No.4,pp.522-531,2010.