# Passive Multiplexer Test Structure For Fast and Accurate Contact and Via Fail-Rate Evaluation

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***Abstract*—Complexity of integrated circuits has led to millions of contacts and vias on every chip. To allow accurate yield evaluation, it is required to determine fail rates of $< 10$ faults per billion, which requires test structures with huge chains of 1 million or more contacts and vias. At the same time, contacts and vias are getting smaller, and thus their resistance is increasing for every new technology node. Consequently, the resistance of such chains becomes impossible to measure. To overcome this limit without increasing the number of measurement pads, we are proposing a passive multiplexer array of via chains, which breaks up a huge contact–via chain in many individually measurable subchains. Accuracy of fail rates will be increased since the fail rate can be determined based on many subchains, instead of being determined based on only one huge chain. Furthermore, this test structure better supports failure analysis since it is faster to locate a faulty contact or via. No additional devices or process steps are required which allows implementation as short flows for fast process problem debugging.**

***Index Terms*—Multiplexing, testing, test structure, yield.**

## I. Introduction

THE FABRICATION of integrated circuits is an extremely complex process that may involve hundreds of individual operations. Each step has to work without any errors to produce an integrated circuit that is working toward its specification without errors. A typical completed integrated circuit may have millions of transistors and interconnecting routing elements over many layers that will define its function. The electrical connections from one interconnect layer to another interconnect layer are called vias while layers which connect an interconnect layer to a transistor are called contacts. Typically, a large complete integrated circuit may have anywhere from 1 to 100 million vias and contacts. A failure of any one of these usually means a complete failure of the circuit. Thus, exceptionally high yields are required for vias and contacts—usually better than five failures per billion vias or contacts [1].

Traditionally, via and contact yields are measured by fabricating test structures composed of chains of vias or contacts connected end to end in a serial fashion, such as shown in Fig. 1 [2]. Optical inspection equipment is usually not reliable or useful especially for current process technologies. These chains need to be long enough to permit measurement of very small failure rates using commonly used yield prediction methods [1]. Unfortunately, overly long via or contact chains cannot be measured because the resistance becomes too high. If there is a failure in a huge via chain containing 1 000 000 or more vias, there is no easy way of knowing exactly which via or contact failed. A via chain could be taped at multiple places to overcome some of these limitation, but in this case many extra pads would be needed, which will significantly reduces the chip area available for the via chains themselves. Extra pads also cause increased test times.

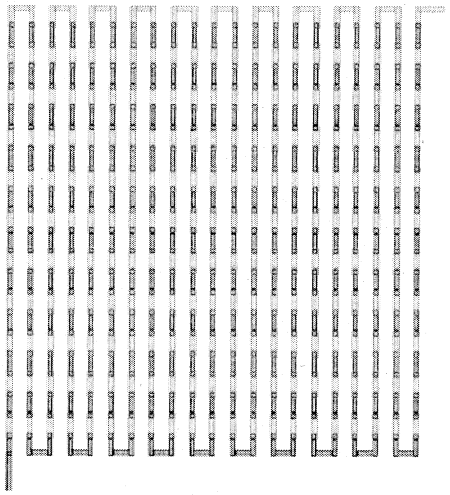

Fig. 1. Traditional serial via–contact chain [2].

There have been methods proposed using a diode or transistor array to allow smaller subchains by keeping the number of pads low, but additional process steps needed to implement such techniques slow down the process debugging feedback loop [3], [4]. References [5] and [6] have proposed a method that works without additional devices. However, the number of implemented vias is demonstrated too small for today's yield prediction purposes and this paper will extend this approach to much larger via numbers and faster test methods. The following presents a methodology that will:

- permit determination and modeling of the effect of neighborhood and via attributes on yield;
- allow spatial or systematic failures within a die to be observed and modeled;
- permit the measurement and modeling of via or metal shorts independently from via opens;
- enable a procedure for measuring the test structures using digital testers as well as analog testers;

For ease of reference, we refer to the test structure as a passive multiplexer configuration.

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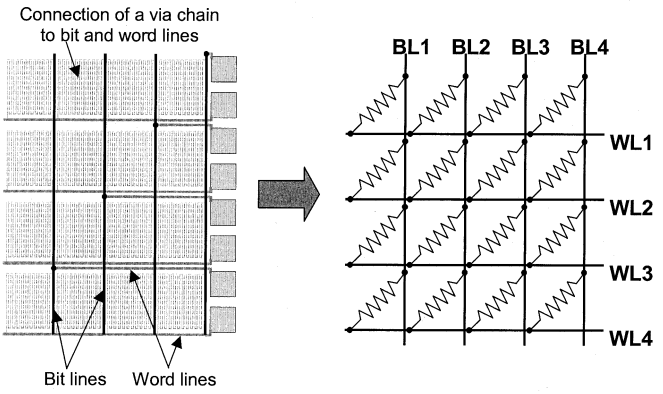


Fig. 2. Passive multiplexer configuration (layout on the left and schematic on the right).

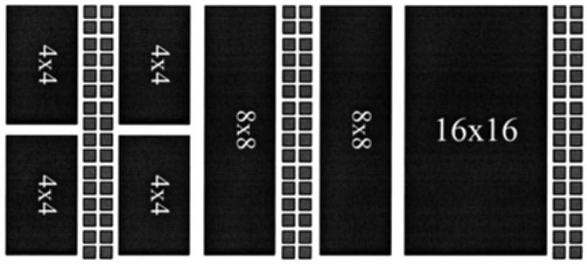


Fig. 3. Examples of different block configurations for the passive multiplexer structure.

## II. Test Structure Design

The passive multiplexer, as shown in Fig. 2, is composed of horizontal word lines and vertical bit lines, which connect to the probe pads. Each region inside of a word line and bit line is called a bit. The word lines and bit lines are purposely drawn wide to prevent the introduction of any opens in these tracks and to permit a low resistance path to each bit. Any vias used to connect the word lines or bit lines to the pads are also doubled up to insure that any opens are due from the bit cells themselves and not any parasitic opens in the vias–contacts used in the bit lines or word lines. Inside each bit, a traditional serial via or contact chain is placed. One end is routed to the word line while the other end is connected to a bit line.

Fig. 2 shows a passive multiplexer in a $4 \times 4$ configuration; that is, each block is composed of $4 \times 4$ or 16 individual bit cells. Many variants of the passive multiplexer are possible such as the $16 \times 16$ and $8 \times 8$ configurations shown in Fig. 3. The size of each block in a passive multiplexer configuration is at the discretion of the designer, but each block can be no more than $(N/2) \times (N/2)$ in size where $N$ is the number of pads in each pad frame (32 in this example). The breakdown of a passive multiplexer into a $4 \times 4$, $8 \times 8$, or other configuration is critical for allowing testing using digital testers, for allowing independent measurement of via–metal shorts from via opens, and for modeling the effect of via attributes on via open and metal–via shorts.

The structure inside each bit of the passive multiplexer is also central for successful yield prediction. So, for instance the density of vias should be varied, to better copy the via density variation that occurs in regular product chips. In addition,

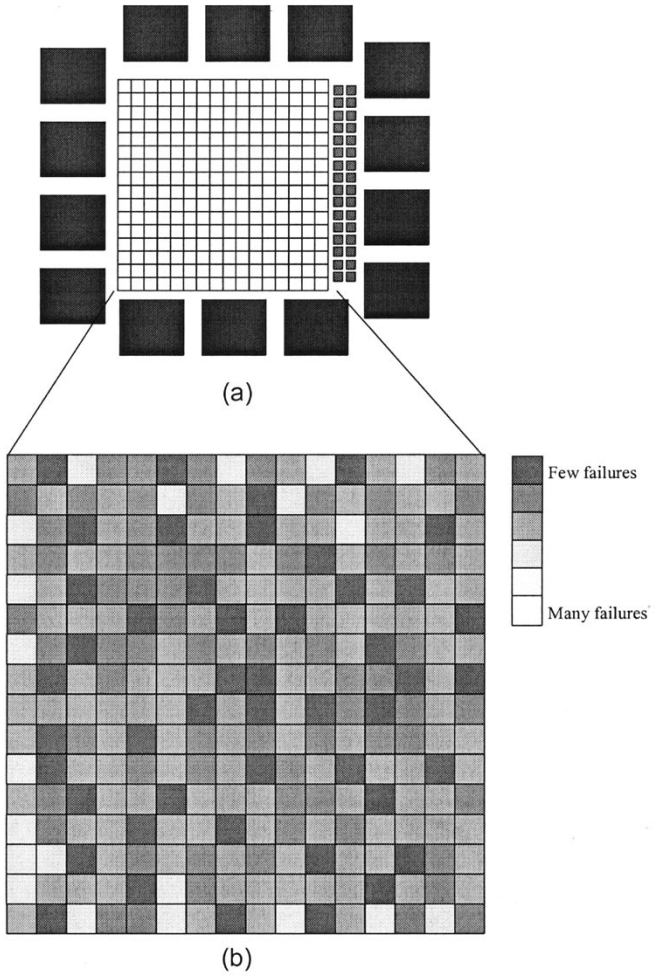


Fig. 4. (a) Examples of different block configurations for the passive multiplexer structure. (b) Passive multiplexer with neighboring patterns failure bitmap.

process-related issues such as variation of via size or metal overlaps can be explored as documented in [7]. Since no diodes or other active devices are needed, the passive multiplexer can be run as a short-flow; i.e., only METAL1-VIA-METAL2 (in the case of via) or POLY-CONTACT-METAL1 or AA-CONTACT-METAL1 (in the case of contacts) need to be fabricated. Even though an entire passive multiplexer structure may contain 100 000 vias or contacts, a $16 \times 16$ configuration implies that each bit would have $100\,000/256 \sim 400$ vias. Thus, failures can be localized down to 400 vias. Hence, it is far easier to perform failure analysis rather than on 100 000 vias, for which failure analysis is practically impossible without prolonged use of special tools such as voltage contrast testers.

Finally, by looking at the yield of each bit in a multiplexer, spatial dependencies within a die can be observed and correlated to various process effects. For example, consider the two sample structures shown in Figs. 4 and 5. Fig. 4(a) shows the multiplexer with neighboring structures placed very close to the multiplexer while Fig. 5(a) shows the multiplexer which has been isolated from neighboring structures by several hundred micrometer. Dummy metal lines have been used as neighboring structures, which are drawn at the nominal metal den-

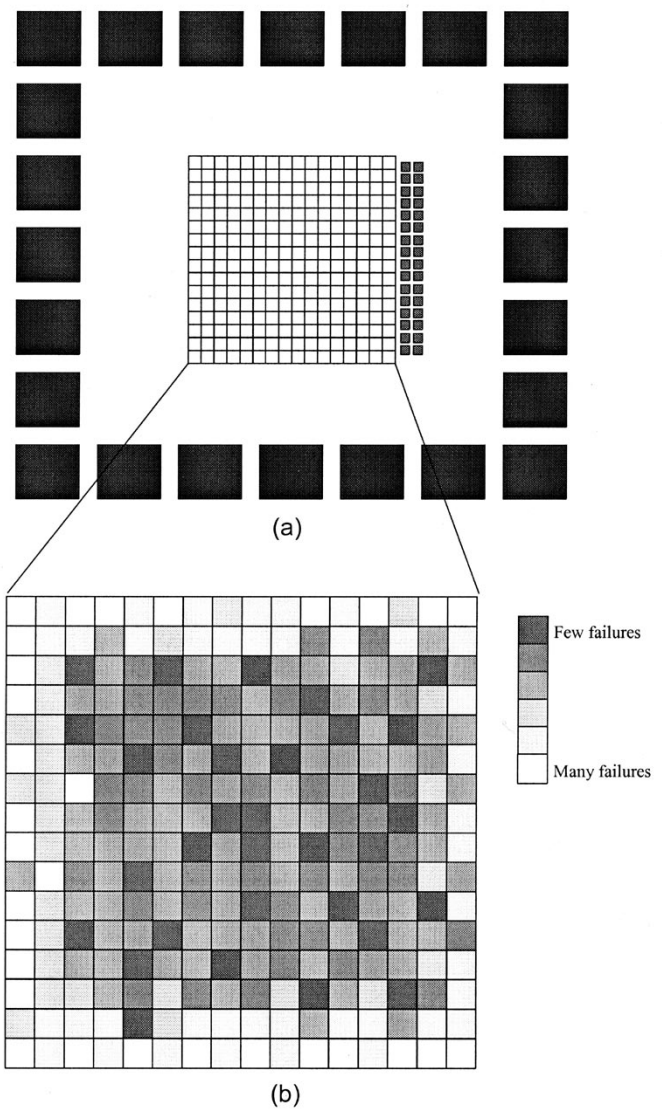


Fig. 5. (a) Isolated passive multiplexer structure. (b) Isolated passive multiplexer structure failure bitmap.

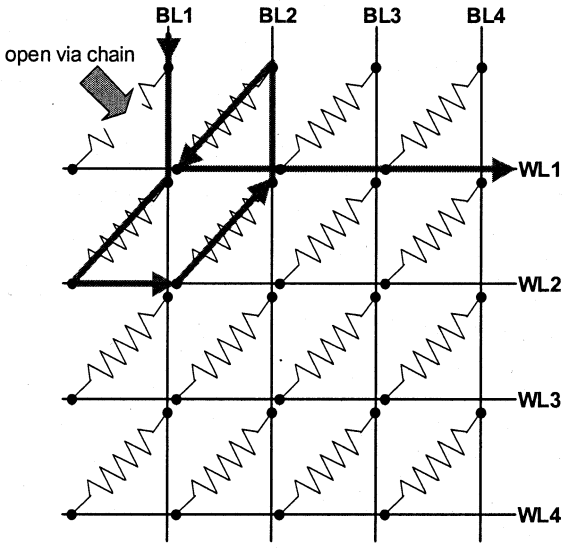


Fig. 6. Even though the bit in the upper left corner is open, a current still flows from the bit line to the word line associated with this bit in the upper left corner. A sample path is highlighted.

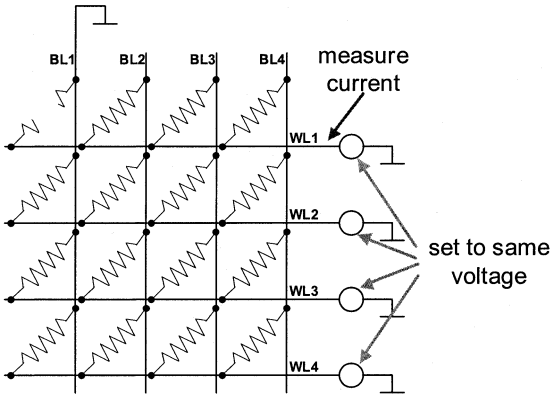


Fig. 7. Correct method for measuring the upper left corner bit. Other bits are measured by measuring the current on the word line connected to the bit and grounding the bit line connected to the bit. All other bit lines are left floating.

sity as recommended in the design rules. The resulting example yield maps by bit for Figs. 4(a) and 5(a) are shown in Figs. 4(b) and 5(b), respectively. Clearly, the number of failures around the edge of the multiplexer structure is significantly higher for Fig. 5(b) compared with Fig. 4(b). This is because of the uniform density around the edge of the multiplexer in Fig. 4(a) while Fig. 5(a) has a very different and much lower density around the edge of the multiplexer. Thus, one can conclude that there are systematic failure mechanisms owing to differences in density of neighboring structures or lack of proximity of neighboring metal–vias. The difference in fail rates with and without neighboring structures maybe more or less significant for different via pitches due to the chemical mechanical polishing (CMP) recipe being used as well as mechanical stress which is dependent on the interlayer dielectric material being used.

## III. Test Procedure

Unfortunately, measuring the yield of each bit in the passive multiplexer is not simply a matter of measuring the current flowing between the bit line and word line connected to each bit. This is because the passive multiplexer has multiple connection paths. Even if the bit under test is truly open, a current will still be measured because it can flow from the word line to the bit line using any of the other surrounding bit or word lines. Fig. 6 shows that if the bit in the upper left corner is open, a current can still flow through the word line and bit lines attached to this particular bit.

In order to test a particular bit, a different approach is needed. All of the word lines should be attached to the power supply and only the bit line related to the bit of interest should be connected to ground. All of the other bit lines should be left unconnected. The current flowing from the word line connected to the bit line of interest to the grounded bit line is the measurement of concern. The "sneak" path as described in Fig. 6 is blocked, since no current can flow between different word lines if they are set to the same voltage. Fig. 7 shows this procedure for measuring the bit in upper left of a $4 \times 4$ configuration. By measuring the current flowing through each word line with the required bit line

TABLE I
MEASUREMENT VECTORS FOR PARAMETRIC TESTING ON A 4 × 4 PASSIVE MULTIPLEXER

| Pin Number ---> | | | 1 9 17 25 | 2 10 18 26 | 3 11 19 27 | 4 12 20 28 | 5 13 21 29 | 6 14 22 30 | 7 15 23 31 | 8 16 24 32 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Test Vector | Row | Column | | | | | | | | | Measurement | Measurement Pins |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | X | X | X | Open test | 5,13,21,29 |
| 2 | 2 | 2 | 0 | 1 | 1 | 1 | X | 1 | X | X | Open test | 6,14,22,30 |
| 3 | 3 | 3 | 0 | 1 | 1 | 1 | X | X | 1 | X | Open test | 7,15,23,31 |
| 4 | 4 | 4 | 0 | 1 | 1 | 1 | X | X | X | 1 | Open test | 8,16,24,32 |
| 5 | 1 | 5 | 1 | 0 | 1 | 1 | 1 | X | X | X | Open test | 5,13,21,29 |
| 6 | 2 | 6 | 1 | 0 | 1 | 1 | X | 1 | X | X | Open test | 6,14,22,30 |
| 7 | 3 | 7 | 1 | 0 | 1 | 1 | X | X | 1 | X | Open test | 7,15,23,31 |
| 8 | 4 | 8 | 1 | 0 | 1 | 1 | X | X | X | 1 | Open test | 8,16,24,32 |
| 9 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | X | X | X | Open test | 5,13,21,29 |
| 10 | 2 | 2 | 1 | 1 | 0 | 1 | X | 1 | X | X | Open test | 6,14,22,30 |
| 11 | 3 | 3 | 1 | 1 | 0 | 1 | X | X | 1 | X | Open test | 7,15,23,31 |
| 12 | 4 | 4 | 1 | 1 | 0 | 1 | X | X | X | 1 | Open test | 8,16,24,32 |
| 13 | 1 | 5 | 1 | 1 | 1 | 0 | 1 | X | X | X | Open test | 5,13,21,29 |
| 14 | 2 | 6 | 1 | 1 | 1 | 0 | X | 1 | X | X | Open test | 6,14,22,30 |
| 15 | 3 | 7 | 1 | 1 | 1 | 0 | X | X | 1 | X | Open test | 7,15,23,31 |
| 16 | 4 | 8 | 1 | 1 | 1 | 0 | X | X | X | 1 | Open test | 8,16,24,32 |

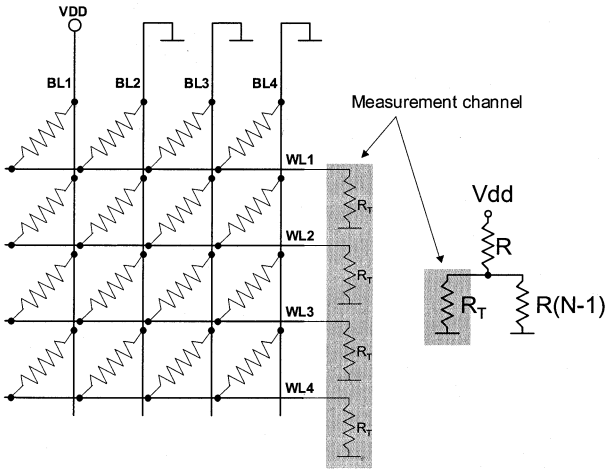


Fig. 8. Arrangement of two passive 8 × 8 multiplexers in a 32 pad frame configuration.

grounded and then cycling through all the bit lines, each individual bit can be measured. If the measured current is below some predefined threshold, the bit is considered to have failed. Table I shows an example for a complete set of 16 test vectors for 4 passive 4 × 4 multiplexer within a 2 by 16 padframe.

The method of testing listed above is similar to that discussed by Walton, *et al.* in [5] and [6]; however, it is very slow and requires careful programming of the tester. For rapid measurement, a digital test approach is needed. Based on methods described in [8], Fig. 8 shows the setup for measurement using a digital tester for a 4 × 4 multiplexer. In each case, a terminating resistor $R_T$ must be attached to each row of the multiplexer (ideally, but not necessarily, $R_T \gg R$). The rows of the multiplexer are attached to the measurement channels of the digital tester. Using a measurement channel, the terminating resistor can be set to any reasonable value. A "1" or "$Vdd$" is attached to one of the $N$ columns of the multiplexer as shown in Fig. 7 and the remaining columns are attached to "0" or "$Gnd$." As far as the measurement channel is concerned, the multiplexer looks like a voltage divider with one end connected to a resistor of value $R$ through $Vdd$ and the other end connected to ground through $(N-1)$ resistors $[R(N-1)]$ connected in parallel to the terminating resistor. If we assume $R_T \gg R$, then the measurement channel sees a voltage of approximately $(Vdd/N)$ if there are no opens in the structure or a voltage of nearly "0" if there is an open in the chain (see Table I). If we assume any voltage significantly $> 0$ is a pass and any voltage approximately equal to zero is a fail, then we can measure the yield of each chain. The pass–fail criteria should not be set to exactly zero since some noise will always be present in the system. Since the digital tester has many measurement channels, we can also measure the yield of each chain in the column simultaneously and then repeat the measurement method on the next column, etc. Since a digital tester can make each measurement in microseconds, the entire passive multiplexer can be tested in less than 1 s. Although we make mention of this method toward digital testers, the use of this method can be equally replicated using an analog or parametric measurement method.

## IV. EXPERIMENTAL RESULTS

Many passive multiplexer via and contact arrays have been manufactured at Philips Semiconductor in San Antonio, TX. The primary features of the 0.20-$\mu$m five-layer metal complementary metal–oxide–semiconductor process are:

- Shallow trench isolation (STI).
- High density plasma (HDP) oxide for trench fill.
- CMP.
- Dual gate oxide.
- Dual doped (N + /P+) poly gates.
- Titanium salicide.
- TiN–AlCu–TiN metal stack.

The process employs STI with HDP oxide for gap fill, dual-gate oxide, complementary (N + /P+) polysilicon gate electrodes, inorganic (SiON) bottom antireflective coating to facilitate gate lithography, titanium salicide to cover diffusion

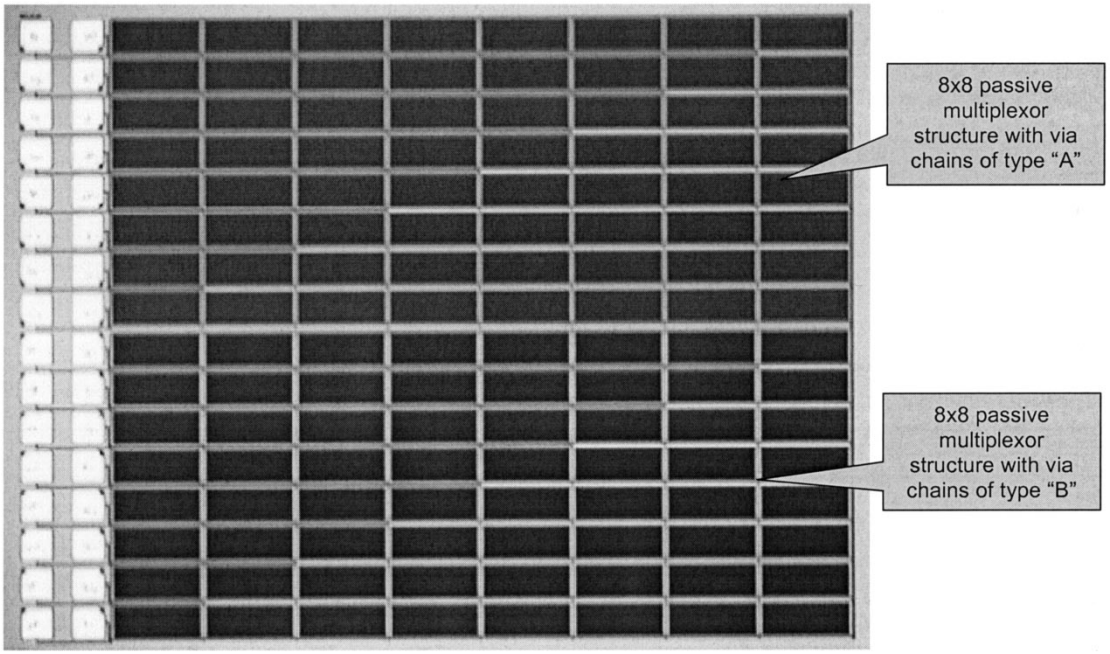


Fig. 9. Measurement setup for using a digital tester.

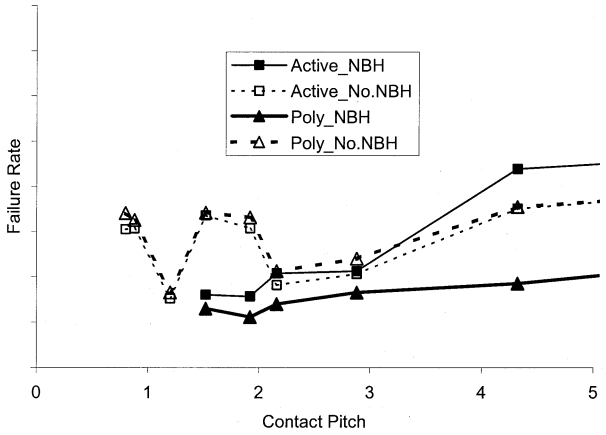


Fig. 10. Contact fail rate dependent on contact density (pitch), layer, and neighborhood.

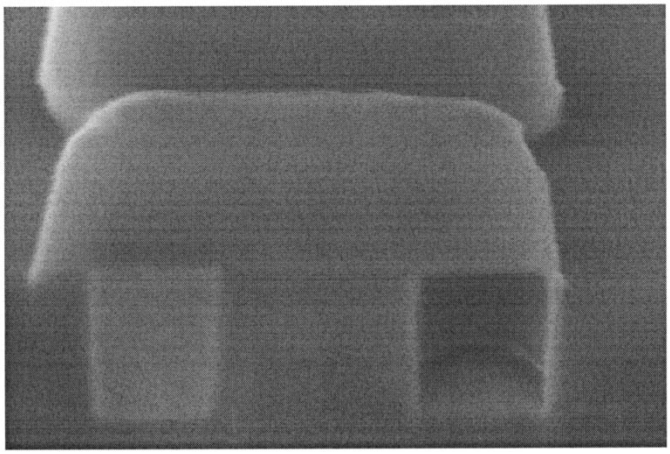

Fig. 11. FA analysis indicates that contact–via failures are from missing tungsten in the plug.

and gate regions, CMP for planarization of trench and intermetal dielectrics, and a TiN–AlCu–TiN stack for each of the five metal layers. Fig. 9 shows a 2 by 16 padframe with two passive $8 \times 8$ multiplexers.

Contact and via short flows using passive multiplexers have consistently shown high failure rates as they can be seen in Fig. 10 dependent on contact density (pitch), layer, and neighborhood. A clear trend of failure rate versus contact pitch can be seen, which is caused by a tungsten CMP loading effect where less dishing (plug recess) occurs for dense area contacts. In addition, the extensive forced-air-cooled transformer (FA) analysis has shown these failures are from missing tungsten in the plug, as can be seen in Fig. 11. It is caused by corrosion, which is an electrochemical reaction between charged metal structures, the exposed tungsten plug, and the polymer solvent applied after metal etch. More detailed experimental results using a passive multiplexer test structure are described in [9].

## V. Conclusion

The passive multiplexer test structure, which has been presented, allows breaking up large contact and via chains into smaller subchains, without increasing the number of pads to measure them. No additional process steps or active devices are needed to implement this concept which supports fast manufacturing as short flows. Thus, process problem debugging will be faster which will further be enhanced by better support of failure analysis within the subchains. In addition, the described measurement procedure for measuring the test structures using digital testers as well as analog testers will further allow wide usage within a given fab–measurement environment. Using contact and via chains within the passive multiplexer enables determination and modeling of the effect of neighborhood and via attributes on yield. Spatial or systematic failures within a die can be observed and modeled. The passive multiplexer design, in conjunction with the proposed test procedures, allows the

measurement and modeling of via or metal shorts independently from via opens. Although serial via chains are often placed inside each bit, any type of structure can be used where measuring open yield is important.

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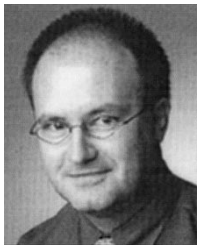

**Christopher Hess** (S'94–A'98–M'00–SM'01) was born in Wiesbaden, Germany. He received the diploma degree in electrical engineering from the University of Karlsruhe, Germany in 1992 and the Dr.-Ing. (Ph.D.) degree in computer science from the University of Karlsruhe, Germany in 1998.

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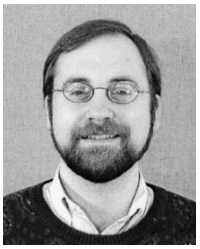
Dr. Hess is a member of the IEEE Electron Device Society. He is a technical committee member of several semiconductor manufacturing related conferences. He has served as Technical Chairman of the 2000 International Conference on Microelectronic Test Structures (ICMTS) and General Chairman of ICMTS in 2003.



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He was an Intel Graduate Fellow in 1997. He is currently a Director in the client services organization of PDF Solutions, Inc., San Jose, CA. His work mostly focuses on accelerating yield ramps of system-on-chip products for 0.18, 0.13 $\mu$m, and below technology nodes for key clients in the Japanese semiconductor market.

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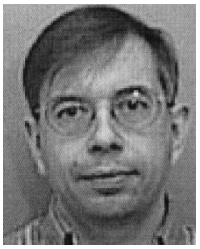

**Todd Mitchell** (M'81) received the B.S. in physics from the University of Arizona, Tucson, in 1980.

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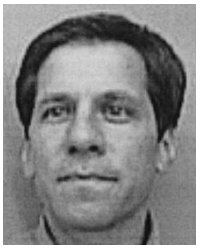
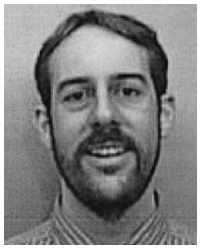
Mr. Mitchell is a member of Sigma Pi Sigma.



**Martin P. Karnett** (M'88–SM'01) received the B.S. degree in chemistry from the State University of New York (SUNY), Stony Brook, in 1977, and the Masters and Doctorate degrees in physical chemistry from Yale University, New Haven, CT, in 1978 and 1981, respectively.

He is currently Technology Enhancement and Yield Improvement Manager for Philips Semiconductor in San Antonio, TX, where he has been with the company for more than seven years. Prior to joining Philips, he enjoyed employment over a period of eleven years at both Raytheon Company and the Department of Defense where his positions included Photolithography Engineer, Device Engineering Manager, and Wafer Fab Manager.



**Keith Gardner** received the B.Sc. in chemical engineering from Arizona State University, Tempe, AZ, in 1986.

He spent ten years working in manufacturing and device engineering with VLSI Technology, Inc. and has contributed for the past four years as a Yield Engineer at Philips Semiconductors, San Antonio, TX.