Precision microcomb design and fabrication for x-ray optics assembly

Yanxia Sun,[a] Ralf K. Heilmann,[b] Carl G. Chen, Craig R. Forest, and Mark L. Schattenburg
Space Nanotechnology Laboratory, Center for Space Research, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139

(Received 26 June 2003; accepted 2 September 2003; published 10 December 2003)

Silicon microcombs developed at our laboratory for the precision alignment and assembly of large-area foil optics have previously been demonstrated to achieve submicron-level assembly repeatability with submillimeter-thick flat substrates. In this article we report on a double-side deep reactive-ion etch fabrication process using silicon-on-insulator wafers which was developed to improve the microcombs' manufacturing accuracy. © *2003 American Vacuum Society.* [DOI: 10.1116/1.1621668]

I. INTRODUCTION

The Constellation-X mission is the next major NASA x-ray observatory,[1] which expands on the capabilities of the current Chandra[2] and XMM[3] missions. For its spectroscopy x-ray telescope to meet the mission requirement of 15 arc sec half-power diameter resolution, thousands of segmented cylinder-like foil mirrors must be aligned at grazing incidence to the focal plane to a tolerance in the neighborhood of 1 μm. A typical optic resembles a 60° partial cylinder of 200 mm length and a wall thickness of 440 μm.[4] Precision silicon microcombs[5] developed in our laboratory have previously been used to assemble submillimeter-thick flat substrates to achieve submicron-level assembly repeatability and accuracy.[5,6] Their design was modified to hold cylindrical Wolter-I type optics for Constellation-X to improve the total assembly accuracy. In this article, a silicon-on-insulator (SOI) double-side etch fabrication process is reported, which was developed to improve the microcombs' manufacturing accuracy.

II. DESIGN OF MICROCOMBS

The design for a set of microcombs includes two types of combs. Reference combs provide highly accurate quasisingle-point contacts against which mirrors are registered, and spring combs provide the mechanical actuation needed to properly position the mirrors (see Fig. 1). A raised-up nose-like feature (so-called bullnose) was added to reference combs to remove an Abbe misalignment error source. The details of the mechanical design of microcombs and the assembly strategy are described in previous publications.[7–9]

III. MICROCOMB FABRICATION

A. Previous results

Microcombs are fabricated with microelectromechanical systems technology.[5] Both photoresist (PR) and silicon dioxide serve as etch masks during the deep reactive-ion etch (DRIE) process, which plasma etches through the entire silicon wafer. We use double-side polished (DSP) wafers for microcomb fabrication. Figure 2 shows a scanning electron microscope (SEM) micrograph of a pair of microcomb teeth.

The manner in which photoresist and silicon dioxide are patterned contributes to dimensional accuracy loss, and the etching uniformity of the DRIE process further limits the final manufacturing accuracy. However, we are presently only interested in the relative placement of the tooth-to-mirror contact points and their relative placement with respect to the bullnose tip, which we call position accuracy. That means as long as the dimensional accuracy loss is repeatable and uniform over the entire wafer, the combs will have perfect position accuracy. We have demonstrated position accuracy of better than 1 μm with a single-side etching process.[5] Our goal is to develop an improved microcomb fabrication process which can achieve position accuracy of much less than 1 μm.

Our current DRIE fabrication facility has poor etch rate uniformity over the entire wafer, especially for larger and therefore thicker wafers. Etch rate variations cause variations in mask erosion and undercut, thus compromising position accuracy. Figure 3 shows measured etch depth results for a group of 200-μm-wide trenches on a single 150-mm-diameter and 500-μm-thick wafer. The positions of measured points on the pattern are illustrated in Fig. 4. Four groups of measurements have been taken for 30, 60, 100, and 110 min etch times. Generally, the DRIE etch rate is nonuniform and nonsymmetrical, and the etch rate is always higher near the edge than in the center. The results show that the one sigma deviation from uniformity is 12.7% for a 30 min etch and 13.9% for a 100 min etch.

For efficient volume assembly of foil optics the combs should be as long as feasible. The design in Fig. 4 is for 100-mm-long microcombs, which requires patterning across an entire wafer. In order to etch through the middle trenches, the features at the wafer edges will require about 20 min overetch. This overetch introduces micrometer scale defects to the features which will directly affect position accuracy.

To make longer microcombs, larger and thicker wafers are required. The typical thickness of a double-side polished 150

[a]Electronic mail: yxsun@mit.edu
[b]Author to whom correspondence should be addressed; electronic mail: ralf@space.mit.edu

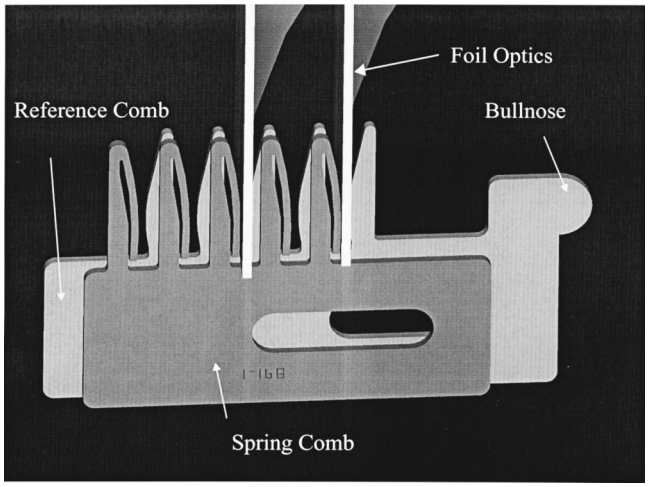

FIG. 1. Computer aided design model of a set of microcombs designed to hold cylindrical optic foils (only two foils and five teeth are shown).

mm wafer is 500 μm, which requires about 2.5 h DRIE for a 100-μm-wide trench. Long etches risk degrading the sidewall profile and surface roughness. Figure 5(a) shows a SEM micrograph of the regularly scalloped sidewall surface after a 30 min etch, and Fig. 5(b) illustrates a typical sidewall after a 90 min etch for comparison. The irregular rough surface may not meet assembly accuracy requirements. The problem is worse for narrower trenches.

B. Double-side etch process

A double-side etch process was investigated to help solve the comb accuracy problem. Silicon wafers were etched from both sides with wider trenches etched from the back. For a 100-μm-wide trench to be DRIE etched, oxide alone can serve as the protection mask. The accurate front-side DRIE etch depth is reduced to 100 μm, where the optic to be assembled only needs to touch the regularly scalloped sidewall. The process is illustrated in Fig. 6. Our mask aligner has a 2

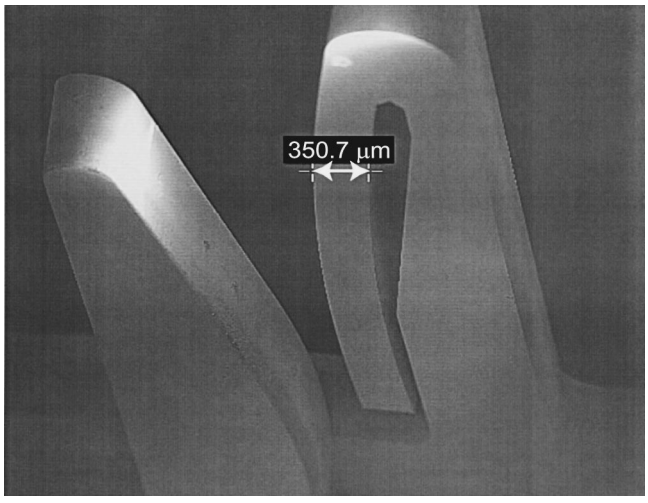

FIG. 2. SEM micrograph of a pair of microcomb teeth fabricated with a single-side etch process.

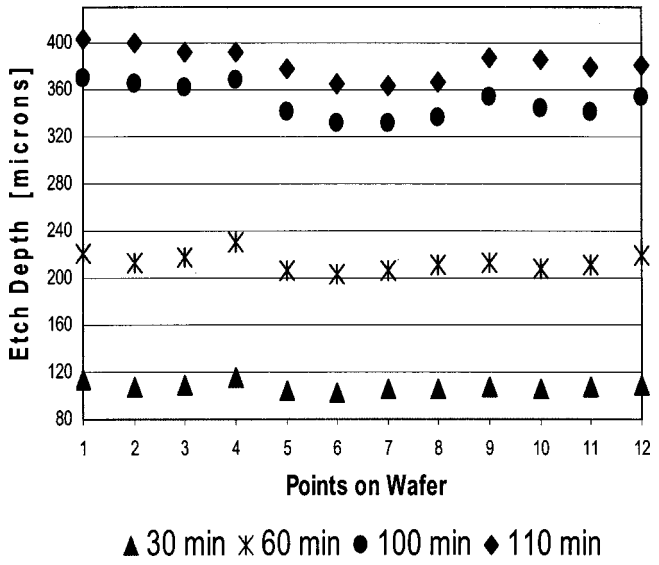

FIG. 3. Etch depth results over the entire wafer after 30, 60, 100, and 110 min of etching. Twelve points on the wafer are measured, and the trenches are 200 μm wide.

μm alignment accuracy for front-to-back alignment which is sufficient for our application. Optical contact lithography was used to pattern photoresist, which results in some accuracy loss. More accurate patterning such as direct e-beam lithography could be used to pattern the oxide so that better lithography results can be achieved, which in turn would yield even better position accuracy. The result of the double-side etch process on silicon is illustrated in Fig. 7.

However, since the depth of the front side etch is affected by the nonuniform etch depth of back side features, regardless of which side is etched first, the depth of the accurate front side features cannot be held constant. For larger and

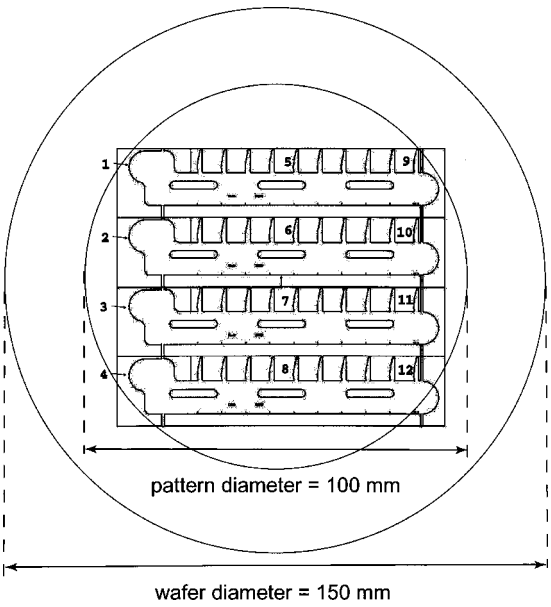

FIG. 4. Locations on wafer where etch depth was measured. Measurements were performed at 12 points.

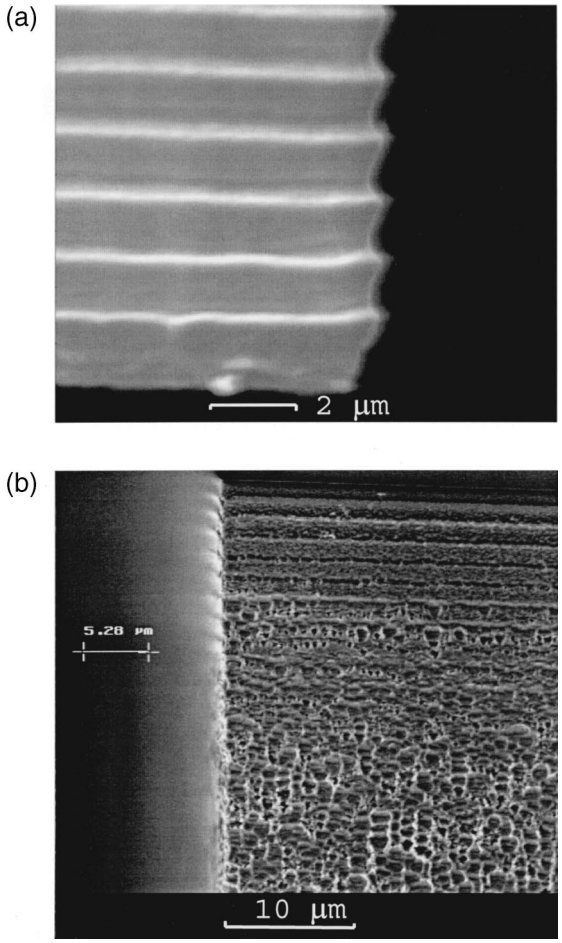

FIG. 5. SEM micrographs of typical DRIE results: (a) 30 min etch, showing regular scalloping and (b) 90 min etch, showing irregular and rough surfaces.

thicker wafers, the variation in depth is on the order of tens of microns, which will change the teeth's stiffness and the mechanical properties.

Furthermore, our current DRIE fabrication facility has poor repeatability performance. Figure 8 shows the measured

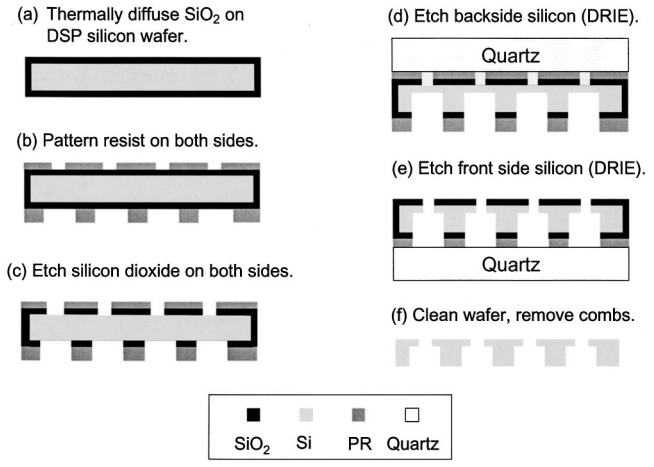

FIG. 6. Depiction of microcomb double-side etch fabrication process on DSP silicon wafer.

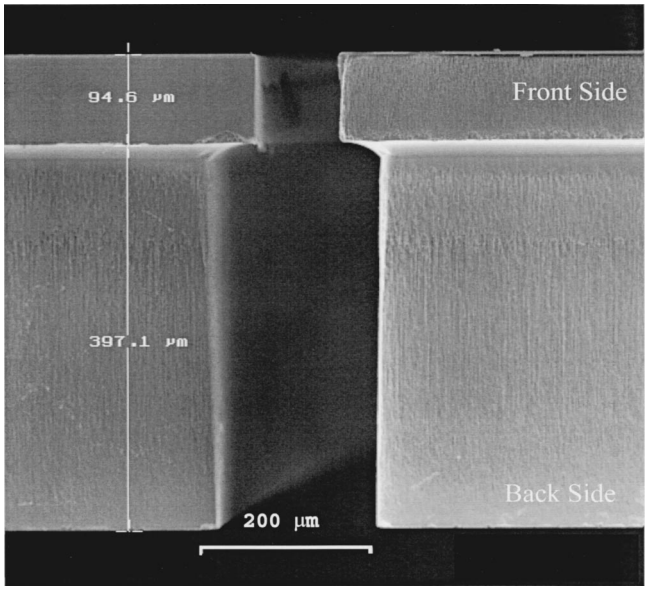

FIG. 7. SEM micrograph of a double-side DRIE etched trench. The widths of the trench in the mask are 100 and 200 μm for the wafer front and back side, respectively.

etch depth for 100-μm-wide trenches on six different wafers. The measured positions on each wafer are the same as those in Fig. 4. The results show that the etch depth is not repeatable even though the same machine and the same etch recipe have been used. The one sigma wafer-to-wafer variation for a 30 min etch over six wafers is 6.5%, and similar behavior has been observed for longer etch times. Since several microcombs have to be used together to build one module assembly, and hundreds of modules have to be assembled for the entire telescope construction so that replacement of microcombs due to wear or damage may be necessary, the repeatability problem will adversely affect assembly accuracy.

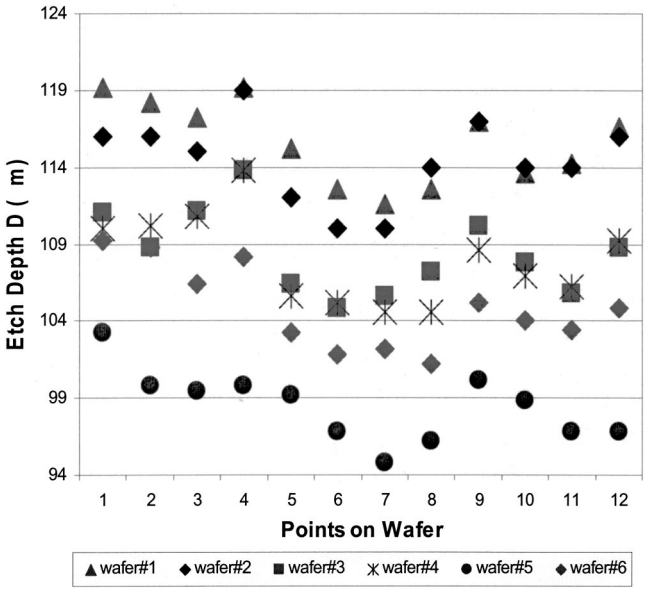

FIG. 8. Etch depth results with the same process and fabrication recipe for six different wafers. The trench is 100 μm wide and the etch time is 30 min.

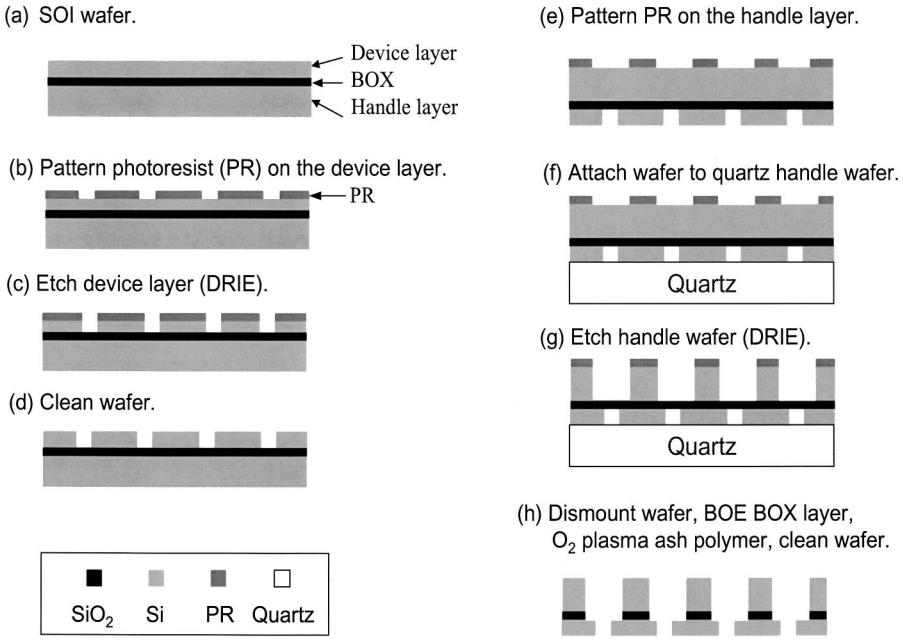

FIG. 9. Schematic of a revised microcomb double-side etch fabrication process on a SOI wafer. The device layer is 100 ± 1 μm, buried oxide layer (BOX) is 2 μm, and the handle layer is 350 ± 5 μm thick.

C. SOI double-side etch process

An improved fabrication process based on SOI wafers was developed. By applying the double-side etch process to a SOI wafer, the buried silicon dioxide (BOX) layer can serve as an etch stop for both etches, so that the dimensions of the foil optic contact area are determined by the thickness of the device layer of the SOI wafer which is very well controlled. Current commercially available SOI wafers have excellent total thickness variation (TTV) control on the device layer. The TTV for a 100-μm-thick layer is as good as 1 μm, which can be improved when device layers become thinner.

The revised fabrication process is illustrated in Fig. 9. The 2-μm-thick buried oxide layer is able to withstand a 15 min overetch from the backside and serves well as the etch stop. The BOX has been removed by buffered oxide etch (BOE) after the process is completed. Oxygen plasma etching (3–6 h) is required to remove the polymer layer deposited during the DRIE passivation cycles. Figure 10 shows a SEM micrograph for an etched trench on a SOI wafer. The BOX layer is unobservable in this image due to the undercut from the BOE etch.

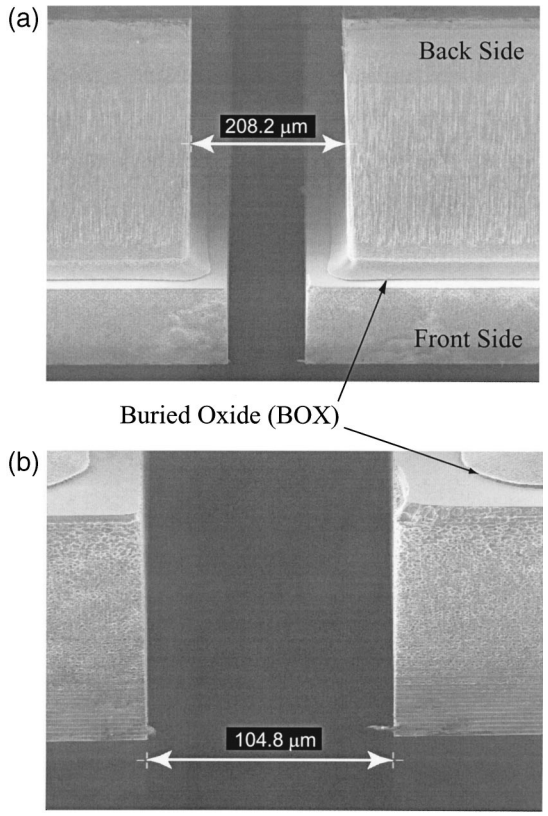

FIG. 10. SEM micrographs of a double-side etched trench on a SOI wafer. The widths of the trenches in the mask are 100 and 200 μm for the wafer front and back side, respectively: (a) low magnification and (b) high magnification.

IV. CONCLUSION

A SOI double-side etch process has been developed to fabricate accurate microcombs. The nonuniform and nonrepeatable DRIE results can be avoided if SOI wafers are used. The BOX layer of SOI wafers serves well as the etch stop. This fabrication process can improve the yield and the accuracy of microcomb fabrication. Longer microcombs can be fabricated with the same accuracy and repeatability using larger and thicker wafers. Assembly accuracy results obtained with improved microcombs will be reported soon.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the outstanding student, staff, and facility support from the Space Nanotechnology Laboratory, the Nanostructures Laboratory, and the Mi-

crosystems Technology Laboratory, all at MIT. This work is supported by NASA Grant Nos. NAG5-5271 and NCC5-633.

[1]R. Petre *et al.*, Proc. SPIE **4851**, 433 (2003).
[2]M. Weisskopf, B. Brinkman, C. Canizares, G. Garmire, S. Murray, and L. P. van Speybroeck, Publ. Astron. Soc. Pac. **114**, 1 (2002).
[3]B. Aschenbach, U. G. Briel, F. Haberl, H. W. Braeuninger, W. Burkert, A. Oppitz, P. Gondoin, and D. H. Lumb, Proc. SPIE **4012**, 731 (2000).
[4]W. A. Podgorski *et al.*, Proc. SPIE **4851**, 491 (2003).
[5]C. G. Chen, L. M. Cohen, R. K. Heilmann, P. T. Konkola, O. Mongrard, G. P. Monnelly, and M. L. Schattenburg, J. Vac. Sci. Technol. B **18**, 3272 (2000).
[6]G. P. Monnelly *et al.*, Proc. SPIE **4138**, 164 (2000).
[7]O. Mongrard, Master's thesis, Massachusetts Institute of Technology, Cambridge, MA, 2001.
[8]C. R. Forest *et al.*, Proc. SPIE **4851**, 538 (2003).
[9]C. R. Forest, Master's thesis, Massachusetts Institute of Technology, Cambridge, MA, 2003.