

## Research Article

# Charge-Trapping Devices Using Multilayered Dielectrics for Nonvolatile Memory Applications

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Charge-trapping devices using multilayered dielectrics were studied for nonvolatile memory applications. The device structure is Al/Y<sub>2</sub>O<sub>3</sub>/Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>/Si (MYTOS). The MYTOS field effect transistors were fabricated using Ta<sub>2</sub>O<sub>5</sub> as the charge storage layer and Y<sub>2</sub>O<sub>3</sub> as the blocking layer. The electrical characteristics of memory window, program/erase characteristics, and data retention were examined. The memory window is about 1.6 V. Using a pulse voltage of 6 V, a threshold voltage shift of ~1 V can be achieved within 10 ns. The MYTOS transistors can retain a memory window of 0.81 V for 10 years.

## 1. Introduction

One of the most attractive candidates for nonvolatile memory applications is the charge-trapping device in which multilayered dielectrics are used. The semiconductor-oxide-nitride-oxide-semiconductor (SONOS) memory is typical of the charge-trapping devices. The advantages of SONOS-type charge-trapping devices include smaller cell size, lower programming voltage, and better cycling endurance compared with the floating-gate devices. By reducing the tunneling oxide thickness in the SONOS-type devices, faster programming speed and lower operating voltage can be accomplished [1–4]. However, the issues of poor retention time and low erase speed still remain in the SONOS-type memory devices. To improve the retention time of SONOS devices, several researches have been reported. Hsu et al. indicated that HfO<sub>2</sub> can replace Si<sub>3</sub>N<sub>4</sub> and obtain a higher conduction band offset for better retention [5]. Reports showed that the retention of memory devices can be improved using a chemical-vapor-deposited blocking oxide [6] or implementing a high-temperature deuterium annealing [7]. Additionally, using a high-k dielectric as the blocking oxide, the program/erase speed and retention characteristic

can be improved [8, 9]. In the study using Si<sub>3</sub>N<sub>4</sub>, HfO<sub>2</sub>, and HfAlO as the charge storage layer, Tan et al. showed that larger band offset can improve the program speed and reduce the overerase phenomenon [10]. Furthermore, using the structures of TaN/HfO<sub>2</sub>/T<sub>2</sub>O<sub>5</sub>/HfO<sub>2</sub>/Si (MHTHS) and TaN/Al<sub>2</sub>O<sub>3</sub>/Ta<sub>2</sub>O<sub>5</sub>/HfO<sub>2</sub>/Si (MATHS) both program speed and retention time can be improved as compared to the traditional SONOS devices [11, 12].

In this work, charge-trapping devices using multilayered dielectrics were studied for nonvolatile memory applications. The structure is metal—yttrium oxide—tantalum oxide—silicon oxide—silicon (MYTOS), that is, Al/Y<sub>2</sub>O<sub>3</sub>/Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>/Si. The MYTOS devices were fabricated using Ta<sub>2</sub>O<sub>5</sub> as the charge storage layer and Y<sub>2</sub>O<sub>3</sub> as the blocking oxide for both high energy barrier at Al/Y<sub>2</sub>O<sub>3</sub> interface and large dielectric constant. The expected advantages of MYTOS device include longer retention time and faster program/erase speed. Figure 1 shows the energy band diagrams of the MYTOS memory device. The conduction band offset between the tunneling oxide and the high-k charge storage layer is 2.25 eV at the Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub> interface. The large conduction band offset is expected to improve the data retention property because the tunneling electrons

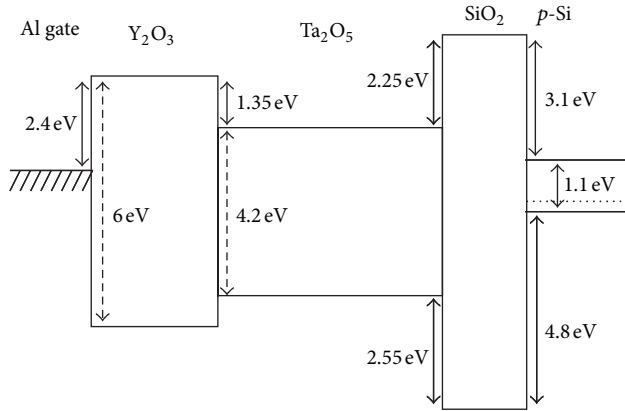


FIGURE 1: Schematic energy band diagrams of the Al/Y<sub>2</sub>O<sub>3</sub>/Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>/Si memory device.

can be firmly confined into the charge storage layer. In addition, the Ta<sub>2</sub>O<sub>5</sub> trap level is about 2.7 eV [13] below the conduction band edge which is much deeper than the 1 eV trap level in Si<sub>3</sub>N<sub>4</sub>. The deeper trap level is expected to further improve data retention characteristic. Aside from the retention property, the SONOS-type devices with high- $k$  blocking dielectrics can increase the electric field for the tunneling oxide at the same operating voltage used. Hence, the program/erase speed can be improved using a high- $k$  blocking layer. In this work, Y<sub>2</sub>O<sub>3</sub> is chosen to be the blocking oxide in which the charge injection efficiency in the tunneling oxide can be increased; meanwhile, the blocking function can be maintained. The dielectric constant of Y<sub>2</sub>O<sub>3</sub> blocking oxide is about 15 and the conduction band offset at the Ta<sub>2</sub>O<sub>5</sub>/Y<sub>2</sub>O<sub>3</sub> interface is about 1.35 eV. This large conduction band offset is expected to give better blocking efficiency which may improve the memory window characteristic. Besides, this high- $k$  blocking layer is expected to increase the program/erase speed as well as to reduce the program/erase voltage.

## 2. Experiment

P-type, (100) orientation, and 4-inch diameter silicon wafers with 1–10  $\Omega$  cm resistivity were used as the starting substrates. A 3 nm tunneling oxide (SiO<sub>2</sub>) was thermally grown by dry oxidation at 900°C. The charge storage layer (Ta<sub>2</sub>O<sub>5</sub>) was deposited by RF magnetron sputtering under a pressure of  $1.1 \times 10^{-3}$  torr at room temperature in argon gas. The purity of Ta<sub>2</sub>O<sub>5</sub> target is 99.9%. The thickness of the Ta<sub>2</sub>O<sub>5</sub> layer is 20 nm. The Ta<sub>2</sub>O<sub>5</sub> films were either as-deposited or annealed at 400°C, 500°C, and 600°C. The annealing was performed in nitrogen at a flow rate of 3 standard cubic centimeters per minute (sccm). After annealing, the blocking layer Y<sub>2</sub>O<sub>3</sub> was deposited by RF magnetron sputtering under a pressure of  $1.1 \times 10^{-3}$  torr at room temperature in argon gas. The thickness of the Y<sub>2</sub>O<sub>3</sub> blocking layer is 10 nm. For transistor processing, a 500 nm oxide was first grown by wet oxidation and used as the field oxide. The source and drain windows were defined by wet etching and doped by

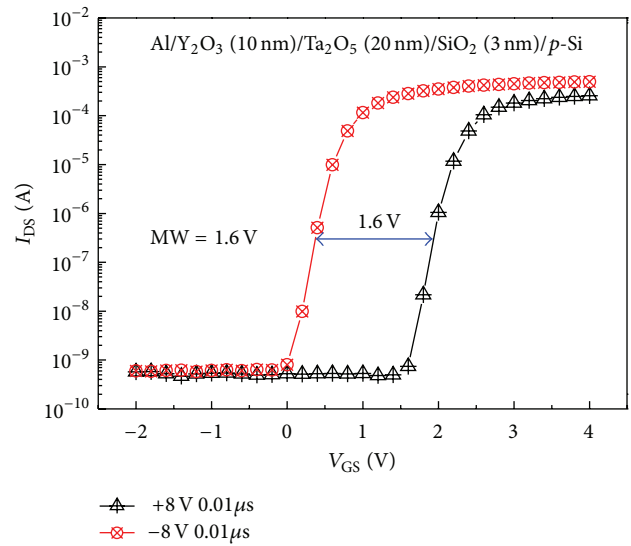


FIGURE 2:  $I_{ds}$ - $V_{gs}$  memory window characteristic.

arsenic implantation ( $5 \times 10^{15}$  cm<sup>-2</sup>, 40 keV). The implant was annealed at 950°C in N<sub>2</sub> for 30 minutes. The contact region in Ta<sub>2</sub>O<sub>5</sub> was etched by reactive ion etch (RIE) and in SiO<sub>2</sub> and Y<sub>2</sub>O<sub>3</sub> by buffered oxide etch (BOE). The 300 nm thick top aluminum electrodes were evaporated by DC sputtering. Postmetallization annealing (PMA) was performed at 400°C in N<sub>2</sub> for 30 seconds. The crystalline phase of the high- $k$  dielectric films was identified by X-ray diffraction (Shimadzu XD-5) using Cu K $\alpha$  radiation. Separate MHHOS capacitors were also fabricated. The  $I$ - $V$  characteristics were measured using Keithley 236 electrometer and the  $C$ - $V$  characteristics using high-frequency  $C$ - $V$  meter MegaBytek Mi-494.

## 3. Results and Discussion

Figure 2 shows the  $I_{ds}$ - $V_{gs}$  memory window measurement for MYTOS transistors. The  $I_{ds}$ - $V_{gs}$  memory window after a 8 V, 0.01  $\mu$ s program pulse is 1.6 V. The memory window can also be estimated by the capacitance-voltage ( $C$ - $V$ ) hysteresis curves for the MYTOS capacitors. Using a sweep voltage range of  $\pm 10$  V, the  $C$ - $V$  memory window of 1.6 V can be achieved due to the electron trapping (not shown here).

Figure 3 shows the programming characteristics of the MYTOS transistors. Pulse voltages of 6 V or 8 V are first applied to the gate. Thus, the electrons can tunnel from Si-substrate into Ta<sub>2</sub>O<sub>5</sub> and be stored into the Ta<sub>2</sub>O<sub>5</sub> charge storage layer which forms a potential well between Si-substrate and Y<sub>2</sub>O<sub>3</sub>, as shown in Figure 1. In the program event, Y<sub>2</sub>O<sub>3</sub> is the blocking layer which can prevent the tunneling electrons from passing across the Y<sub>2</sub>O<sub>3</sub> layer since the Y<sub>2</sub>O<sub>3</sub>/Ta<sub>2</sub>O<sub>5</sub> interface barrier is high enough. Accordingly, the tunneling electrons can be reserved into the Ta<sub>2</sub>O<sub>5</sub> charge storage layer. The pulse widths are from 10<sup>-8</sup> s to 10<sup>-2</sup> s. After applying the gate pulse, the threshold voltage of the transistor was monitored by measuring the  $I_{DS}$ - $V_{GS}$  characteristics.  $V_{th}$  is defined as the gate voltage at 1  $\mu$ A drain current with

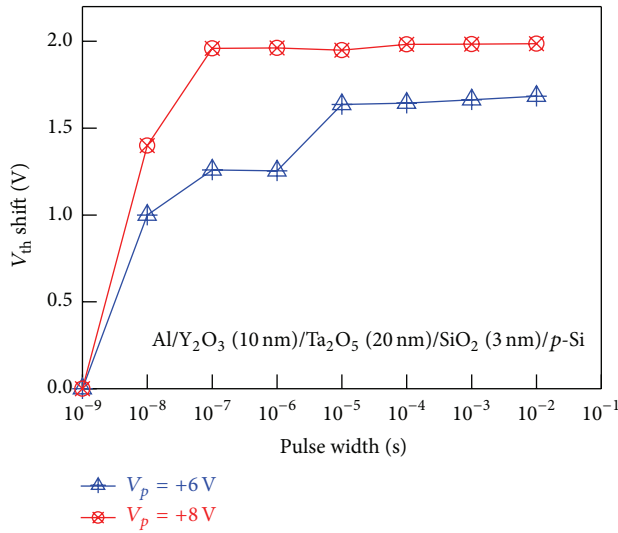


FIGURE 3: Programming characteristics of the Al/Y<sub>2</sub>O<sub>3</sub>/Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>/Si transistors.

$V_{DS} = 0.1$  V. The transistor is defined as “programmed” when the  $V_{th}$  shift is larger than 0.5 V. For MYTOS transistors, the  $V_{th}$  shift of more than 0.5 V will occur at an applied voltage of 6 V and with a pulse width 10 ns. For MHTHS [11] and MATHS [12], the  $V_{th}$  shift of more than 0.5 V will occur at an applied voltage of 10 V and with pulse widths of 1 ms and 100 ns, respectively. Therefore, low program voltage and fast programming speed were achieved with the MYTOS transistors in this work. The MYTOS transistors thus have faster programming speed and lower program voltage than MHTHS and MATHS memory devices. This is most likely due to the larger conduction band offset of 2.25 eV at the Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub> interface compared with 1.2 eV at the Ta<sub>2</sub>O<sub>5</sub>/HfO<sub>2</sub> interface. At the same gate bias where Fowler-Nordheim tunneling is dominating, the electron tunneling distance from Si-substrate to the conduction band of the storage dielectric is therefore shorter for structures with Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>. The large conduction band offset is expected to give better blocking efficiency which will improve memory window and programming speed. In addition, large conduction band offset can also relieve overerase problem. The program voltage of MYTOS transistor can be as low as 6 V, which is lower than that of 10 V for MHTHS [11] and MATHS [12]. The programming time of 10 ns is also faster than that of 1 ms and 100 ns of MHTHS and MATHS, respectively. As for the erase event, the negative pulse voltage is applied to the Al gate. Hence, the holes can tunnel from Si-substrate into Ta<sub>2</sub>O<sub>5</sub> and recombine the electrons stored into the Ta<sub>2</sub>O<sub>5</sub> layer. Figure 4 shows the erase characteristics of the MYTOS transistors. The transistor is defined as “erased” when the  $V_{th}$  reduces more than 0.5 V. Obviously, an applied gate voltage of -6 V is not enough to do the erase process. Meanwhile, the  $V_{th}$  reduced more than 0.5 V at an applied voltage of -8 V with a pulse width of 0.1  $\mu$ s.

Figure 5 shows the retention characteristic of the MYTOS transistors. The  $I_{DS}$  versus  $V_{GS}$  characteristic was first measured with a sweep voltage from -3 V to 3 V to determine

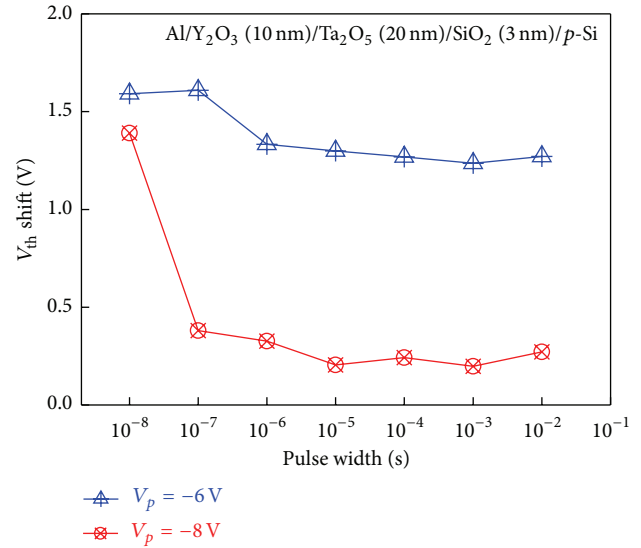


FIGURE 4: Erase characteristics of the Al/Y<sub>2</sub>O<sub>3</sub>/Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>/Si transistors.

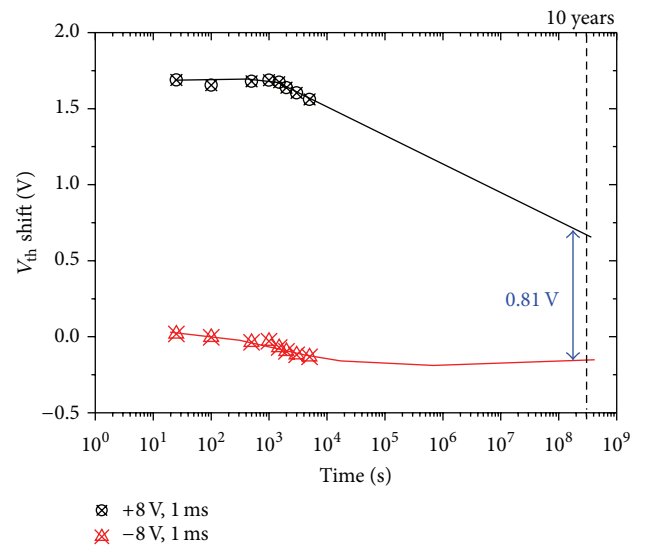


FIGURE 5: Retention characteristic of the Al/Y<sub>2</sub>O<sub>3</sub>/Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>/Si transistors.

the original threshold voltage. Pulse voltages of  $\pm 8$  V at 1 ms duration were then applied for program and erase operations. The threshold voltage shift is measured at different time periods. The MYTOS transistors are projected to have a  $\Delta V_{th}$  window of 0.81 V after 10 years. Table 1 lists the comprised memory parameters of the charge-trapping devices in which the adopted trapping layers include Ta<sub>2</sub>O<sub>5</sub>, Y<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, ZrO<sub>2</sub>, La<sub>2</sub>O<sub>3</sub>, and Dy<sub>2</sub>O<sub>3</sub> [11–20]. The MYTOS shows faster programming time of 10 ns at a low voltage of 6 V.

#### 4. Conclusion

In summary, Al/Y<sub>2</sub>O<sub>3</sub>/Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>/Si field effect transistors were fabricated and investigated. The electrical properties,

TABLE I: Comprised memory parameters of the charge trapping devices.

Trapping layer	Ta <sub>2</sub> O <sub>5</sub> (this work)	Ta <sub>2</sub> O <sub>5</sub> [11]	Ta <sub>2</sub> O <sub>5</sub> [12]	Y <sub>2</sub> O <sub>3</sub> [14]	Y <sub>2</sub> O <sub>3</sub> [15]	HfO <sub>2</sub> [16]	HfO <sub>2</sub> [17]	ZrO <sub>2</sub> [18]	La <sub>2</sub> O <sub>3</sub> [19]	Dy <sub>2</sub> O <sub>3</sub> [20]
Program speed	10 ns $V_g = 6\text{ V}$ $\Delta V_t = 1\text{ V}$	1 $\mu\text{s}$ $V_g = 10\text{ V}$ $\Delta V_t = 0.5\text{ V}$	10 ns $V_g = 10\text{ V}$ $\Delta V_t = 0.5\text{ V}$	0.1 ms $V_g = 8\text{ V}$ $V_d = 6\text{ V}$ $\Delta V_t = 1\text{ V}$	0.1 ms $V_g = 6\text{ V}$ $V_d = 8\text{ V}$ $\Delta V_t = 1.4\text{ V}$	1 $\mu\text{s}$	10 $\mu\text{s}$ $V_g = 15\text{ V}$ $V_d = 10\text{ V}$ $\Delta V_t = 1\text{ V}$	0.1 ms $V_g = 15\text{ V}$ $V_d = 10\text{ V}$ $\Delta V_t = 2\text{ V}$	0.1 ms $V_g = 9\text{ V}$ $V_d = 9\text{ V}$ $\Delta V_t = 2.1\text{ V}$	~0.1 s $V_g = 7\text{ V}$ $\Delta V_t = 0.5\text{ V}$
	100 ns $V_g = -8\text{ V}$ $\Delta V_t = 1\text{ V}$	10 ns $V_g = -10\text{ V}$ $\Delta V_t = 0.5\text{ V}$	1 $\mu\text{s}$ $V_g = -10\text{ V}$ $\Delta V_t = 0.5\text{ V}$	10 $\mu\text{s}$ $V_g = -3\text{ V}$ $V_d = 8\text{ V}$ $\Delta V_t = 1.5\text{ V}$	10 $\mu\text{s}$ $V_g = -3\text{ V}$ $V_d = 8\text{ V}$ $\Delta V_t = 2.1\text{ V}$	0.1 ms	10 $\mu\text{s}$ $V_g = -12\text{ V}$ $V_d = 10\text{ V}$ $\Delta V_t = 1.5\text{ V}$	10 ms $V_g = -10\text{ V}$ $V_d = 10\text{ V}$ $\Delta V_t = 2\text{ V}$	0.1 ms $V_g = -5\text{ V}$ $V_d = 9\text{ V}$ $\Delta V_t = 2\text{ V}$	~0.1 s $V_g = -10\text{ V}$ $\Delta V_t = 0.5\text{ V}$
Memory window	1.6 V 0.81 V ( $3 \times 10^8\text{ s}$ )	0.8 V 0.64 V ( $3 \times 10^8\text{ s}$ )	2.5 V 0.64 V ( $3 \times 10^8\text{ s}$ )	2.3 V 8%CL ( $10^4\text{ s}$ )	2.4 V 4%CL ( $10^4\text{ s}$ )	1.2-1.5 V 10%CL ( $10^5\text{ s}$ )	1.5 V 6%CL ( $10^4\text{ s}$ )	2.7 V 5%CL ( $10^4\text{ s}$ )	2 V 9%CL ( $10^8\text{ s}$ )	~1.5 V 0.9 V ( $3 \times 10^8\text{ s}$ )
Retention										

CL: charge loss.

including memory window, program/erase characteristics, and data retention time, were measured. The  $I_{ds}-V_{gs}$  memory window after  $\pm 8$  V, 0.01  $\mu$ s programming pulse is 1.6 V. The  $V_{th}$  shift of the MYTOS transistors at an applied gate voltage of 6 V with a pulse width of 10 ns is about 1.0 V. As for retention properties, the MYTOS transistors are projected to have a  $\Delta V_{th}$  window of 0.81 V after 10 years. The excellent performance of the MYTOS transistors is most likely due to the larger conduction band offset at the  $Ta_2O_5/SiO_2$  and the  $Y_2O_3/Ta_2O_5$  interfaces and the large dielectric constant of  $Y_2O_3$ .

## Conflict of Interests

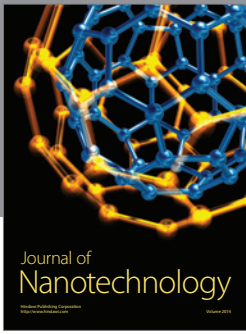
The authors declare that there is no conflict of interests regarding the publication of this paper.

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