A new CMOS voltage reference scheme based on Vth-difference principle

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***Abstract*— a new CMOS voltage reference, which takes advantage of the temperature dependence of NMOS and PMOS threshold voltages, is presented. Due to the circuit architecture the mobility factor is completely cancelled. It does not use resistors and all transistors works in strong inversion. The circuit is simple, opamp-less and can be implemented in a standard CMOS process. When the input power supply changes from 1.8V to 2.1V and the temperature changes from -20 to 80ºC, simulations for the reference circuit using the proposed architecture shows an output voltage of 1.184V and a T_{FC} of 100 ppm/ºC.**

I. INTRODUCTION

References are intrinsically required by circuits such as biasing circuits, digital-to-analog converters, analog-to-digital converters and operational amplifiers. These building blocks are the basic elements that make up phones, computers and many other popular electronics products. For this reason, much research has been conducted and is still continuing in order to improving reference circuits. Generally speaking, reference circuits based on BJT technology have put emphasis in improving accuracy by implementing second or higher order temperature compensation schemes [1][2], while the development of CMOS circuits has focused more on low voltage applications [3][4]. The design objective of this work is to propose a novel structure that can be implemented in low cost CMOS technology and with performance comparable to the performance of the bandgap voltage reference. The proposed CMOS reference circuit has the potential to establish a reference voltage for analog-to-digital and digital-to-analog converters and to provide a biasing voltage for other circuits that is insensitive to the power supply and temperature. Section II provides a detailed analysis of the temperature characteristics of MOS transistors, which are the basic elements of the reference circuit used in this work. Section III has a more practical engineering orientation. First, the proposed voltage reference is presented. The concept of the reference circuit is described and analyzed to derive the equations governing its functioning. An example of the proposed design and simulation results are presented in Section IV and the conclusions are given in Section V.

II. THEORY REVIEW

A. Temperature dependence of MOS transistors

To successfully design a CMOS current/voltage reference, one must have a thorough understanding of the temperature behavior of MOS transistors. The threshold voltage and the mobility are the main temperature-dependent parameters. As the temperature increases, both the threshold voltage and the mobility decrease. But the decrease of V_{TH} and the decrease of μ have opposite effects on the drain current; a lower threshold voltage tends to increase the drain current, but a lower mobility tends to decrease it. It has been shown in [5] that the threshold voltage decreases approximately linearly with an increase in temperature. The temperature dependency of the threshold voltage usually used is:

$$V_{TH}(T) = V_{TH}(T_0) - \alpha_{VT}(T - T_0) \tag{1}$$

where α_{VT} is the temperature coefficient of the threshold voltage. The value of α_{VT} varies from 1mV/ºC to 4mV/ºC, it is technology dependent and differs from a NMOS to a PMOS transistor. On the other hand, a general expression which is used to describe the temperature dependency of the mobility is given by:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{2}$$

where $\mu(T_0)$ is the mobility at the reference temperature, T_0, and $1 \le m \le 2.5$.

B. Mobility cancellation

Since mobility is a nonlinear function of temperature, it is difficult to build voltage references that rely on MOS

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characteristics [3]; it is not easy to obtain a low TC reference voltage by canceling mobility with a linear voltage (Vth). This is the same problem as in the traditional bandgap voltage reference where a PTAT voltage is used to cancel a nonlinear voltage of V_{BE}. It is obvious that the curvature comes from the nonlinear temperature dependence of mobility. Reference [6] uses a voltage that is inversely proportional to mobility to cancel it. Nevertheless, the mobility factor can be totally cancelled if transistors NMOS are not combined with the PMOS in a same branch. This mobility cancellation idea is intuitive. While the intuition has the advantage of understanding the operation of a circuit without have to describe it in equations, mathematical analysis can find the exact relationship among variables from equations. This intuitive idea is developed into a voltage reference design. In the mathematical analysis of the circuit, it is revealed how the mobility is eliminated to avoid the temperature dependency contribution on Vref caused by it.

III. CIRCUIT IMPLEMENTATION

For voltage references in a CMOS process, one obvious design method is to emulate that of the well known bipolar reference designs. However, independent bipolar transistors are not available in a standard CMOS process. Most previous CMOS voltage references use the bandgap architecture and their performances are limited due to the poor performance of the well transistors in CMOS process. The CMOS bandgap voltage reference designs also suffer from the weaknesses of a large amplifier offset. There are many methods to minimize the effects of the offset voltage. In this design, the op amp is eliminated to avoid the offset, drift, chip area and power consumption associated with it. In this section, a different architecture for voltage references is proposed. The proposed architecture is based on the threshold voltage difference principle [6] [7] and no parasitic transistors are used.

The principle of the circuit relies on two independent groups of NMOS and PMOS as shown in Fig. 1. Observe that resistors are not used and its temperature dependence is avoided [8] [9]. If the mobility is cancelled, the only dependency with the temperature comes from the threshold voltage.

For example, for the two threshold voltages V_{THN} and V_{THP} that vary in the same direction with temperature (but different in magnitude), we choose k_1 and k_2 so as to accomplish:

$$k_1 \frac{\partial V_{THN}}{\partial T} - k_2 \frac{\partial V_{THP}}{\partial T} = 0 \cdot \tag{3}$$

In this way, a reference voltage is given by:

$$V_{REF} = k_1 V_{THN} - k_2 V_{THP} \tag{4}$$

Both V_{THN} and V_{THP} have negative TCs, but they are different in value. Hence, they can be subtracted with different weighting factors to form a near zero-TC output voltage. The voltage reference is fully compatible with standard digital CMOS processes and gives moderate temperature performance.

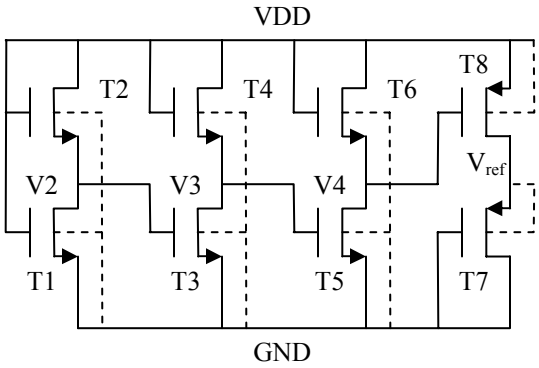

Fig.1. Voltage reference circuit

A. Operation

To provide a qualitative understanding of the circuit behavior, the circuit can be analyzed using a simple square-law MOS model. The circuit of Fig. 1 operates as follows; transistors T_2, T_3 and T_4 are saturated and T_1 works in the triode region. The effect of supply-voltage variations is twofold. Suppose V_{DD} increases. First, since the currents of T_1 and T_2 are the same, the gate-source voltage of T_1 will increase proportional to the increase in V_{DD}. Therefore the voltage V_2 will also increase proportionally. Secondly, the gate-source voltage of T_3 increases with V_{DD} due to its gate is connected to V_2. Therefore, despite the body effect, its drain current will increase proportionally with the increase in V_{DD}. The circuit is designed so that the required increase in current through T_3 is provided by the increase in T_4′s current. As a result V_3 will remain constant with changing V_{DD}. Transistors T_5 and T_6 (both are saturated) have to convert from a supply-independent threshold-referenced NMOS voltage (V_3) relative to ground to a voltage relative to V_{DD}. The final result is that V_{DD}–V_4 will remain constant with changing V_{DD} for a given range of values.

Transistor T_7 and T_8 will act as a subtractor of both V_{THN} and V_{THP} which have different weighting factors to form a reference voltage.

Due to Body effect affects the group of NMOS transistors, it is necessary to change slightly the relationship between sizes of transistors in order to reach a true independence of V_{DD}. The PMOS transistors are on different wells so they are insensitive to Body effect.

B. Equations

It can be demonstrated that, considering body effect, the voltages V_2, V_3 and V_4 are:

$$V_2 = \frac{(V_{DD} - V_{THN})}{\delta}\left(1 - \sqrt{\frac{\beta_1}{1+\beta_1}}\right) \tag{5}$$

$$V_3 = \frac{(V_{DD} - V_{THN})}{\delta}\left[1 - \frac{\sqrt{\beta_2}}{\delta}\left(1 - \sqrt{\frac{\beta_1}{1+\beta_1}}\right)\right] + \frac{\sqrt{\beta_2}V_{THN}}{\delta} \quad (6)$$

$$V_4 = \frac{(V_{DD} - V_{THN})}{\delta} - \frac{\sqrt{\beta_3}}{\delta}\frac{(V_{DD} - V_{THN})}{\delta} + \frac{\sqrt{\beta_3}}{\delta}\frac{(V_{DD} - V_{THN})}{\delta}\frac{\sqrt{\beta_2}}{\delta}\left(1 - \sqrt{\frac{\beta_1}{1+\beta_1}}\right) - \frac{\sqrt{\beta_3}}{\delta}\frac{\sqrt{\beta_2}}{\delta}V_{THN} + \frac{\sqrt{\beta_3}}{\delta}V_{THN} \quad (7)$$

where $\beta_1 = \frac{(W/L)_1}{(W/L)_2}$, $\beta_2 = \frac{(W/L)_3}{(W/L)_4}$, and $\beta_3 = \frac{(W/L)_5}{(W/L)_6}$.

The constant δ which accounts for the body effect is approximately 1.36 for the 1.5 µm AMI Technology. If the conditions $\frac{\sqrt{\beta_3}}{\delta} = 1$ and $\frac{\sqrt{\beta_2}}{\delta} = \frac{\delta}{1 - \sqrt{\frac{\beta_1}{1+\beta_1}}}$ are fulfilled, then

$$V_4 = V_{DD} - \frac{\sqrt{\beta_2}}{\delta}V_{THN} \quad (8)$$

As expected, the voltage V_4 is relative to the supply voltage but still a linear function of temperature. Finally, the voltage of Vref is calculated as:

$$V_{ref} = \frac{\frac{\sqrt{\beta_2}}{\delta}V_{THN} - \left(1 - \sqrt{\beta_4}\right)V_{THP}}{\sqrt{\beta_4}} \quad (9)$$

where $\beta_4 = \frac{(W/L)_7}{(W/L)_8}$.

The temperature coefficient of Vref can be derived by differentiating (9) with respect to temperature and is given by:

$$\frac{\partial V_{ref}}{\partial T} = \frac{-\frac{\sqrt{\beta_2}}{\delta}\alpha_{vthn} + \left(1 - \sqrt{\beta_4}\right)\alpha_{vthp}}{\sqrt{\beta_4}} \quad (10)$$

where α_{vthn} and α_{vthp} are the temperature coefficients for the threshold voltages of a NMOS and PMOS transistors respectively. To obtain $\frac{\partial V_{ref}}{\partial T} = 0$, the ratio of temperature coefficients must be equal to:

$$\frac{\alpha_{vthp}}{\alpha_{vthn}} = \frac{\frac{\sqrt{\beta_2}}{\delta}}{1 - \sqrt{\beta_4}} \quad (11)$$

All equations show that the voltage reference and its temperature coefficient can be determined by circuit parameters.

IV. Design Example and Simulations Results

The circuit shown in Fig. 1 was designed for realization in 1.5 µm AMI Technology using the BSIM3v.3 MOS model. The dimensions of transistors used for simulation are indicated in table 1. Long-channel devices are chosen in order to minimize channel-length modulation effect.

TABLE I. Device sizes

Transistors	Size [µM/µM]
T1	12/54.8
T2	54.8/12
T3	24.5/12
T4	12/24.5
T5	16.3/12
T6	12/16.3
T7	12/40
T8	40/12

The temperature behavior is shown in Fig. 2. When the input power supply changes from 1.8V to 2.1V and the temperature changes from -20 to 80ºC, simulations for the reference circuit using the proposed architecture shows an output voltage of 1.184V and a *TFC* of 100 ppm/ºC. The PSRR for a 1.9V supply voltage, without using a filtering capacitor to improve the high-frequency behavior, is shown in Fig. 3.

V. Conclusions

A novel CMOS reference voltage scheme was presented. A startup circuit commonly present in other configurations is not necessary. In standard digital CMOS technologies, models for the resistors may not be available or reliable. For this reason it is advantageous to avoid them. The proposed circuit does not use resistors. This reference is suitable for standard low-cost CMOS technologies since additional fabrication steps are not needed. The devices operate in strong inversion, for which accurate device models are usually available, simplifying the design procedure, especially in digital CMOS technologies. Mobility compensation is not necessary. Since the NMOS transistors are not combined in the same branch with PMOS transistors the mobility factor is completely cancelled.

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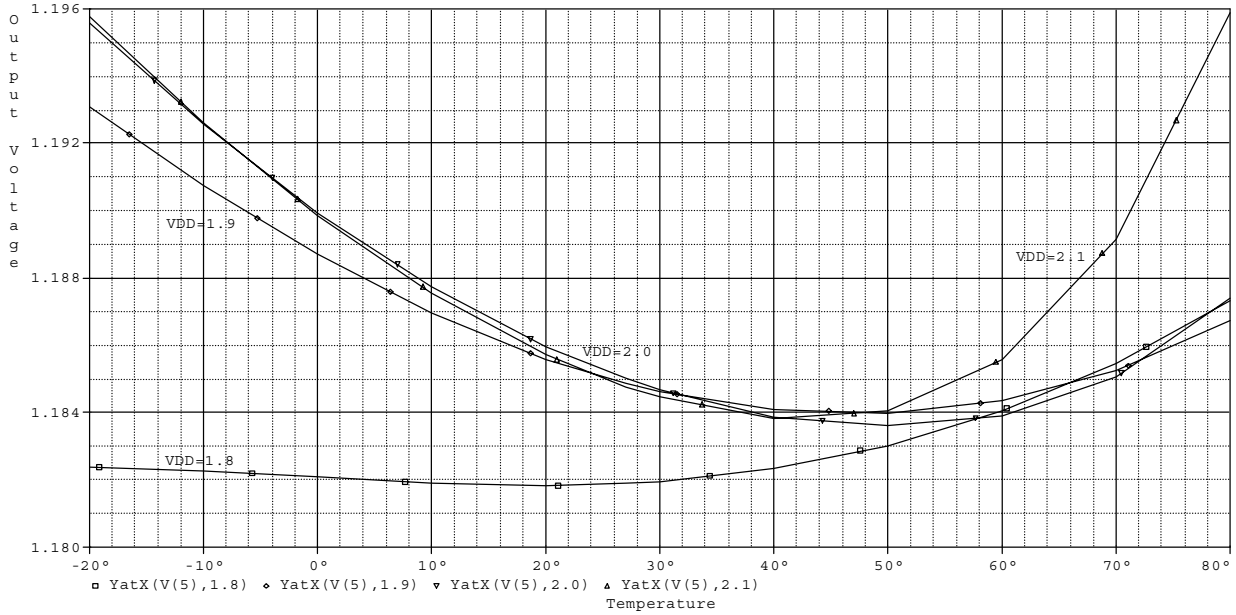

Fig.2. Output voltage vs. Temperature for different VDD

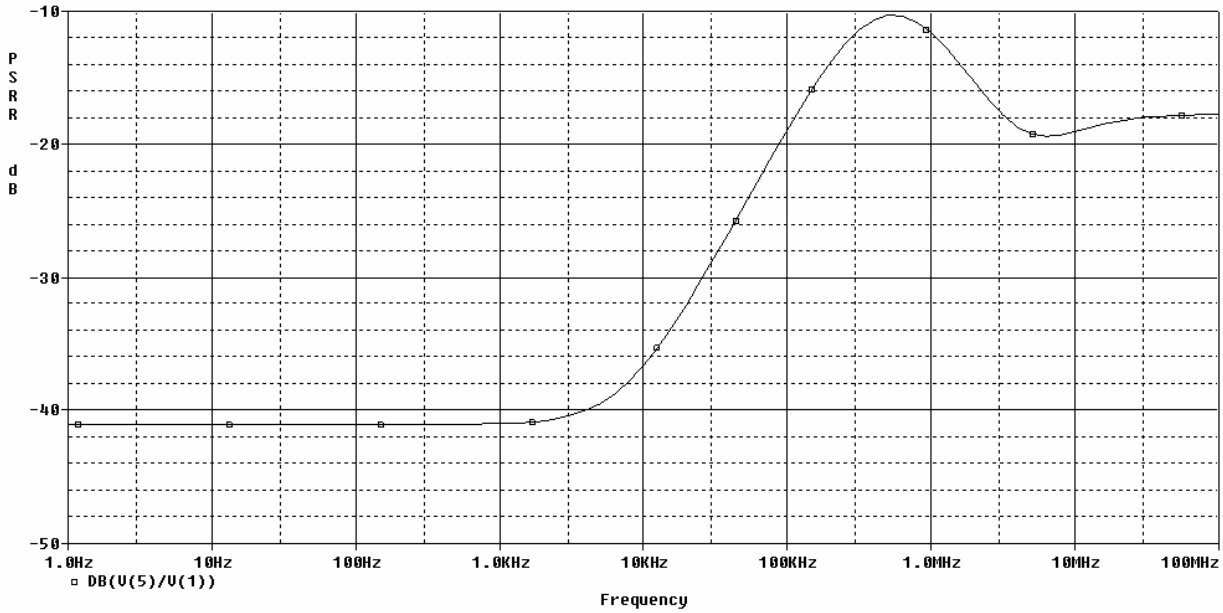

Fig.3. PSRR of the proposed voltage reference for a 1.9V power supply