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Research Article

A Low-Power Ultrawideband Low-Noise Amplifier in 0.18 μm CMOS Technology

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This paper presents an ultrawideband low-noise amplifier chip using TSMC 0.18 μm CMOS technology. We propose a UWB low noise amplifier (LNA) for low-voltage and low-power application. The present UWB LNA leads to a better performance in terms of isolation, chip size, and power consumption for low supply voltage. This UWB LNA is designed based on a current-reused topology, and a simplified RLC circuit is used to achieve the input broadband matching. Output impedance introduces the LC matching method to reduce power consumption. The measured results of the proposed LNA show an average power gain (S_{21}) of 9 dB with the 3 dB band from 3 to 5.6 GHz. The input reflection coefficient (S_{11}) less than −9 dB is from 3 to 11 GHz. The output reflection coefficient (S_{22}) less than −8 dB is from 3 to 7.5 GHz. The noise figure 4.6–5.3 dB is from 3 to 5.6 GHz. Input third-order-intercept point (IIP_3) of 2 dBm is at 5.3 GHz. The dc power consumption of this LNA is 9 mW under the supply of a 1 V supply voltage. The chip size of the CMOS UWB LNA is 1.03×0.78 mm^2 in total.

1. Introduction

The ultrawideband (UWB) system has become one of the major technologies for wireless communication systems and local area networks. The IEEE 802.15.3a ultrawideband (UWB) system uses a specific frequency band (3.1 GHz~ 10.6 GHz) to access data and employs the system of orthogonal frequency-division multiplexing (OFDM) modulation [1–3]. The frequency band consists of four groups: A, B, C, and D, with thirteen channels. Each channel bandwidth is 528 MHz, as shown in Figure 1. The system operates across a wide range of frequency 3.1–5 GHz or 3.1–10.6 GHz. The low frequency band from 3.1 to 5 GHz has been allocated for developing the first generation of UWB systems [4]. The system has several advantages such as low complexity, low cost, and a high data rate for the wireless system. In the front-end system design, a low-noise amplifier (LNA) is the first block in the receiver path of a communication system. The chief objective of the LNA is to reach the low-noise figure to improve the overall system noise [5]. The LNA must minimize the noise figure over the entire bandwidth, feature flat gain, good linearity, wideband input-output matching, and low power consumption. In the radio frequency circuit design, GaAs and bipolar transistors have performed fairly well. Nevertheless, these processes lead to increased cost and greater complexity. The RF front-end circuits using CMOS technology can provide a single-chip solution, which greatly reduces the cost [6]. With the rapid improvement of CMOS technology, it can implement RF ICs with CMOS. Three major topologies of the present wideband low-noise amplifiers are used. First, distributed amplifiers [7–9] can provide good linearity and wideband matching but require high power consumption and a large chip area because of the multiple amplifying stages. Second, resistive shunt feedback amplifiers [4, 10] provide good wideband matching and flat gain but require high power consumption. Last, Chebyshev filter amplifiers [11, 12] adopt a wideband LC bandpass filter for input matching and a source follower for output matching. This type of wideband amplifier dissipates a small amount of dc power. The Chebyshev filter matching design requires three inductors. Therefore, a very large chip area is required. This paper proposes RLC broadband matching for LNA design. The primary goal is to obtain wideband input-output matching and to reduce the chip area and power consumption. The LNA topology is

proposed in Section 2. The complete analysis of the design methodology of the wideband matching network is presented in Section 3. In Section 4, implementation and measurement results are presented. The conclusion is presented in the last section.

2. Low-Voltage Wideband Cascode LNA Design

Figure 2 shows the basic cascode LNA. The current-reused configuration can be considered as two common-source amplifiers (M_1 and M_2). The current shared cascode amplifier provides a low-power characteristic under the low voltage supply. Because M_1 and M_2 share the same bias current, the total power consumption is minimized [6, 12, 16]. For a cascode amplifier, the overall noise figure can be obtained in terms of the noise figure (NF) and gain of each stage as follows:

$$F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_{A1}}, \tag{1}$$

where F_{total} is the total NF and F_1 and F_2 are the NF values of the first and second stage; respectively. G_{A1} is the power gain of this first stage, therefore, in the LNA circuits, the noise of the first stage is more critical. Consequently, the gain of the transistor's M_1 must be high enough to suppress the noise. The dominant noise sources for active MOSFET transistors are flicker and thermal noises. The flicker noise is modeled as the voltage source in series with the gate of value:

$$\overline{V_g^2(f)} = \frac{K}{WLC_{ox}f}, \tag{2}$$

where the constant K is dependent on device characteristics and can vary widely for different devices in the same process. The variables W, L, and C_{ox} represent the width, length, and gate capacitance per unit area, respectively. The flicker noise is inversely proportional to the transistor area, WL. In other words, a larger device reduces this noise. The noise process of thermal noise is random. The MOSFET thermal noise includes three main noise sources, as shown in Figure 3: distributed gate resistance noise ($\overline{V_{\text{rg}}^2}$), drain current noise ($\overline{i_{\text{nd}}^2}$), and gate current noise ($\overline{i_{\text{nd}}^2}$).

The thermal noise source mainly comes from the drain current noise and gate-induced noise of the transistors. Multifinger layout technology is applied to reduce the gate-induced noise. According to the MOSFET noise analysis in [17, 18], we must express the noise figure in a way that explicitly considers power consumption. In order to determine the width of M_1 and find out the best NF, we use the dependency among noise factor (F), power dissipation (PD), and quality factor (Q_L) to find out the optimal value [17]. Based on these parameters, the related curves, NF (dB) versus Q_L, are plotted in Figure 4 by MATLAB simulation software. There is a compromise between noise performance and power gain in Figure 4. Therefore, the Q_L can be determined to be 4, as PD equals to 10 mW. The optimal width of MOSFET can be obtained by [17, 18]:

$$W_{\text{opt}} = \frac{3}{2}\frac{1}{\omega_o LC_{ox}R_S Q_L} \approx \frac{1}{3\omega_o LC_{ox}R_S}, \tag{3}$$

where ω_o is the operation frequency, L is the gate length, and C_{ox} is the gate capacitance per unit area. Equation (3) shows that the optimal width for M_1 is 240 μm, for $\omega_o = 3.4$ GHz, $L = 0.18$ μm, $C_{ox} = 8.62$ F/m^2, $R_S = 50\Omega$, and $Q_L = 4$.

Figure 5 shows the proposed UWB LNA schematic. The current sharing cascode amplifier provides low-power characteristics with low voltage supply. Note that M_2 is the common-gate stage of the cascode configuration, which eliminates the Miller effect and provides better isolation from the output return signal [18, 19]. The passive components C_1, C_2, C_3, R_1, and L_1 are adopted for the matching network at the input to resonate over the entire frequency band. The resistors R_2 and R_g are used to provide bias voltage for the transistors M_1 and M_2. The capacitor C_4 provides signal coupling between the two stages. The capacitor C_5 bypasses the ac current to the ground and avoids coupling to the first stage. This affects gain flatness; therefore, it is possible to provide an ideal ac ground, but gain flatness is not affected in the design. L_2 is the inductor load of the first stage. The output matching network is composed of L_3, L_4, C_6, and C_7. In the cascode stages, the first stage's noise figure contribution is more than the second stage's. The first stage's transistor size and bias point should be optimized for the low NF [17]. The second stage's transistor size and bias point should be optimized for high linearity. The cascode LNA design is full of trade-offs between optimal gain, low noise figure, input and output matching, linearity, and power consumption. Moreover, to avoid oscillation, the parasitic couplings have to be minimized [16]. The sizes of the devices of the LNA are shown in Table 1.

3. Proposed Wideband Matching Network Analysis

3.1. Input Impedance Matching. As shown in Figure 2, in the conventional narrow band LNA design, the input impedance of the input stage (M_1) can be written as

$$Z_{\text{in}} = s\left(L_g + L_S\right) + \frac{1}{sC_{\text{gs1}}} + \left(\frac{g_{m1}}{C_{\text{gs1}}}\right)L_s, \tag{4}$$

where C_{gs1} is the gate-source capacitance and g_{m1} is the transconductance of the input transistor M_1. We choose appropriate values of inductance ($L_g + L_s$) and capacitance C_{gs1}, which resonate at a certain frequency. The real term can be made equal to 50 Ω. Equation (3) determines the width of M_1 and finds the best NF. For wideband design, it is difficult to let the imaginary part of (4) remain zero for a wide range. To discuss UWB input impedance matching, we need to consider the standard form of the second-order filter:

$$T(S) = \frac{a_2S^2 + a_1S + a_o}{S^2 + S\left(\omega_o/Q_{\text{in}}\right) + \omega_o^2} = \frac{a_2S^2 + a_1S + a_o}{S^2 + \text{SB} + \omega_o^2}, \tag{5}$$

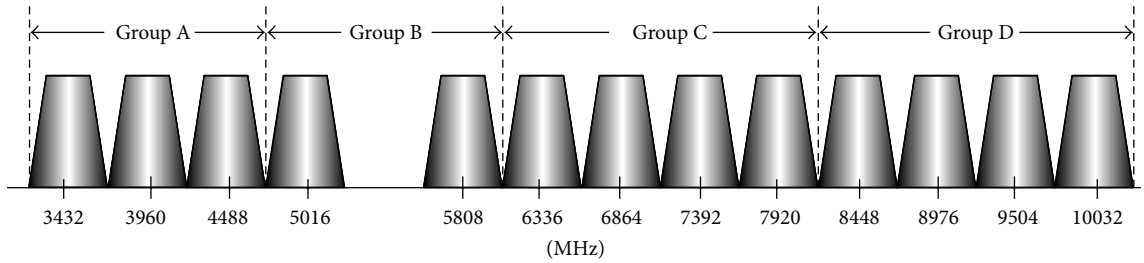

Figure 1: The IEEE 802.15.3a spectrum.

Table 1: Device sizes of the proposed UWB LNA.

Device	C_1 (pF)	C_2 (pF)	L_1 (nH)	C_3 (pF)	R_1 (kΩ)	R_g (kΩ)	C_4 (pF)	L_2 (nH)	C_5 (pF)	R_2 (kΩ)	L_3 (nH)	L_4 (nH)	C_6 (pF)	C_7 (pF)	M_1-M_2 (μm)
Size	9.51	0.11	0.91	7.6	0.14	3.84	5.7	5.53	5.7	3.84	1.19	0.59	0.16	1.23	240/0.18

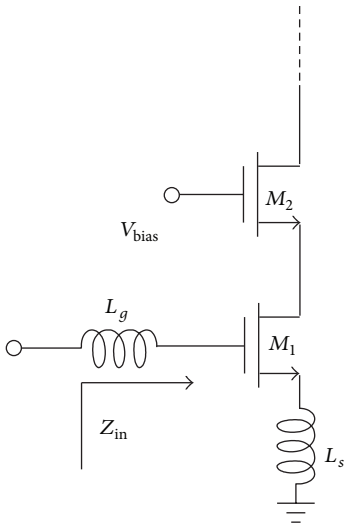

Figure 2: Cascode low noise amplifier.

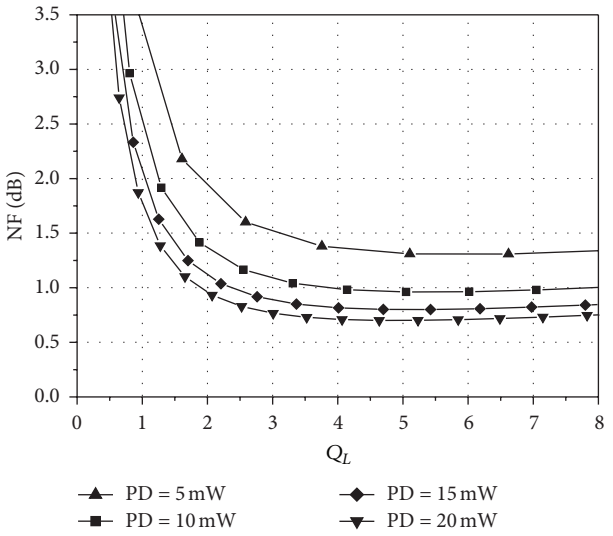

Figure 4: Noise Figure versus Q_L for several power dissipations at 3.4 GHz.

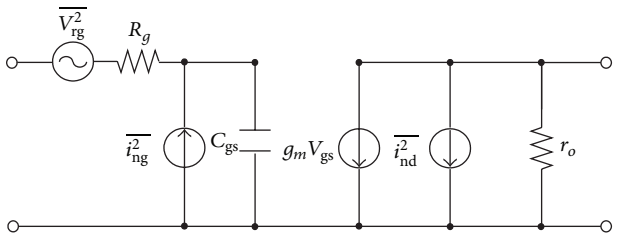

Figure 3: CMOS noise model.

where a_2, a_1, and a_o are numerator coefficients determining the type of second-order filter function. ω_o is called the pole frequency, Q_{in} is termed the pole factor, and B is called bandwidth. According to $B = \omega_o/Q_{in}$, the bandwidth is inversely proportional to the Q_{in} if the value of the pole frequency ω_o is fixed.

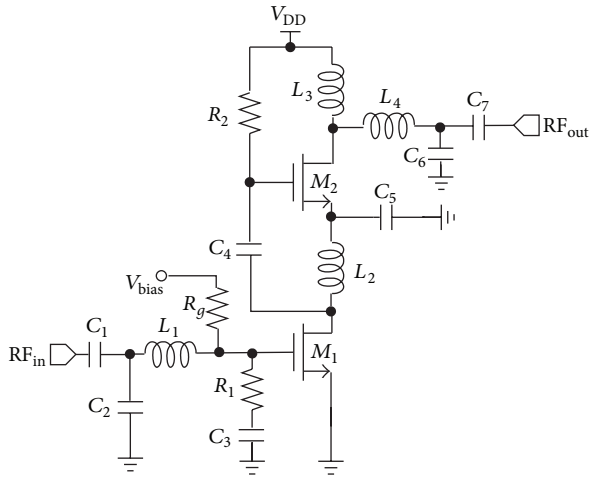

Figure 5: Schematic of the proposed UWB LNA.

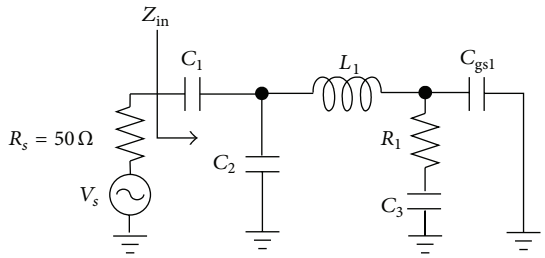

FIGURE 6: The proposed wideband matchingapproximate first stage input matching small-signal equivalent circuit.

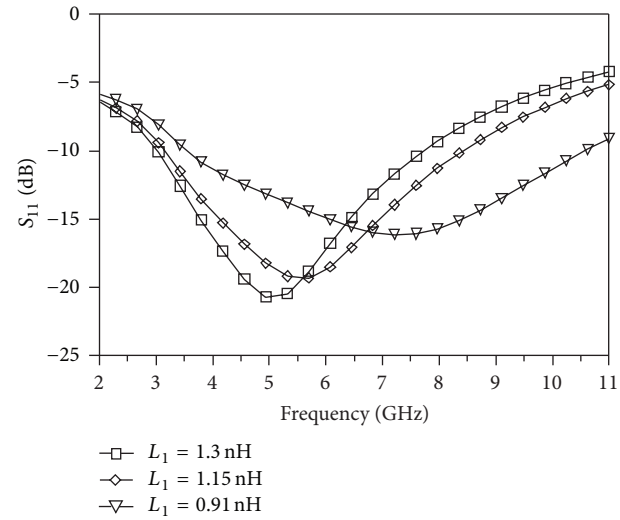

FIGURE 7: Fixed C_1, C_2, C_3 and R_1 and simulated L_1 variation input reflection coefficient.

Figure 6 shows the proposed wideband matching and a small-signal equivalent circuit in the first stage. The input impedance of the RLC network can be written as

$$Z_{\text{in}} = \frac{1}{SC_1} + \frac{1}{SC_2} // \left[SL_1 + \left(R_1 + \frac{1}{SC_3} \right) // \frac{1}{SC_{\text{gs1}}} \right] = R_{\text{in}} + jX_{\text{in}}. \quad (6)$$

Because C_3 capacitance value is much larger than C_{gs}($C_3 \gg C_{\text{gs}}$), the $(R_1 + (1/SC_3))//(1/SC_{\text{gs1}})$ will approximate $(R_1 + (1/SC_3))$:

$$Z_{\text{in}} = \frac{1}{SC_1} + \frac{1}{SC_2} // \left(SL_1 + \left(R_1 + \frac{1}{SC_3} \right) \right) = R_{\text{in}} + jX_{\text{in}},$$
$$Z_{\text{in}} \approx \frac{\left(S + \left(R_1/L_1 \right) \right) \left(\left(C_1 + C_2 \right)/C_1C_2 \right)}{S^2 + S\left(R_1/L_1 \right) + \left(\left(C_2 + C_3 \right)/L_1 \left(C_2C_3 \right) \right)}, \quad (7)$$

where C_{gs1} is the gate-source capacitance of M_1. This equivalent circuit can roughly be an RLC second-order filter structure. In (7), the quality factor of the filter circuit can be given by

$$f_o \approx \frac{1}{2\pi} \sqrt{\frac{C_2 + C_3}{L_1 \left(C_2C_3 \right)}}, \quad (8)$$

$$Q \approx \frac{1}{R_1} \sqrt{\frac{L_1 \left(C_2 + C_3 \right)}{C_2C_3}}, \quad (9)$$

where f_o is the resonant frequency. In (8) and (9), to obtain broader bandwidth, a low-quality factor needs to be added to the passive devices. The narrowband LNA can be converted into a wideband amplifier by properly selecting passive devices. According to (8), the capacitors C_2, C_3 and inductor L_1 will be optimized at the resonant frequency. We use the CAD of Agilent ADS to analyze the circuit performance of input impedance matching. According to (8) and (9), f_o is inversely proportional to L_1 while Q is proportional to L_1. Therefore, bandwidth is inversely proportional to L_1. Figure 7 is fixed as C_1 (9.51 pF), C_2 (0.11 pF), C_3 (7.6 pF), and R_1 (140 Ω), showing that the resonant frequency is inversely proportional to the L_1. Bandwidth is inversely proportional to L_1. According to (9), the input matching circuit uses R_1 and C_3 to reduce the number of inductors and make the Q factor smaller. Q is inversely proportional to R_1. Therefore, bandwidth is proportional to R_1. Figure 8 is fixed as C_1 (9.51 pF), C_2 (0.11 pF), C_3 (7.6 pF), and L_1 (0.91 nH), showing that the bandwidth is proportional to the R_1. Figure 9 is fixed as C_1 (9.51 pF), C_2 (0.11 pF), C_3 (7.6 pF), and L_1 (0.91 nH), showing that the noise figure is inversely proportional to the R_1. f_o is inversely proportional to C_3 while Q is inversely proportional to C_3. Therefore, the bandwidth is proportional to the C_3. Figures 10 and 11 are fixed as C_1 (9.51 pF), C_2 (0.11 pF), R_1 (140 Ω), and L_1 (0.91 nH), showing that the bandwidth and noise figure are proportional to the C_3. The size of the transistors M_1, R_1, and C_3 must be carefully selected. There is a trade-off in the design between wideband matching and the noise figure. On the other hand, the device size must yield a sufficient noise performance and power gain. As can be seen, the second-order filter of L_1 (0.91 nH), R_1 (140 Ω), and C_3 (7.6 pF) is employed as the input matching network. The input matching network has less complexity and better reflection coefficient from 3 GHz to 10 GHz.

3.2. Output Impedance Matching. Low-noise amplifiers rely on output impedance matching to achieve maximum power gain. A source follower technique has been widely used to provide wideband output matching. Output impedance is similar to $1/g_{ms}$, in which g_{ms} is a gate-source transconductance of the source follower [4, 10]. However, it consumes more power. For these reasons, we introduce an output impedance matching method suitable for wideband LNA design. Figure 12 shows the approximate output impedance small-signal equivalent circuit. The output impedance of the RLC network can be written as

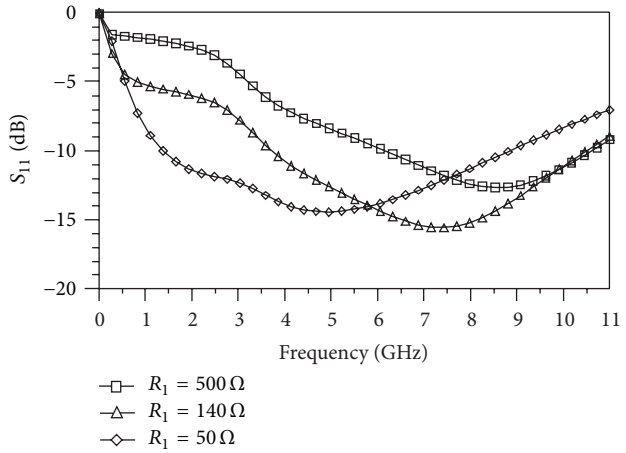

Figure 8: Fixed C_1, C_2, C_3, and L_1 and simulated R_1 variation input reflection coefficient.

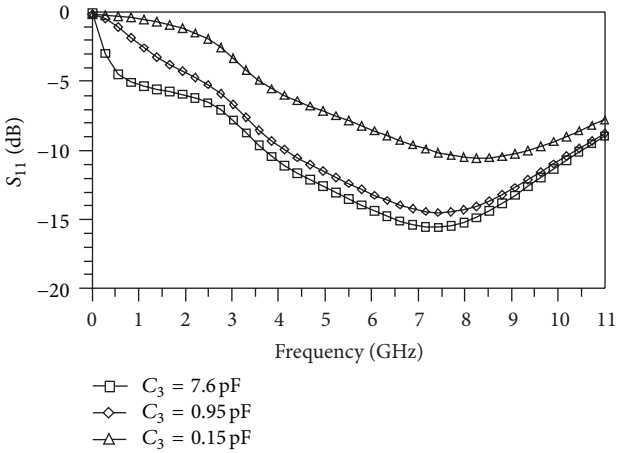

Figure 10: Fixed C_1, C_2, R_1, and L_1 and simulated C_3 variation input reflection coefficient.

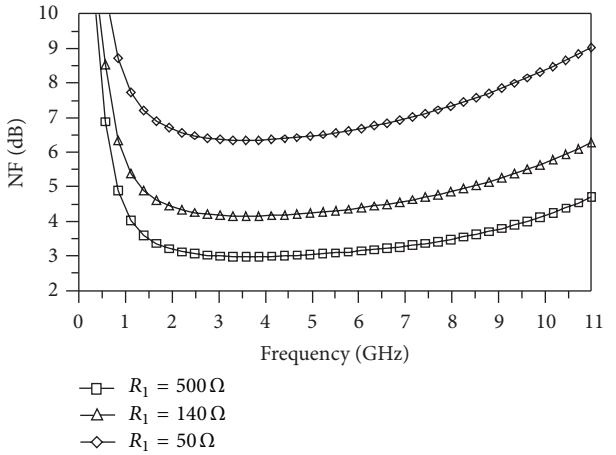

Figure 9: Fixed C_1, C_2, C_3, and L_1 and simulated R_1 variation noise figure.

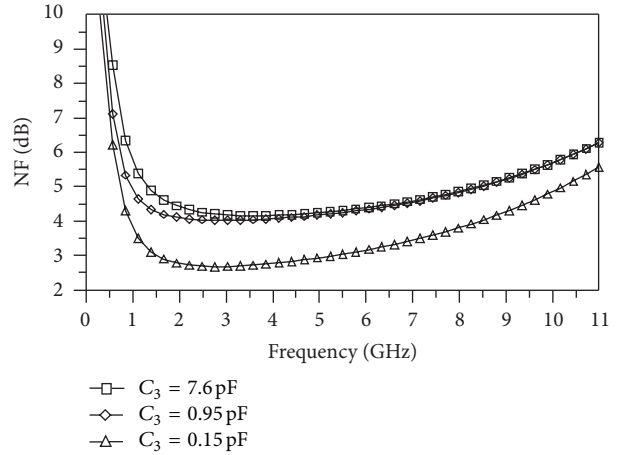

Figure 11: Fixed C_1, C_2, R_1, and L_1 and simulated C_3 variation noise figure.

$$Z_{\text{out}} = \left(\left(r_{d2} // \frac{1}{SC_{d2}} // SL_3\right) + SL_4\right) // \frac{1}{SC_6} + \frac{1}{SC_7} = R_{\text{out}} + jX_{\text{out}}, \tag{10}$$

$$Z_{\text{out}} \approx \frac{\left(S + \left(1/r_{d2}C_{d2}\right)\right)\left(\left(C_7 + C_6\right)/C_6C_7\right)}{S^2 + S\left(1/r_{d2}C_{d2}\right) + \left(\left(C_6L_4 + C_6L_3 + C_{d2}L_3\right)/C_{d2}C_6L_3L_4\right)}, \tag{11}$$

where C_{d2} is the parasitic capacitance of M_2 at the drain node, and r_{d2} is the resistor of M_2 at the drain node. This equivalent circuit can approximately be an RLC second-order filter structure. In (11), the quality factor of the filter circuit can be given by

$$f_o \approx \frac{1}{2\pi}\sqrt{\frac{C_6L_4 + C_6L_3 + C_{d2}L_3}{C_{d2}C_6L_3L_4}}, \tag{12}$$

$$Q \approx r_{d2}C_{d2}\sqrt{\frac{C_6L_4 + C_6L_3 + C_{d2}L_3}{C_{d2}C_6L_3L_4}}, \tag{13}$$

where f_o is the resonant frequency. In (12) and (13), in order to obtain broader bandwidth, a low-quality factor needs to be added to passive devices. f_o is inversely proportional to C_{d2} while bandwidth is inversely proportional to $r_{d2}C_{d2}$. The C_{d2} capacitance is proportional to the width of the transistor. The r_{d2} resistance is inversely proportional to the width of the transistor. UWB system uses a specific frequency band

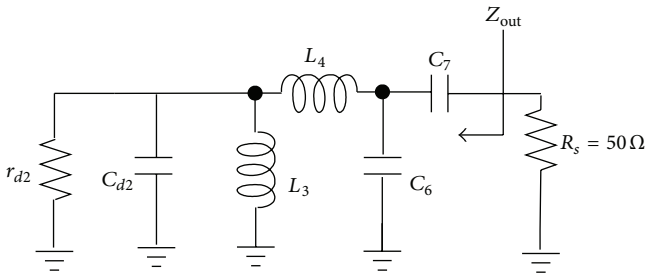

Figure 12: The wideband output matching small-signal equivalent circuit.

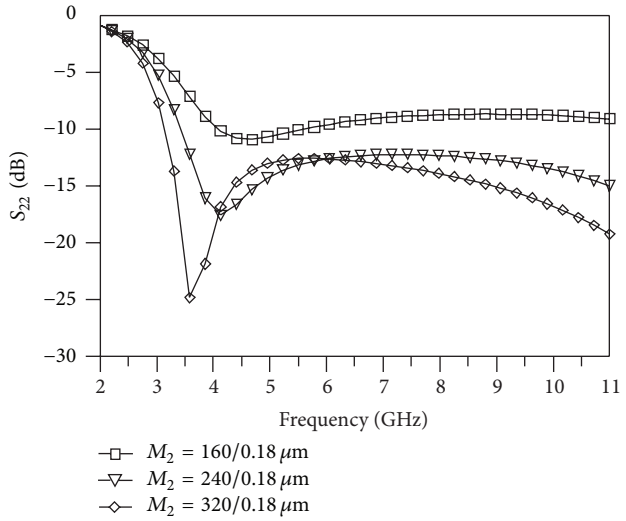

Figure 13: Fixed C_6, C_7, L_3 and L_4, simulated M_2 variation output reflection coefficient.

(3.1–5 GHz or 3.1–10.6 GHz) to access data. Generally the results of UWB return loss are less than −10 dB. The power consumption is proportional to the width of the transistor. According to (13), the narrowband LNA can be converted into a wideband amplifier by properly selecting M_2. This provides good wideband matching and flat gain. Figure 13 is fixed as C_6 (0.16 pF), C_7 (1.23 pF), L_3 (1.19 nH), and L_4 (0.59 nH), showing that the simulated M_2 variation output reflection coefficient. As can be seen, the second-order filter of M_2 (240/0.18 μm) is employed as the output matching network. According to (12), the capacitor C_6 and inductor L_3-L_4 will be optimized at the resonant frequency. Figure 14 is fixed as C_6 (0.16 pF), C_7 (1.23 pF), M_2 (240/0.18 μm), and L_4 (0.59 nH), showing that the resonant frequency is inversely proportional to the L_3. The output network has less complexity and a better reflected coefficient from 3.1 GHz to 10.6 GHz.

3.3. Gain. At a high frequency, the current gain of common source configured transistor M_1 is g_{m1}/sC_{gs1} [11]. Figure 15 shows the approximate first stage M_1 load of the simplified

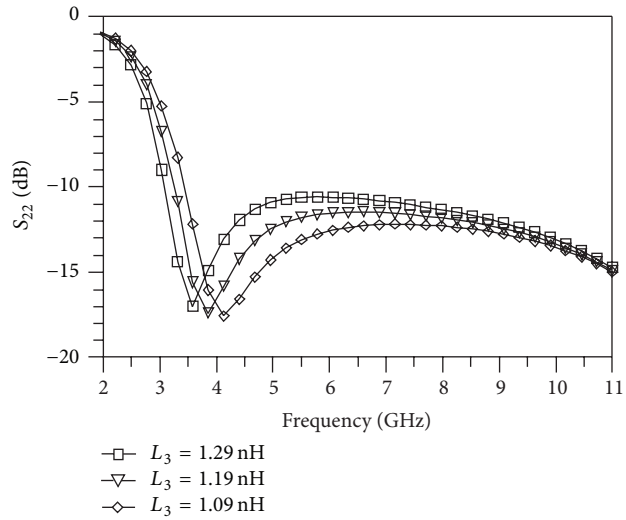

Figure 14: Fixed C_6, C_7, M_2, and L_4 and simulated L_3 variation output reflection coefficient.

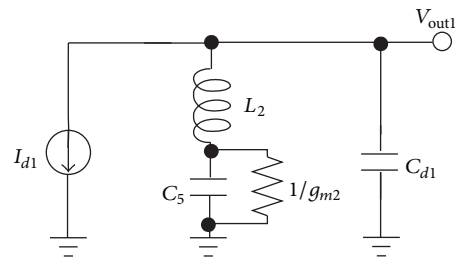

Figure 15: The first stage simplified small-signal equivalent circuit.

small-signal equivalent circuit [12]. The first stage load can be approximated as

$$Z_{\text{load1}} \approx \frac{1}{SL_2C_5C_{d1}} \cdot \frac{S^2L_2C_5 + Sg_{m2}L_2 + 1}{S^2 + S\left(g_{m2}/C_5\right) + \left(\left(C_5 + C_{d1}\right)/\left(L_2\left(C_5C_{d1}\right)\right)\right)}. \quad (14)$$

The transfer function of the input matching network is $Z_{\text{in}}(s)$. The first stage voltage gain can be approximated as

$$A_{V1} \approx -\frac{g_{m1}Z_{\text{in}}}{SC_{\text{gs1}}R_s} \cdot Z_{\text{Load1}}, \quad (15)$$

where R_s is the source resistance, in which voltage gain is determined by the load inductor L_2, the total capacitance at the drain of M_1, and bypass capacitor C_5. The second stage voltage gain can be estimated as

$$A_{V2} \approx -\frac{g_{m2}}{SC_{\text{gs2}}R_{\text{in2}}} \cdot Z_{\text{out}}, \quad (16)$$

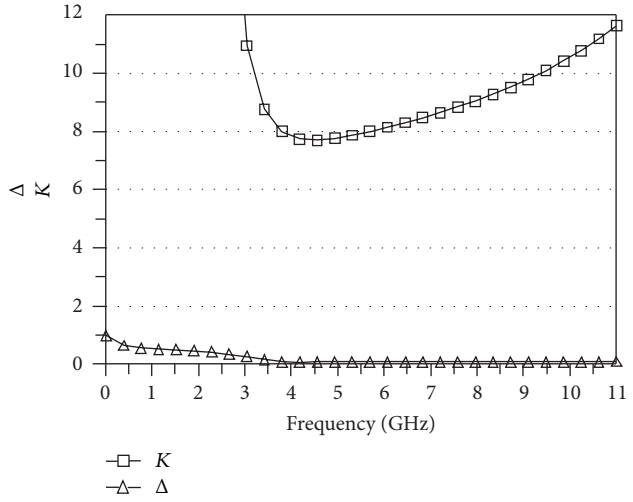

Figure 16: K (stability factor) and Δ simulation result.

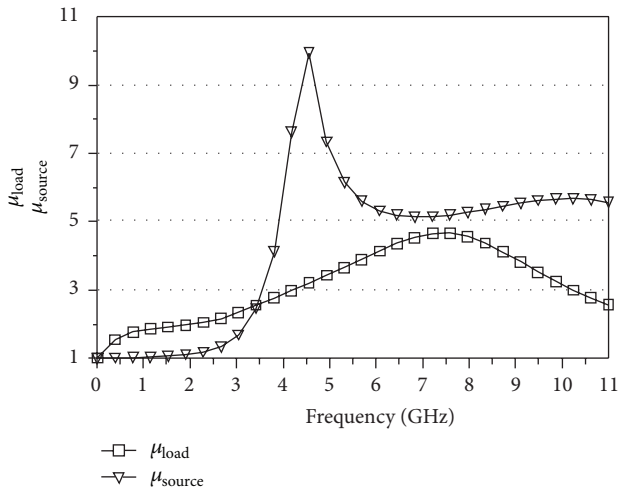

Figure 17: μ factor simulation result.

where R_{in2} is the input resistance at the gate of M_2 and Z_{out} is the output load impedance. The LNA voltage gain can be approximated as

$$A_V \approx \frac{g_{m1} g_{m2} Z_{in} Z_{Load1} Z_{out}}{S^2 C_{gs1} C_{gs2} R_s R_{in2}}. \quad (17)$$

According to (17), the narrowband LNA can be converted into a wideband amplifier by properly selecting the device size. This provides good wideband matching, noise figure optimization design, and flat gain.

3.4. Stability. Amplifier stability is important to prevent natural oscillation. The stability can be determined by the S-parameters, input and output matching network, and circuit terminations. The simpler tests show whether or not a device can be unconditionally stable [20]. One of these is the K-Δ test, which shows if a device can be unconditionally stable if Rollet's condition is defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1,$$
$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1. \quad (18)$$

The K-Δ test cannot be used to compare the relative stability of two or more devices because it involves constraints on two separate parameters. A new criterion has been proposed which combines the S-parameters in a test involving only a single parameter, μ, defined as

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1. \quad (19)$$

The performance of LNA is simulated using the advance design system (ADS). To consider the stability of the LNA, the K factor and Δ should be considered. Figure 16 shows that the K factor is always larger than 1 and the Δ is smaller than 1 all the time. Hence, this circuit is stable for all frequency bands. There is another way to diagnose whether the LNA is unconditionally stable. The μ factor at input and output should be larger than 1 in all frequency bands, as shown in Figure 17.

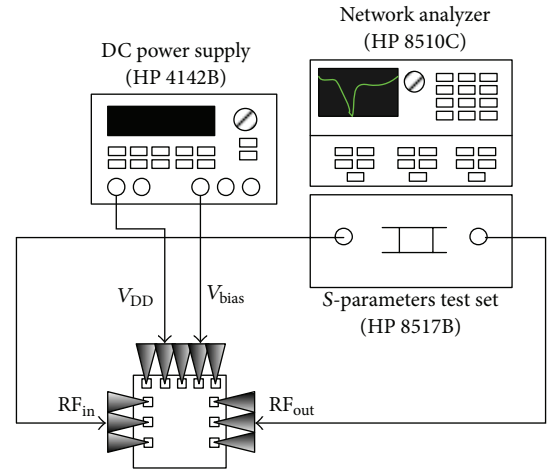

Figure 18: Test setup used for the LNA S-parameter measurements.

4. Measurement Results

On-wafer measurement is performed by an HP 8510C network analyzer and an HP 8517B is to test the S-parameter, as shown in Figure 18. A network analyzer is used to measure the frequency response and input matching of the LNA. The input and output impedance matchings are both 50 Ω. To ensure that the LNA still provides a conversion gain when process deviation occurs, the other process corners, namely, typical-NMOS typical-PMOS (TT), fast-NMOS fast-PMOS (FF), and slow-NMOS slow-PMOS (SS), are also used to simulate this LNA. The results are shown in Figure 19. Figure 19 shows the measurement forward gain (S_{21}), from 3 to 5.6 GHz; the measured gain is about 7–10 dB. The measurement data is 6 dB lower than the pre-simulation data

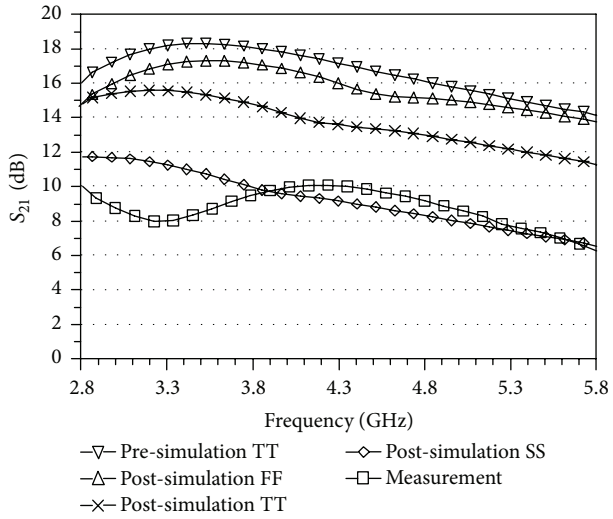

Figure 19: Simulation and measurement results of conversion gain versus frequency of the proposed LNA. RF stands for simulation results of modified MOSFET RF model. FF, TT, and SS represent the simulation results of fast-NMOS fast-PMOS, typical-NMOS typical-PMOS, and slow-NMOS slow-PMOS process corners.

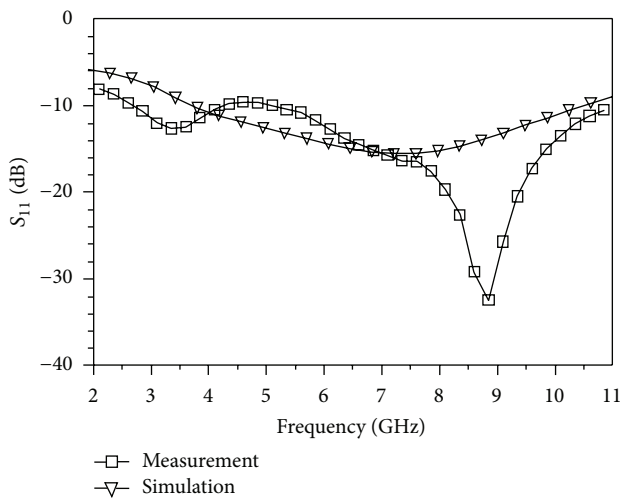

Figure 20: Measured and simulated input reflection coefficient.

because of the process drift and parasitic effect in the layout. The result of conversion gain measurement is situated in the post-simulation (SS) process corner.

Figure 20 shows the input return loss (S_{11}), from 3 to 11 GHz, and the measured S_{11} is less than −9 dB. Figure 21 shows output return loss (S_{22}), from 3 to 7.5 GHz, and the measured S_{22} is less than −8 dB. Figure 22 shows reverse isolation (S_{12}), from 3 to 11 GHz, and the measured S_{12} is less than −40 dB. The simulation measured input of 1 dB compression point at 5.3 GHz shown in Figure 23 is about −8 dB. Figure 24 shows the measured fundamental output power and third-order intermodulation (IM3) for the RF input frequency spacing of 1 MHz, and the IIP_3 is 2 dBm at 5.3 GHz. The IM3 is measured, using two Agilnet E8247C continuous wave

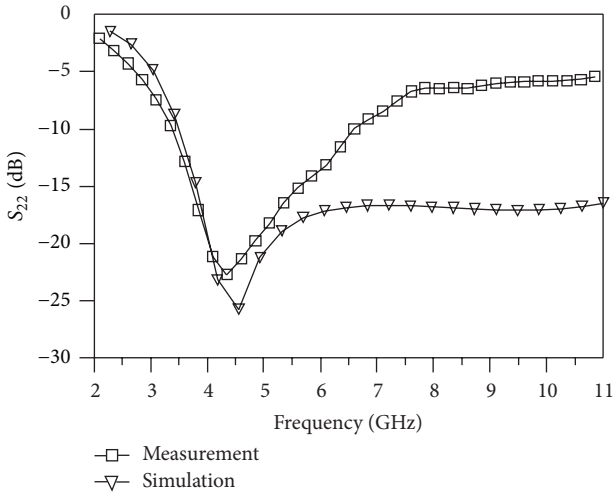

Figure 21: Measured and simulated output reflection coefficient.

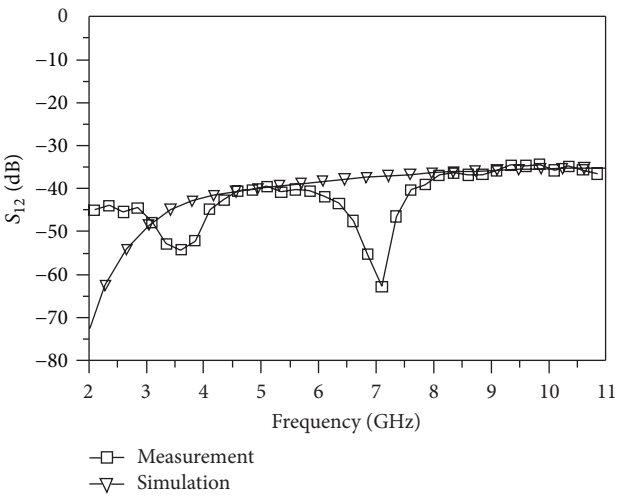

Figure 22: Measured and simulated reverse isolation.

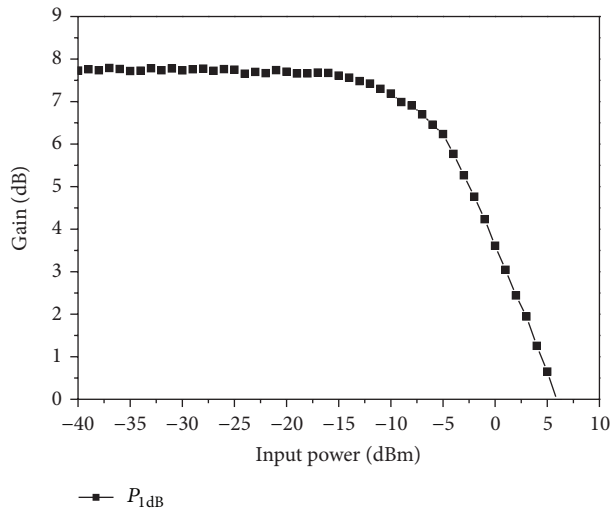

Figure 23: Measured input 1 db compression point at 5.3 GHz.

Table 2: Recently reported performance of UWB LNAs.

Reference	Process CMOS (μm)	S_{11} (dB)	Avg. gain (db)	Freq. (GHz)	NF (dB)	IIP_3 (dBm)	Die area (mm^2)	Power (mW)	Topology
[4]	0.18 μm CMOS	< -7.8	11.9	2–6.5	4.1–4.6	4 (4 GHz)	0.88	27	Feedback
[7]	0.6 μm CMOS	< -7	6.1	0.5–5.5	5.4–8.2	N/A	1.12	83.4	Distributed
[8]	0.18 μm CMOS	< -20	10	0–11	3.1–6.1	N/A	1.44	19.6	Distributed
[9]	0.18 μm CMOS	< -12	14	3–6	4.7–6.7	−5 (4.5 GHz)	1.1	59.4	Distributed
[10]	0.18 μm CMOS	< -9	9.8	2–4.6	2.3–5	−7 (4 GHz)	0.9	12.6*	Feedback
[11]	0.18 μm CMOS	< -9.9	9.3	2.4–9.5	4–9	−6.7 (6 GHz)	1.1	9*	Chebyshev filter
[12]	0.18 μm CMOS	< -10	8.6	2.4–9.4	4.1–10	−3.5 (6 GHz)	1.76	7.1*	Chebyshev filter
[13]	0.18 μm CMOS	< -5	19.1	2.8–7.2	3.2–3.8	−1 (6 GHz)	1.63	32	Feedback network synthesis
[14]	0.18 μm CMOS	< -10	17	2–11	3.8	N/A	0.635	10.56**	Feedback
[15]	0.15 μm HEMT	N/A	18	0.85–13.35	2.5	N/A	1.162	70**	Feedback
This work	0.18 μm CMOS	< -9	9	3–5.6	4.6–5.3	2 (5.3 GHz)	0.8	9	Proposed

*Only core LNA, **Simulation.

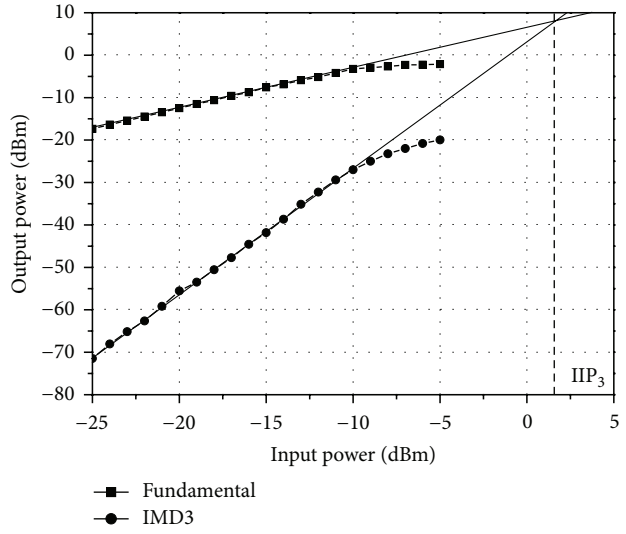

Figure 24: Measured IIP_3 at 5.3 GHz.

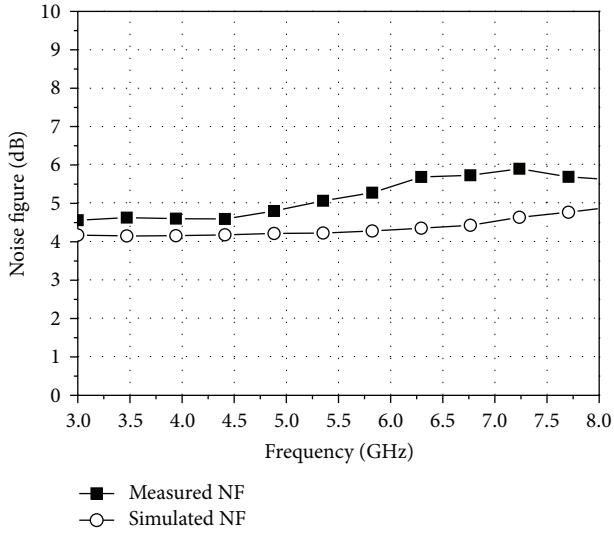

Figure 25: Simulation and measurement NF.

(CW) generators and an Agilent E4407B spectrum analyzer. A noise figure (NF) is measured, using an Agilent N8975A NF meter with an Agilent 346C noise source. The simulation noise figure minimum is 4.1 dB, as shown in Figure 25. Due to the parasitic effect in the layout, the minimum of the measurement is 4.6 dB. Figure 26 shows the micrograph of the LNA. Table 2 summarizes the measurement results and compares them with previous literature. In the proposed LNA topology, the simplified RLC input matching network and the current-reused configuration benefit from the low-power design. The distributed amplifier [7–9] requires high power consumption and a large chip area. Compared with the Chebyshev filter and feedback network synthesis [11–13], the proposed input matching network, which has only one spiral inductor, simplifies the circuit complexity and

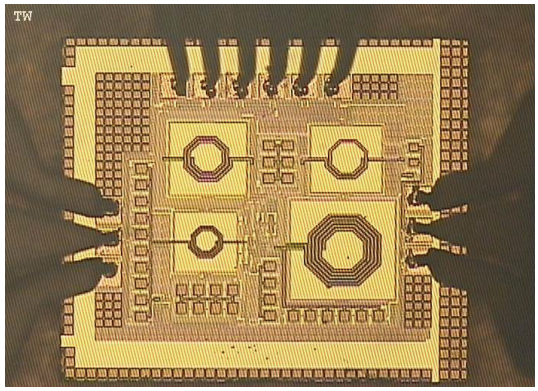

Figure 26: Micrograph of the proposed LNA (size: 1.03×0.78 mm^2).

reduces the chip area. References [10–12] only show core LNA power consumption, excluding the output source follower. References [14, 15] only show simulation. It should show the linearity of the experiment. The LNA plays an important role in improving overall system linearity. Table 2 clearly shows that the proposed LNA has a very small chip area and the lowest power consumption.

5. Conclusion

An RLC wideband matching UWB LNA has been presented in the above results, which can operate at a supply of 1 V voltage in a 0.18 μm CMOS technology. In the proposed topology, the narrowband LNA can be converted into a wideband amplifier by the RLC matching method. The RLC input matching circuit reduces the chip area. The output matching method reduces power consumption. The main advantages of the LNA topology are low power use, moderate noise, linearity, power gain, and a small chip area.

Conflict of Interests

The author indicated no potential conflict of interests.

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