Adaptive Equalization Architecture Using Distributed Arithmetic for Partial Response Channels

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Abstract — *This paper proposes a design and implementation of transversal adaptive digital filter using LMS (Least Mean Squares) adaptive algorithm. The filter structure is based on Distributed Arithmetic (DA), which is able to calculate the inner product by shifting, and accumulating of partial products and storing in look-up table, also the desired adaptive digital filter will be multiplierless filter. In addition, the hardware implementation uses VHDL (Very high-speed integrated circuit Hardware Description Language) and synthesis using FLEX10K Altera FPGA (Field Programmable Gate Array) as target technology and uses Leonardo Spectrum and MAX+plusII program for overall development. The results of this design are shown that the speed performance and used area of FPGA. The experimental results are presented to demonstrate the feasibility of the desired adaptive digital filter..*

Index Terms — LMS Algorithm, Adaptive Digital Filter, Distributed Arithmetic, FPGA.

I. INTRODUCTION

Adaptive digital filters are widely used in the area of signal processing such as echo cancellation, noise cancellation, channel equalization and beamforming. The necessity of hardware implementation requires various of performances such as high speed, low power dissipation and good convergence characteristics. However, generally for design of adaptive digital filters need for fast multiplication and many multipliers. These multipliers will decrease the speed of processing time since the multiplying stage is consumption process and uses large silicon area in VLSI design. Also, this paper proposes a design of distributed arithmetic structure for adaptive digital filter.

Distributed arithmetic (DA) digital filter architecture was first proposed by Peled and Liu in 1974 [1].

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The DA is a direct method for sum of products operations, partial products can pre-compute by difference equation and storing in look-up table contained in memory, input signals is used for addressing.The product can be computed by scaling accumulate of partial products from memory, therefore, multipliers do not necessary for this method, the desired digital filter is multiplierless. Generally, adaptive digital filter has its basis on the widely used LMS adaptive algorithm, originally proposed by Widrow and others [2], it is the popular algorithm for adaptive digital filter. Cowan and others [3] proposed the application of DA for adaptive digital filter with offset binary coding, which is not suitable for the DA adaptive algorithm because the convergence speed of this method degrades extremely. However, this paper proposes the distributed arithmetic adaptive digital filter generalizing with two's complement representation which corresponds to original ideas of Peled and Liu and much more suitable for its implementation.

II. LMS ADAPTIVE ALGORITHM BASED DA

The digital FIR filter is important component of state-of-the-art partial response signaling maximum likelihood (PRML) detection for magnetic hard disk drive (HDD) read channels.

Consider the Nth order of FIR (Finite Impulse Responses) digital filter with input signal vector **S**(k) and N-taps coefficients vector **W**(k) can be expressed as;

$$\mathbf{S}(k) = [s(k), s(k-1), \ldots, s(k-N+1)]^T \quad (1)$$

and

$$\mathbf{W}(k) = [w_0(k), w_1(k), \ldots, w_{N-1}(k)]^T \quad (2)$$

An output signal of FIR digital filter can be expressed as

$$y(k) = \mathbf{S}^T(k)\mathbf{W}(k) = \mathbf{F}^T \mathbf{A}^T(k)\mathbf{W}(k) \quad (3)$$

Defining an address matrix **A**(k) and scaling vector **F** as;

$$\mathbf{A}(k) = \begin{bmatrix} b_0(k) & \cdots & b_0(k-N+1) \\ b_1(k) & \cdots & b_1(k-N+1) \\ \vdots & \ddots & \vdots \\ b_{B-1}(k) & \cdots & b_{B-1}(k-N+1) \end{bmatrix}^T \quad (4)$$

and

$$\mathbf{F} = [-2^0, 2^1, \ldots, 2^{-(B-1)}]^T \quad (5)$$

where B is input signal wordlength, the relationship between input signal and address matrix can be shown as follows;

$$s(k) = [b_0(k), b_1(k), \ldots, b_{B-1}(k)]\ \mathbf{F} \quad (6)$$

From Eq. (4), the address vector will be defined as;

$$\mathbf{A_{vi}}(k) = [b_i(k), b_i(k-1), \ldots, b_i(k-N+1)]^T$$

$$i = 0, 1, \ldots, B-1 \quad (7)$$

Digital equalization for PRML channels uses least mean square (LMS) algorithm in order to update filter coefficients. The equation for coefficients updating of LMS algorithm [2-9] can be expressed as;

$$\mathbf{W}(k+1) = \mathbf{W}(k)+2\mu e(k)\mathbf{S}(k) \quad (8)$$

Hence, multiply the both sides of Eq. (8) by $\mathbf{A}^T(k)$ will give

$$\mathbf{A}^T(k)\ \mathbf{W}(k+1) = \mathbf{A}^T(k)[\mathbf{W}(k)+2\mu e(k)\ \mathbf{S}(k)] \quad (9)$$

Replace $\mathbf{S}(k) = \mathbf{A}(k)\mathbf{F}$ into Eq. (9) will be

$$\mathbf{A}^T(k)\ \mathbf{W}(k+1) = \mathbf{A}^T(k)[\mathbf{W}(k)+2\mu e(k)\mathbf{A}(k)\mathbf{F}] \quad (10)$$

The error signal e(k) can be obtained by;

$$e(k) = d(k) - y(k) \quad (11)$$

where d(k) is a desired signal
The adaptive function space (AFS) [3-5] is defined as

$$\mathbf{P}(k) = \mathbf{A}^T(k)\mathbf{W}(k) = [p_0(k), \ldots, p_{B-1}(k)]^T \quad (12)$$

and

$$\mathbf{P}(k+1) = \mathbf{A}^T(k)\mathbf{W}(k+1) = [p_0(k+1), \ldots, p_{B-1}(k+1)]^T \quad (13)$$

The ith elements of $\mathbf{P}(k)$ and $\mathbf{P}(k+1)$ are partial products that related to address vector $\mathbf{A_{vi}}(k)$ which is ith row vector of $\mathbf{A}^T(k)$. Also, time index of $\mathbf{P}(k)$ and $\mathbf{P}(k+1)$ correspond to $\mathbf{W}(k)$ and $\mathbf{W}(k+1)$ respectively. There are 2^N partial products for the Nth order input signal vector. $\mathbf{P}(k)$ and $\mathbf{P}(k+1)$ include B elements selected by B address vectors. Substituting Eq. (12) and Eq. (13) to Eq. (10), will be obtained

$$\mathbf{P}(k+1) = \mathbf{P}(k)+2\mu e(k)\mathbf{A}^T(k)\mathbf{A}(k)\mathbf{F} \quad (14)$$

The output signal can be represented as;

$$y(k) = \mathbf{F}^T\ \mathbf{P}(k) \quad (15)$$

Assume the input signal is white noise with zero mean unit variance. An expectation value of $\mathbf{A}^T(k)\mathbf{A}(k)\mathbf{F}$ [5] becomes

$$E[\mathbf{A}^T(k)\mathbf{A}(k)\mathbf{F}] = 0.25N\mathbf{F} \quad (16)$$

Replace $\mathbf{A}^T(k)\mathbf{A}(k)\mathbf{F}$ in Eq. (14) with Eq. (16), also Eq. (14) is simplified to

$$\mathbf{P}(k+1) = \mathbf{P}(k)+0.5\mu Ne(k)\mathbf{F} \quad (17)$$

The term $0.5\mu N$ in Eq. (17) can be treated as a constant, integer power of two. Therefore, it is possible to implement hardware without multipliers. Also, it can be obtained multiplierless adaptive digital filter with LMS adaptive algorithm.

III. HARDWARE ARCHITECTURE

An architecture for hardware implementation of adaptive filter uses distributed arithmetic (DA), which is one method often preferred since it eliminates the need for hardware multipliers and is capable of implementing high order filters with very high throughput.

Distributed Arithmetic realization of LMS adaptive digital filter can be derived from Eq. (17). The major design hardware components consist of PISO (parallel in serial out shift register), SISO (serial in serial out shift register), buffer, scaling accumulator, adder, subtractor, update new partial products circuit, RAM and control unit. Therefore, the hardware architecture can be shown in Fig. 1. The operation can be described by 6 steps as follow;

1. A/D is controlled by signal ***sc***, will convert analog signal s(t) to 8 bit digital signal s(k), hence, signal ***lr*** will be loaded to PISO and signal ***clk*** will be shifted each bit of data. Data that shift out from PISO will enter to SISO and will be shifted each bit of SISO by same signal ***clk***.
2. Output of PISO and each SISO can be divided to two groups, one group used for RAM addressing. In the same time another used for prepare data to repeat RAM addressing after input signal shifted already (for RAM coefficient updating).
3. For the first time of RAM addressing, output of RAM will be added to scaled value from ACC using scaling accumulator that controlled by signal ***s_a***. Result will be loaded to ACC by signal ***lacc***. In this time signal ***rd_wr*** that used for RAM reading will be active.
4. Repeat in step 3 until eight bit, output of RAM will be subtracted from scaled value from ACC. Result will be loaded to first buffer by signal ***lr***, then signal ***clacc*** will clear ACC and signal ***lbuff_op*** will be loaded to second buffer for converting digital signal y(k) to analog signal y(t) by D/A.
5. Error signal e(n) can be found by difference between desired signal d(k) and output signal y(k), the error

signal will be passed to update new partial products circuit that contained with bank of shift register to calculate value 0.5μNe(k)**F** that follows by Eq .(17).

6. For the second time of RAM addressing, the new partial products will be replaced old partial products at the same address by new partial products **P**(k+1) are old partial products **P**(k) added with results in step 5. In this time signal ***rd_wr*** that used for RAM reading will be active, and repeat in step 1-6, respectively.

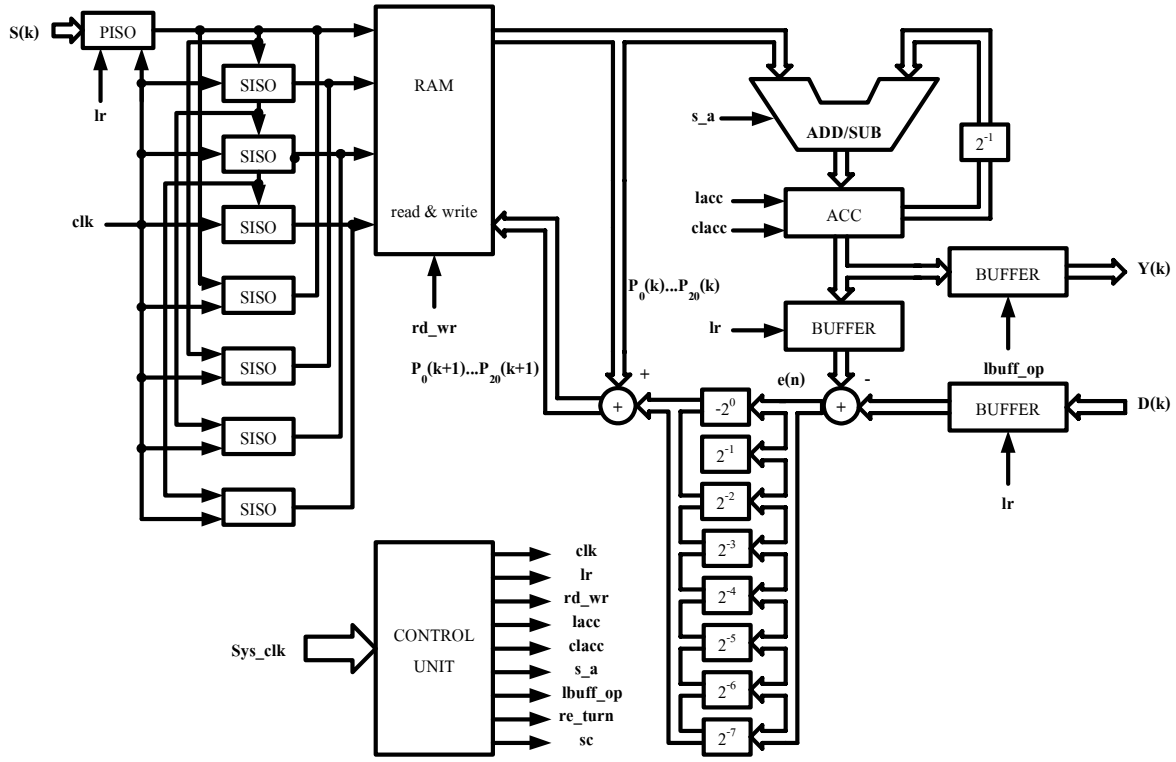

Fig. 1 Proposed hardware architecture for adaptive digital filter based DA

In an implementation will be used VHDL to design and using Leonardo Spectrum and MAX+plusII program for overall development. Timing diagram of control unit is used for controlling all components can be shown in Fig. 2.

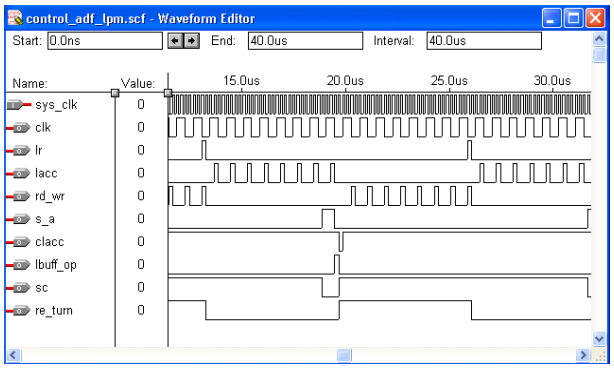

Fig. 2 Timing diagram of control unit

IV. SYSTEM IMPLEMENTATION AND EXPERIMENTAL RESULTS

The simulation result as shown in Fig. 3 shows traces of mean-square error (MSE) plotted versus the number of iterations for 4-taps transversal filter. A number of convergence curves are plotted by showing the performance for 3 cases of the convergence factor.

(i) $\mu = 2^{-3}$
(ii) $\mu = 2^{-4}$
(iii) $\mu = 2^{-5}$

It can be seen that the convergence time increases in the expected manner.

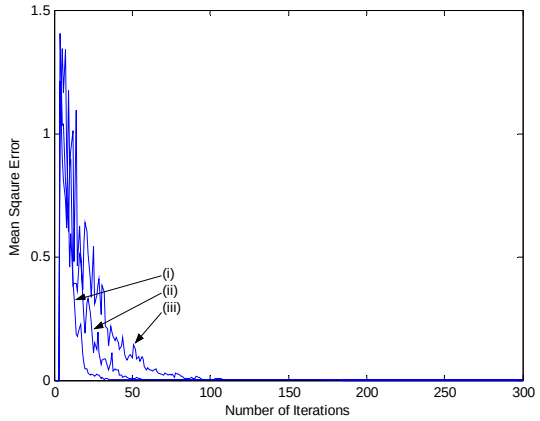

Fig. 3 Plot of MSE versus number of iterations for three convergence factors

An EPF10K10LC84-4 device in FLEX10K family used for circuits synthesis. Device summary of proposed distributed arithmetic adaptive digital filter is shown in Fig. 4 and synthesis result that shown the synthesized circuits in gate-level can be shown in Fig. 5.

** DEVICE SUMMARY **

Chip/ POF	Device	Input Pins	Output Pins	Bidir Pins	Memory Bits	Memory %Utilized	LCs	LCs % Utilized
ad_filter20								
EPF10K10LC84-4		18	9	0	320	5 %	506	87 %
User Pins:		18	9	0				

Fig. 4 Device summary of proposed adaptive digital filter

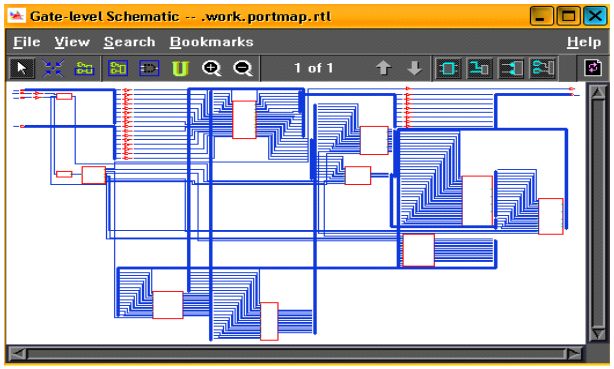

Fig. 5 Synthesized circuits in gate-level

From device summary, 18 input pins used for 8 bits input signal, 8 bits desired signal, system clock and reset, 9 output pins for 8 bits output signal and signal ***sc*** for A/D, 320 memory bits used for implementing 16 address RAM with 20 bits wordlength. Others component will use 506 LCs (logic cells) for implementing. Timing summary shows the maximum frequency of synthesized circuits is shown in Fig. 6.

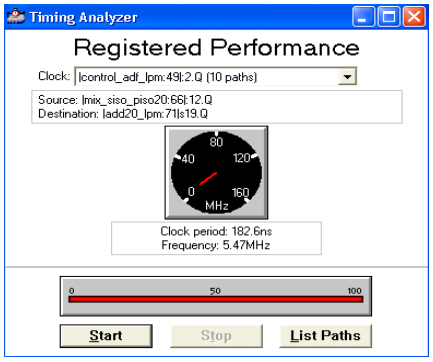

Fig. 6 Timing summary of proposed adaptive digital filter

It should be noted that the major component in this system is RAM, which is independent of number of bits in the input signal wordlength. The size of RAM is determined by number of filter taps used. The number of filter taps chosen for the prototype adaptive digital filter was four since using any more than this involves the use of very large RAMs to store the partial products for filter results. The convergence factor in experiment was fixed at 2^{-4} and the prototype board is shown in Fig. 7.

The experimental result in Fig. 8 is used to show results achieved with this prototype. Input signal s(t) was a square wave, desired signal d(t) was a sinusoidal signal of the same frequency that correspond to fundamental frequency of square wave. The output signal y(t) is the filter output after convergence, which is obviously very close to the desired output.

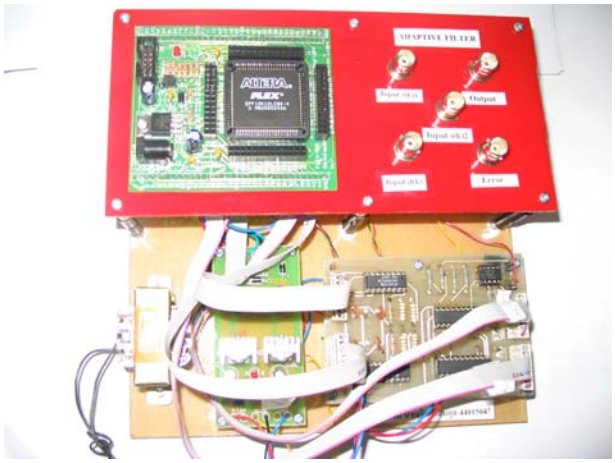

Fig. 7 Prototype of adaptive digital filter using FPGA

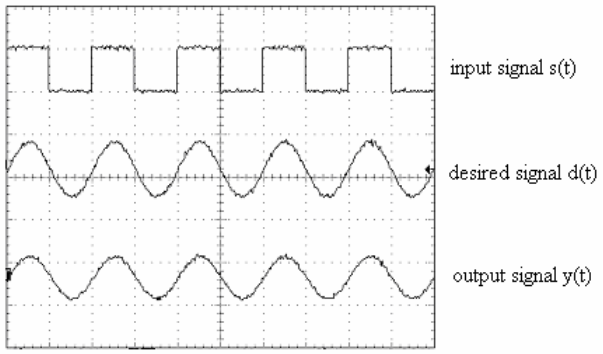

Fig. 8 Experimental result for input signal is square wave

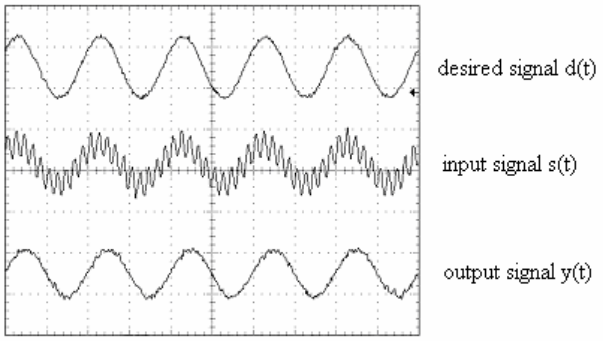

Fig. 9 Experimental result for input signal is composite signal

In Fig. 9 shows the second experimental result from a prototype hardware. The input signal s(t) is a composite signal made up of two frequency sinusoidal inputs at 100 Hz and 1 kHz by amplitude of second frequency is half amplitude of first frequency. Desired signal d(t) is sinusoidal input signal at 100 Hz. After adaptation the filter will be give 100Hz sinusoidal signal that correspond to desired signal with the correct phase.

V.CONCLUSIONS

The experimental results are ensured to the feasibility of the prototype distributed arithmetic adaptive digital filter. The convergence factor analysis of DA adaptive algorithm theoretically using Matlab program, the results are shown in mean square error (MSE) plotting for each convergence factor that must have the values in power of two coefficients.

In Cowan and others papers [3], [5], [7], adaptive digital filter was developed without multipliers using standard integrated circuits and memory devices which have large area and power consumption. This paper uses FPGA in the design and uses VHDL for describing the behavior of proposed hardware architecture. Consequently, it can be obtained the single chip adaptive digital filter and reduces the power consumption. An architecture for hardware implementation of the adaptive equalizer in partial response class 4 (PR4) channel is proposed using this concept.

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