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INVESTIGATIONS ON AN IMPROVED SOFT SWITCHED CLLL DC/DC CONVERTER

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ABSTRACT

A full-bridge CLLL DC/DC converter that uses an auxiliary circuit is proposed in this paper. The soft switching of lagging leg and auxiliary switches is achieved by the proposed circuit for providing reduced switching losses and high efficiency. The theoretical detail operation of the converter is presented. The proposed converter is verified using MATLAB simulation. Closed loop and open loop circuit models are presented for input step change and output load regulation. A prototype of the proposed DC/DC converter is implemented in MATLAB with switching frequency of 20 KHz and output power of 15 W. The performance of the converter is compared with a conventional full-bridge DC/DC converter.

Keywords: CLLL,DC-DC converter, zero voltage switching (ZVS), soft switching techniques, PIC, zero current switching (ZCS).

INTRODUCTION

The PWM phase-shift full bridge DC/DC converter is widely used in medium to high power applications [1-8]. These converters can provide all switching devices to operate under ZVS by using the resonance between a leakage inductor and an output capacitor of switches. It is possible to operate all switching devices of these converters with high switching frequency so that its size can be reduced. But the disadvantage of these converters are under light load conditions, to achieve ZVS for the lagging leg switches require a large inductance which causes an increased loss of duty cycle on the secondary side and more voltage ringing across the secondary side rectifiers. To extend the load range of ZVS many methods have been proposed. Extra passive components are used to achieve full range ZVS in [9-11]. However conduction loss is significant which reduces the efficiency of the converter. Extra active components are used to achieve full range ZVS on the primary side [12, 13]. Although these modifications can decrease the conduction loss and reduce the secondary side voltage spike but it uses two additional main switches in the primary side which increases the cost and it is difficult to implement due to the circuit complexity. A new topology is proposed in [14] where active components are used to achieve full range ZVS on the secondary side but it does not address the freewheeling period conduction loss and secondary diode voltage ringing.

The secondary side voltage ringing can be suppressed by adding an active snubber described in [15, 16] but it adds to cost and it is difficult to implement. The secondary side voltage ringing can also be suppressed by using a primary clamping circuit consisting of an inductor and two diodes [17-19] but it may result in increased primary circulating current and loss of duty cycle.

In [20], a current driven rectifier is introduced. The proposed topology provides zero current switching for output rectifiers with the help of two parallel passive circuits. The voltage spike across the diode bridge is clamped by the output capacitor filter. Parasitic mechanism is analyzed in detail at the secondary side and suppression countermeasure for full bridge converter proposed in [21]. But the proposed LC auxiliary circuit only extends the ZVS range of the lagging leg switches while at light load condition, ZVS can not be attained by the leading leg switches.

A soft switching full bridge converter with minimizes parasitic oscillation from no load to full load is proposed in [22]. ZVS range of leading and lagging legs extend due to the addition of auxiliary coupled inductor. The above literature does not deal with CLLL network based full bridge DC/DC converter.

In this paper, a soft switching full bridge new DC/DC converter with CLLL network is proposed where ZVS of the primary switches and ZCS of the auxiliary switches are achieved by the energy stored in the inductive component of the auxiliary circuit.The operation principle of the proposed converter is explained in detail. The simulation results using MATLAB and experimental results using PIC microcontroller are presented for 15 W/12 V output. The auxiliary circuit which is used in the proposed converter is very simple to implement and the converter provides ZVS in a wide load range with high efficiency.

PROPOSED CIRCUIT AND OPERATION

Figure-1 shows the proposed DC/DC converter. It consists of an auxiliary circuit as shown in dotted line. The auxiliary circuit introduced in the proposed converter, contains two active switches S_5 and S_6, two diodes D_{1a} and

D_{2a}, resonant capacitor C_r, resonant inductor L_{1r} and L_{2r}, and coupling winding L. The main switches of full bridge are S_1,S_2,S_3 and S_4.

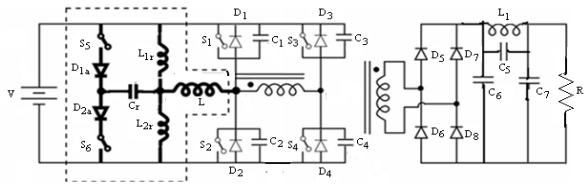


Figure-1. Proposed full bridge DC/DC converter with an auxiliary circuit.

The driving signals for all main switches, auxiliary switches and the principal waveforms of the proposed converter are shown in Figure-2.

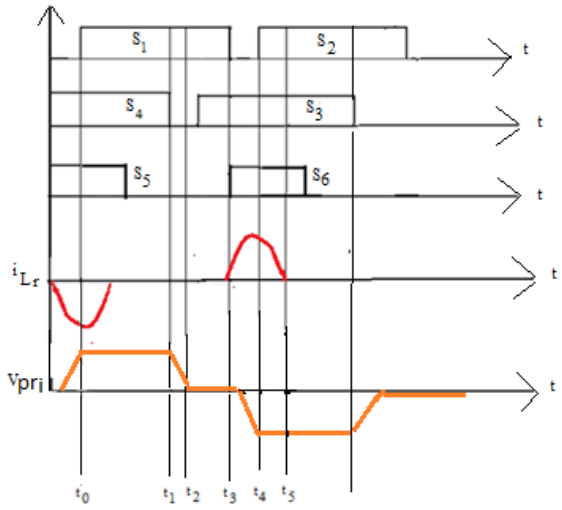


Figure-2. Waveforms of theproposed full bridge DC/DC converter with an auxiliarycircuit.

Prior to t_0, body diode D_1 and S_4 are conducting. Body diode D_1 provides ZVS turn on for switch S_1 when it is on at t_0.

Mode1: As shown in Figure-3(a),at $t=t_0$, S1 and S_4 are on and rectifier diodes $D_5$and D_8 are on and a positive voltage appears across the transformer secondary dotted end. Positive power transfer happens in this interval.

Let $C_1 = C_2 = C_3 = C_4 = C$ and $L_{1r} = L_{2r} = L_r$
L_m = magnetizing inductance of the transformer.
i_m= magnetizing current.
I_0 = output current
i_1=reflected load current
$V_{primary}$= voltage across the primary of the transformer.
$I_{primary}$= current across the secondary of the transformer

Voltage across the primary of the transformer and current across the secondary of the transformer during this mode is given as,

$$V_{primary}(t-t_0) = \frac{L_m di_m(t-t_0)}{dt} = V \quad (1)$$

$$i_{primary}(t\text{-}t_0)=i_1(t\text{-}t_0)+i_m(t\text{-}t_0)=nI_0+i_m(t\text{-}t_0) \quad (2)$$

At the end of this interval at $t=t_1$,

$$V_{C_1}(t_1) = V_{C_4}(t_1) = 0 \text{ and } V_{C_2}(t_1) = V_{C_3}(t_1) = V$$

Mode2: As shown in Figure-3(b), S_4 is off and primary current which was flowing through S_4 charges the output capacitance of S_4 and discharges the output capacitance of S_3. Rectifier diodes $D_5$and D_8 continue to conduct because voltage across the transformer primary and secondary remains same. At the end of this interval, body diode D_3 is forward biased so that switch S_3 can be turned on at ZVS. This leading leg ZVS is achieved very easily even for small load because the energy of the large filter inductor in the secondary is used to achieve the ZVS.

$$i_{c4}(t\text{-}t_1)+i_{c3}(t\text{-}t_1)=i_p(t\text{-}t_1)=nI_0+i_m^* \quad (3)$$

wherei_m^* is the magnetizing current at t_1.
At the end of this interval at $t=t_2$,

$$V_{C_1}(t_2) = V_{C_3}(t_2) = 0 \text{ and } V_{C_2}(t_2) = V_{C_4}(t_2) = V$$

Mode3: As shown in Figure-3(c), S_1 and D_3 are on during this period which is called a free wheeling period. Voltage across the primary winding is zero since it is shorted by the conduction of the body diodes of S_3 and switch S_1. Voltage across secondary is zero because primary of the transformer is shorted. So, the secondary voltage is shorted and all the output rectifier diodes are in conduction.

Voltage across the primary of the transformer and current across the secondary of the transformer during this mode is given as,

$$V_{primary}(t-t_2) = L_m \frac{di_m(t-t_2)}{dt} = 0 \quad (4)$$

$$I_{Primary}(t-t_2) = i_1(t-t_2)+i_m(t-t_2) = i_m^* \quad (5)$$

At the end of this interval at $t=t_3$,

$$V_{C_1}(t_2) = V_{C_3}(t_2) = 0 \text{ and } V_{C_2}(t_2) = V_{C_4}(t_2) = V$$

Mode4: As shown in Figure-3(d), S_1 is off and auxiliary switch S_6 is on. Resonant current flows through the resonant capacitor C_r and resonant inductor L_{2r}.

Resonant capacitor voltage $\left(V_{C_r}\right)$ and resonant inductor current $\left(i_{l_r}\right)$ is given by

$$i_{L_r}\left(t-t_4\right)=nI_0+V\sqrt{\frac{C_r}{L_r}}Sin\left(w\left(t-t_3\right)\right) \quad (6)$$

$$V_{C_r}\left(t-t_4\right)=V\cos(w(t-t_3)) \quad (7)$$

Where $w=\frac{1}{\sqrt{L_r.C_r}}$

Body diode of S_2, D_2 starts conducting at the end of this interval to ensure ZVS turn-on for S_2. At the end of this interval, resonant capacitor voltage is given by

$$V_{C_r}=\left(\frac{-V}{K_T}\right)$$

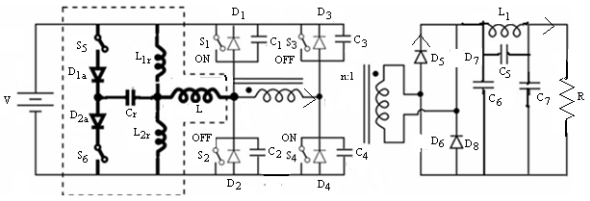
Where K_T is the turns ratio between primary of power transformer and coupled winding.Output rectifier diodes D_6 and D_7 starts conducting full load current.
At the end of this interval at $t=t_4$,

$$V_{C_2}\left(t_4\right)=V_{C_3}\left(t_4\right)=0 \text{ and } V_{C_1}\left(t_4\right)=V_{C_4}\left(t_4\right)=V$$

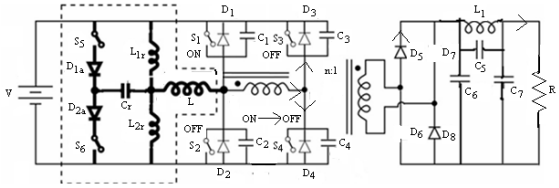
Mode5: As shown in Figure-3(e), at the end of mode4, resonant capacitor voltage ($-V/K_t$) resets the resonant current in L_{2r} to zero. So, S_6 is turned off at ZCS. Output rectifier diodes D_6 and D_7 conducts in the same direction.
At the end of this interval at $t=t_5$,

$$V_{C_2}\left(t_6\right)=V_{C_3}\left(t_6\right)=0 \text{ and } V_{C_1}\left(t_6\right)=V_{C_4}\left(t_6\right)=V$$

Mode6 to Mode10 is similar to Mode1 to mode5



(a)



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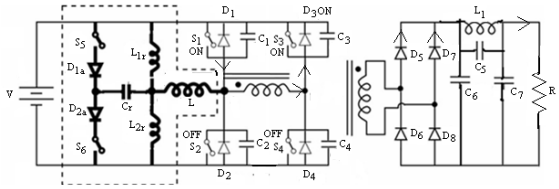
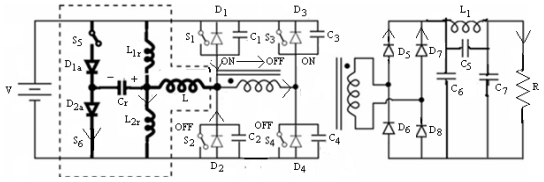
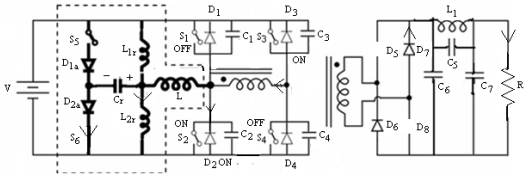


(c)



(d)



(e)

Figure-3. Operating circuits during the first half cycle: (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, and (e) Mode 5.

SIMULATION RESULTS AND DISCUSSIONS

The designed converter is simulated using matlab simulation and the prototype is fabricated. The converter specifications and component values are shown in Table-1.

Table-1. Converter specifications and component values.

Specification	Component values
Input voltage: V = 48 V	Auxiliary inductance: 20 mh
Output voltage: V_0 = 12 V	Auxiliary capacitance: 10 µF
Switching frequency: f = 20 KHz	Auxiliary filter inductance: 1 h
Power: P = 15 W	Auxiliary filter capacitance: C_5= 100 µF, C_6= C_7 =500µ F

The proposed circuit has been simulated by using matlabsimulink and the waveforms are shown in Figure-4. Gating signals for S_1 and S_2 (lagging leg switches) and S_5 and S_6 (auxiliary switches) are shown in Figure-4(a). It is observed that the auxiliary switch S_6 is on when lagging leg switch S_1 is off and S_5 is on when S_2 is off. The conduction time of auxiliary switch is shorter than that of main switch.

The gating signal for S_6, drain to source voltage of S_2, resonant inductor current i_{Lr}, and drving voltage of S_2 are shown in Figure-4(b). It is seen that the resonant inductor current i_{Lr} is zero before gating signal to S_6 becomes zero.which ensures zero current switching (ZCS) for S_6. It is also observed that, drain to source voltage of main switch S_2, is zero before it is gated which ensures zero voltage switching (ZVS) turn on for S_2.

The transformer primary voltage is shown in Figure-4(c). The transformer secondary voltage is shown in Figure-4(d). DC output voltage is shown in Figure-4(e) and DC output current is shown in Figure-4(f). DC output voltage is 12 V and DC output current is 1.2 A. Table-2 shows the performance of the proposed converter from simulation. From simulation, Figure-5 shows the efficiencies of the proposed converter and the conventional converter as a function of load current.

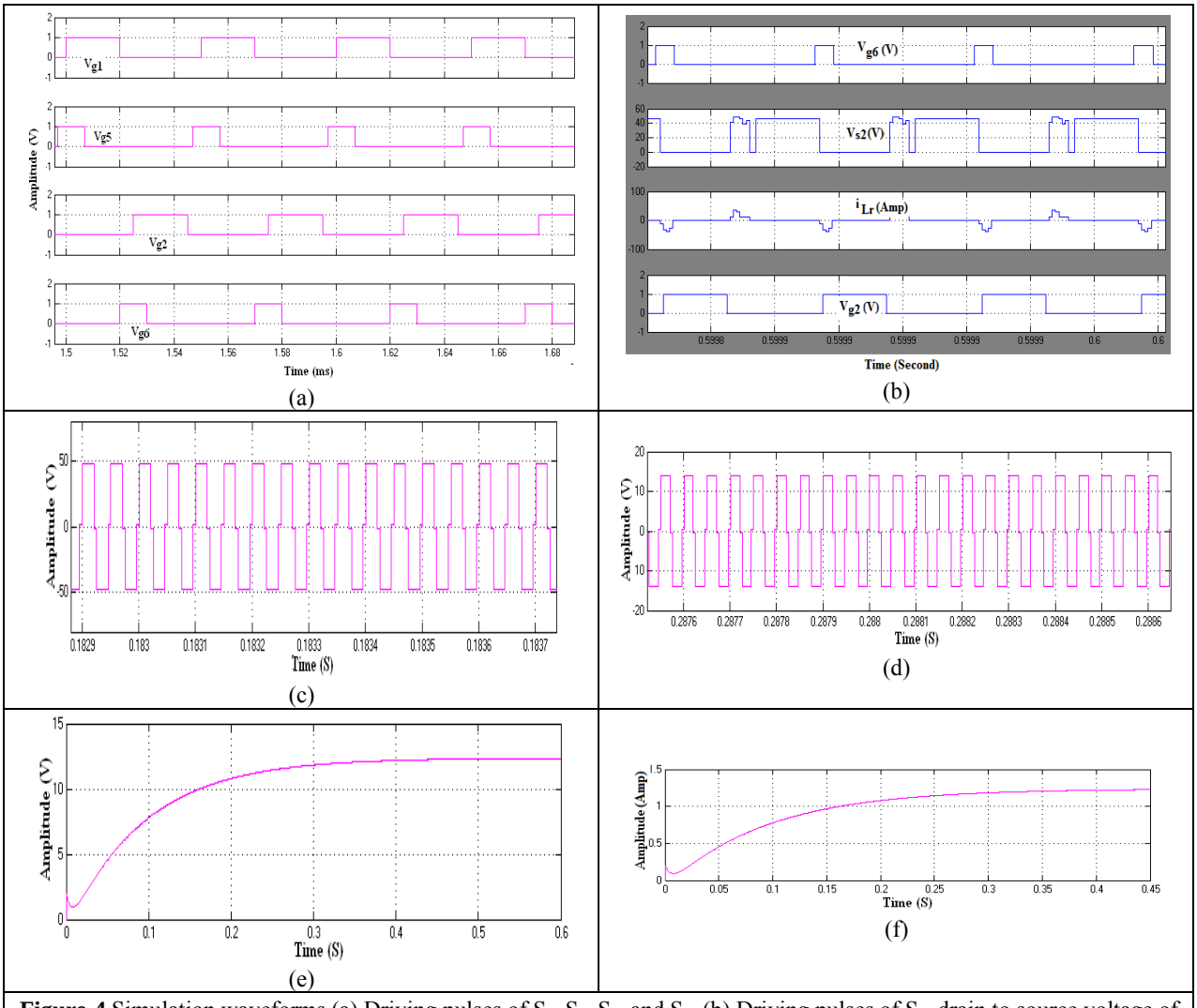


Figure-4. Simulation waveforms.(a) Driving pulses of S_1, S_5, S_2, and S_6. (b) Driving pulses of S_6, drain to source voltage of S_2, resonant inductor current i_{Lr}, drving voltage of S_2(c)Primary voltage of the transformer. (d) Secondary voltage of the transformer. (e) DC output voltage, (f) DC output current.

Table-2. Performance of the proposed converter from simulation.

% load	Output voltage (V)	Outputcurrent(Amp)	Output power (W)	Input power (W)	Efficiency (%)
45	12.07	0.73	8.78	9.64	91.12
52	12.05	0.84	10.15	11	92.26
58	12.01	0.94	11.29	12.14	93.03
68	11.95	1.1	13.15	14.17	92.82
78	11.9	1.26	15.03	16.33	92.02
100	11.82	1.61	19.03	20.73	91.79

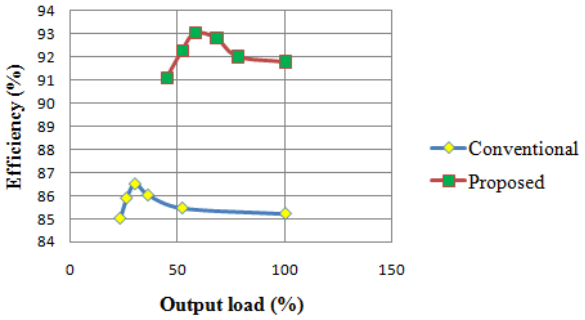


Figure-5. Efficiency versus load current from simulation.

COMPARISON OF OPEN LOOP SYSTEM WITH CLOSED LOOP FOR CHANGE IN INPUT VOLTAGE

The block diagram of closed loop system is shown in Figure-6. The open loop based simulink model of the proposed circuit is shown in Figure-7 with an input disturbance at 0.7 second. Figure-8 shows the input and output voltage with input step change. From Figure-8, we observe that the output voltage changes due to change in input voltage

The closed loop simulink model of the proposed circuit is shown in Figure-9 with a disturbance input at 0.7 second. The instantaneous output voltage is compared with the set voltage of 12V. The error signal is sent to the PI controller which controls the output voltage of the closed loop system. From Figure-10, we observe that output voltage increases and reduces to 12 V. Thus, the steady state error is reduced by using the closed loop system.

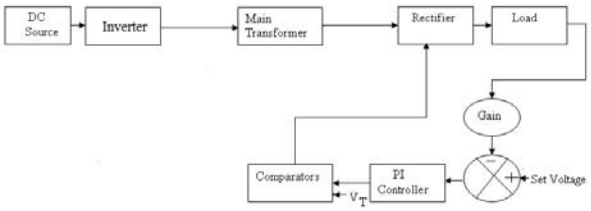


Figure-6. Blockdiagram of closed loop system.

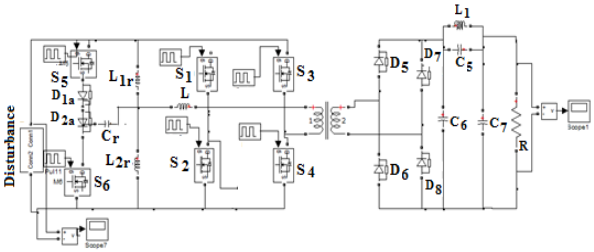


Figure-7. Open loop system with input step change.

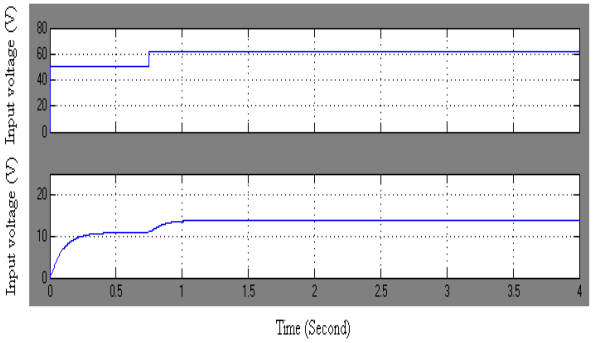


Figure-8. Input and output voltage with input step change.

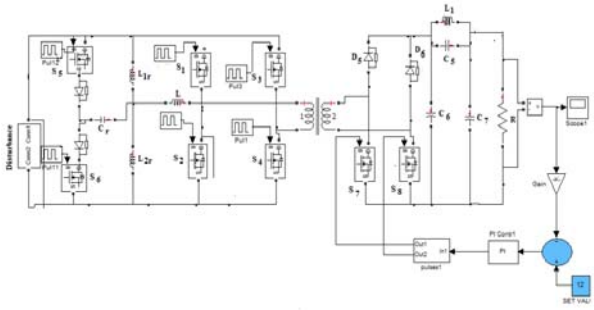


Figure-9. Closed loop system with input step change.

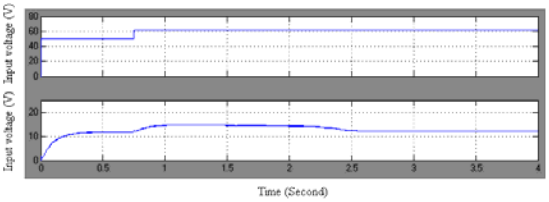


Figure-10. Input and output voltage with input step change.

COMPARISON OF OPEN LOOP SYSTEM WITH CLOSED LOOP FOR OUTPUT LOAD REGULATION

The open loop system simulink model of the proposed circuit is shown in Figure-11 without output load regulation. The input voltage is 48V DC and load resistance is connected through a breaker. Load resistance is 10Ω and additional resistance 10Ω resistance is connected. Initially the breaker is opened and it is closed at 0.5S. Figure-12 shows that due to the change in the load, the DC output voltage changes at 0.5S. The closed loop simulink model of the proposed circuit is shown in Figure-13 with output load regulation. The input voltage is 48V DC. The subtractor in the control loop gets output voltage of the converter as one of input and other input to the subtractor is the reference voltage or set voltage of 12V. The output of the subtractor is given to the PI controller which is called the error signal. The PI controller output is given to the two comparators. The two comparator outputs are the PWM waves which are given as control signals to the gate pulses for switches S_7 and S_8Initially the breaker is opened and it is closed at 0.5S. The DC output voltage reduces at 0.5S when the breaker is closed and due to the closed loop control, the final output voltage reaches to a value of 12V as shown in Figure-14.

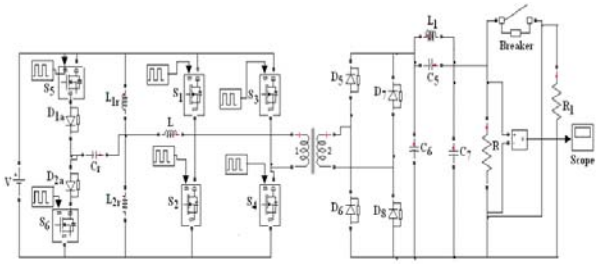


Figure-11. Open loop system without output load regulation.

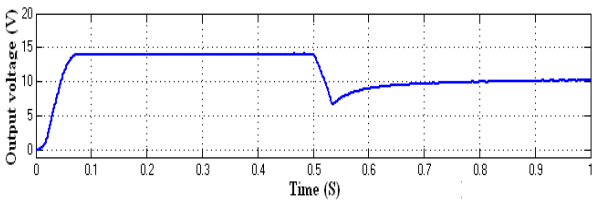


Figure-12. DC output voltage without load regulation.

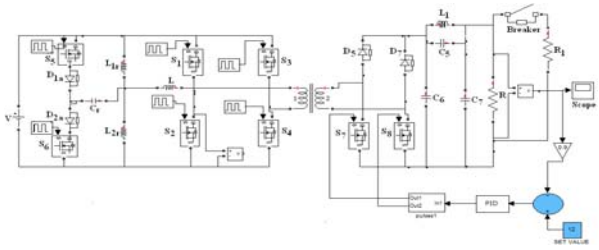


Figure-13. Closed loop system with output load regulation.

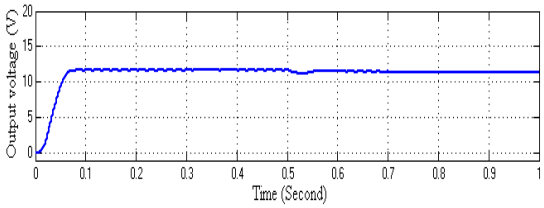


Figure-14. DC output voltage with output load regulation.

CONCLUSIONS

This paper presents an improved soft switched full bridge CLLL DC/DC converter. The operating principles with necessary mathematical equations have been presented. The proposed converter is analyzed, and a prototype is developed.In MATLAB. Closed loop and open loop circuit models were developed for input step change and output load regulation and they are successfully used for simulation studies. Conversion of 48V to 12V is done using the proposed method and the results are compared with a conventional method. It has been found that the proposed converter has improved efficiency in comparison to conventional converter. The theoryand simulation results show good agreement. The proposed converter can be used for medium and high power applications where very high efficiency has to be maintained from no load to full load.

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