

# Vertical cavity surface emitting laser based optoelectronic asynchronous transfer mode switch

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**Abstract.** Large broadband asynchronous transfer mode (ATM) switching nodes require novel hardware solutions that could benefit from the inclusion of optical interconnect technology, since electronic solutions are limited by pin out and by the capacitance/inductance of the interconnections. We propose, analyze and demonstrate a new three stage free space optical switch that utilizes vertical cavity surface emitting lasers (VCSELs) for the optical interconnections, a liquid crystal spatial light modulator (SLM) as a reconfigurable shutter and relatively simple optics for fan out and fan in. A custom complementary metal oxide semiconductor (CMOS) chip is required to introduce a time delay in the optical bit stream and to drive the VCSELs. Analysis shows that the switch should be scalable to  $1024 \times 1024$ , which would require  $2048 \sim 2$  mW VCSELs. © 1999 Society of Photo-Optical Instrumentation Engineers. [S0091-3286(99)01407-5]

Subject terms: optical switching; vertical cavity surface emitting lasers; asynchronous transfer mode; smart pixels; optical interconnections.

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## 1 Introduction

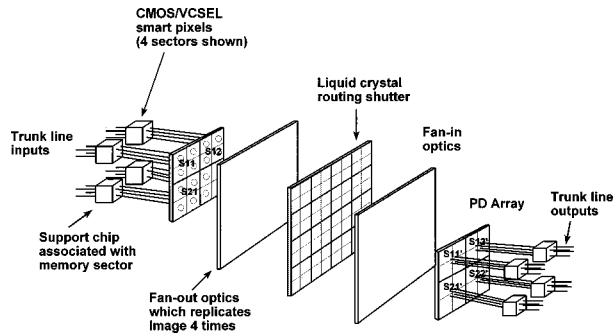
Asynchronous transfer mode (ATM) is a form of packet switching that transmits information by attaching a 40 bit header to a message packet of 384 bits. ATM services are presently based on all-electronic switching fabrics.<sup>1</sup> However, as the size of the switch becomes large, the throughput of the switch becomes limited by communication bottlenecks caused not by the electronic processing units themselves, but by the electronic interconnects. Thus, while the processing power of electronic chips is sufficiently great that a single chip can contain much of the processing capability needed for an entire system (or a large portion of a system), a much more difficult task involves supplying the chip with enough high speed reconfigurable input/output ports. Hence it is advantageous to consider a hybrid optoelectronic approach where free space optics is used to increase the connectivity and electronics is used to carry out the processing functions.<sup>2-6</sup>

This paper presents a scalable technique of implementing a three stage switching architecture<sup>7</sup> using arrays of vertical cavity surface emitting lasers (VCSELs) and a liquid crystal over silicon [ferroelectric liquid crystal/very large scale integration (FLC/VLSI)] spatial light modulator (SLM). The VCSELs are used primarily as high speed optical interconnects and the liquid crystal SLM functions as a reconfigurable routing shutter. VCSELs can easily be fabricated into 2-D arrays of individually addressed lasers that emit a low divergent column of light normal to the array surface.<sup>8</sup> These lasers are highly efficient and have high reliability.<sup>9,10</sup> Thus, VCSELs are ideal light sources for large scale optical free space interconnects in a communication switch. However, as has been shown by others,<sup>4-6</sup> it is difficult to find a technique of reconfiguring the optical interconnections without requiring a large number of

VCSELs, needing complex optics, or suffering excessive optical loss due to fan-out. Liquid crystal SLMs are relatively slow, but can be used to project large, programmable patterns that can be used for routing. By merging the advantages of the two optical technologies with electronics, a scalable ATM switch can be formed.

Previously, researchers at NEC utilized VCSELs in communication packet switching. Kawai and Kurita<sup>4</sup> implemented a three stage switching architecture using multiwavelength VCSEL arrays and multimode fiber interconnects. This approach requires a large number of VCSELs and complex optics, which results in a relatively high optical power loss. Li et al.<sup>5,6</sup> proposed an architecture with low optical loss by assigning an array of  $N$  VCSELs to each of the  $N$  input channels and using passive optics to steer the beams to the required output. In this way, there is no optical fan-out loss. However, the system requires  $N^2$  VCSELs, and therefore the number of VCSELs increases rapidly as the switch increases to a practical size. In addition, the size of the microlenses and the macrolens also increases significantly as  $N$  increases. Even so, these researchers have succeeded in demonstrating a system with over 200 inputs by using fiber bundles to route the optical signals to and from a free space switch.

Walker<sup>11</sup> at Heriot-Watt University proposed using VCSELs to send packets of data between complementary metal-oxide semiconductor (CMOS) chips. The  $N$  input data packet streams are fanned out with a binary phase grating (BPG) to form  $N$  subarrays. Each packet has an address header that can be read by an array of smart pixels. One multiple quantum well (MQW) modulator is attached to each smart pixel subarray. The modulator then transmits one of the data streams from its subarray. The number of data streams is limited by the custom made multiple com-



**Fig. 1** Conceptual illustration of the three stage ATM switching fabric.

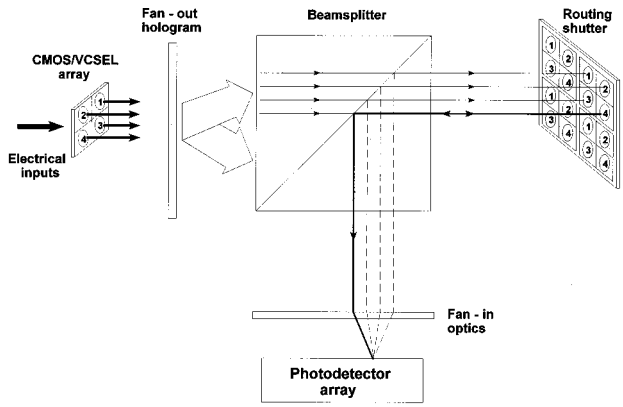
ponent lenses that are required for this system. Other MQW ATM switching systems have also been proposed and/or demonstrated.<sup>3,12-14</sup> In addition, several VCSEL based, free space processing systems have been demonstrated.<sup>15-18</sup>

The architecture presented here uses an array of only  $2N$  VCSELS that transmits through fan-out optics onto a liquid crystal routing shutter. The array is divided into sectors that were previously<sup>2,7</sup> shown to reduce optical loss in proportion to the number of sectors, e.g., for a system with 1024 inputs and 32 sectors, the optical fan-out is reduced from 1024 to 32 and the required optical output power of the VCSELS is also reduced by a factor of 32. The total beam loss of this system, as shown later is then only  $\sim 23$  dB. This loss appears to be sufficiently low to provide a BER of  $\leq 10^{-9}$  with an output power of  $\sim 2$  mW per VCSEL. Thus, the proposed VCSEL/LC switch is scalable to  $N \geq 1024$ .

## 2 Three Stage VCSEL/SLM Based ATM Switching Architecture

The three stage switch illustrated in Fig. 1 was previously described in detail.<sup>7</sup> It is composed of a central routing switch (sectorized optical crossbar) that performs cross point routing of the inputs to the outputs. The stage in front of the routing switch performs two tasks: (1) it organizes the inputs into sectors to reduce the number of cross points and (2) it selects locations on the input plane to prevent the collisions of cells destined for the same output group on input sectors. The stage following the routing switch (the output stage) places the arbitrated inputs into queues and performs a time slot interchange as required. This architecture is independent of the technology used to implement it and we describe here a scalable technique that utilizes VCSELS as high speed optical interconnects and an FLC SLM that performs the routing.

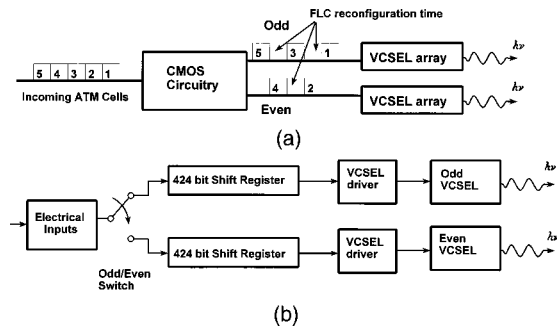
Figure 2 illustrates the general features of the proposed VCSEL/SLM reconfigurable switch. The first stage is composed of the VCSEL array and the controlling electronics, the second stage is made up of the diffractive fan-out optics and an SLM (liquid crystal routing shutters), and the third stage contains the fan-in optics, the output photodetector array and electronic queues/controls. As discussed, the first stage electronically divides the  $N$  inputs into  $m$  sectors of size  $N/m$  to reduce the number of cross points. The outputs of these sectorized units drive the VCSELS. Then  $N/m$  copies of each of the optical bit streams emitted from the



**Fig. 2** Layout of the VCSEL/liquid crystal cross point switch showing typical optical paths through the switch.

VCSELS are made by the diffractive fan-out optics and imaged onto the liquid crystal routing shutters. Only  $N$  of the  $N^2/m$  routing shutters are open, i.e., one for each output channel. The beams reflected from the shutter are then collected by the fan-in optics and directed onto a photodetector array prior to queuing for the output port.

The liquid crystal routing shutter pattern remains fixed for one ATM cell period, e.g.,  $2.7 \mu\text{s}$  for STM-1 (155 megabits/s), during which time the bit stream of that set of input cells is routed to the proper output. Since the next set of input ATM cells will be routed to different outputs, the routing shutter array must be reconfigured into another pattern before these new cells arrive. However, there is very little time between the incoming cells (only the  $0.3 \mu\text{s}$  from the 5 bytes of header) and since the liquid crystal shutters switch slowly, a delay between the cells must be introduced. This time delay can be gained by electronically demultiplexing the odd and even incoming ATM cells between two spatially separated VCSEL arrays, as illustrated in Fig. 3(a). To accomplish this, each input channel has a demultiplexing switch, two 424 bit shift registers (which provides a one cell delay between the cells streams) and a VCSEL driver circuit. One array of VCSELS is driven by the first, third, fifth, etc. (odd) cells and the other VCSEL array is driven by the second, fourth, sixth, etc. (even) cells, as shown in the timing diagram of Fig. 3(b). The VCSELS can operate<sup>19</sup> at  $>3$  gigabits/s and therefore the operating frequency is limited by the CMOS driver circuit. However,



**Fig. 3** CMOS/VCSEL smart pixel: (a) schematic timing diagram and (b) block diagram.

CMOS VCSEL drivers operating up to 622 megabits/s have been reported,<sup>20</sup> therefore the VCSEL drivers should not impose a frequency limitation.

The method of connecting the VCSELs to the CMOS and the layout of the VCSEL array must allow for high speed operation, scalability and functionality of the optical system. Simple wire bonding techniques are suitable for small arrays (small number of inputs) operating at low speed, however, as the number of inputs and the operating speed increase, more elegant techniques are required, as discussed in Sec. 3.2. With regard to the layout of the VCSELs, it appears that interleaving the two VCSEL arrays is the optimum layout configuration since physically separating the arrays increases the length of the electrical leads on the CMOS chip, thus increasing the chip area and the lead capacitance. The liquid crystal routing shutters must also be interleaved into two arrays to match the VCSEL arrays. Two shutter arrays are used so that while one shutter array is actively routing the signals from one of the VCSEL arrays, the second shutter array is being reconfigured.

### 3 Scalability

Scalability is the most important consideration in evaluating the potential of an optoelectronic ATM switch since small switches can be implemented electronically and optoelectronic switches will be used only if they increase the aggregate throughput and/or connectivity. Scalability of the proposed switch is a function of a number of interrelated features of the VCSELs, the VCSEL control chip, the sensitivity of the receivers on the output stage and the fan-in/fan-out optics. Primarily these features relate to

1. optical power obtainable from the VCSEL
2. size and the ability of the chips to sink the power dissipation
3. characteristics of the liquid crystal routing shutter
4. optics and optomechanics.

These are discussed in the following sections based on reasonable estimates of the present state of the art devices. The practical aspects of the optics and optomechanics are also considered. It is shown that the proposed switch is practical up to at least  $1024 \times 1024$ .

#### 3.1 Required VCSEL Optical Output Power

The optical output power required by each of the VCSELs is determined by the optical loss of the system and the incident power on the photodetectors needed to achieve a low bit error rate (BER) at the specified bit rate. It is important to minimize the required optical output power since it relates to the electrical power dissipation and the usable VCSEL array size. The incident power for a specified BER must first be estimated. Li et al.<sup>5</sup> calculated the required receiver power for their VCSEL based optoelectronic crossbar switch by assuming Gaussian noise and taking into account the fact that high performance/low noise receivers cannot be fabricated in large arrays, they estimated that a receiver sensitivity of about  $-20$  dBm ( $\sim 10 \mu\text{W}/\text{channel}$ ) is required for a frequency of  $\sim 1.2$  GHz.

The same general approach can be used to analyze the switching architecture proposed here. However, the crosstalk introduced by the finite contrast ratio (CR) of the liquid crystal routing shutter and the VCSEL might also contribute to the noise. The CR is defined as the ratio of the intensity emerging from the liquid crystal cell in the on state compared to that in the off state. If there are  $N$  channels being routed then there is crosstalk due to light leakage through the  $N - 1$  closed shutters, since the closed shutters will reflect  $1/\text{CR}$  of their incident light into the fan-in optics. Assuming that the data presented to the routing shutter are random, the probability of any pixel being on is 0.5. The multiple discrete levels at the photodetector therefore have a binomial probability density function, which for large  $N$ , approaches a Gaussian distribution, which is superimposed on the thermal noise of the photodetector/receiver. The BER for the system can then be approximated by

$$\text{BER} = \sum_{x=0}^N \sqrt{\frac{1}{2\pi N}} \exp[2(1 - N/2)^2/N] \times \text{erfc} \left\{ \frac{i_{\text{ph}}[(\text{CR} + N - 2)/2\text{CR}]}{(8kTB/R)^{1/2}} \right\}, \quad (1)$$

where  $i_{\text{ph}}$  is the photocurrent of the detector,  $B$  is the bandwidth,  $R$  is the input resistance,  $T$  is the absolute temperature and  $k$  is Boltzmann's constant. Plotting BER as a function of contrast ratio reveals that the crosstalk introduced by the routing shutter is minimal if  $\text{CR} \geq 2N/m$ , but it increases rapidly for  $\text{CR} < 2N/m$ . For  $N = 1024$  and  $m = 32$ , CR must be  $\geq 64$ . Since fast liquid crystal shutter with  $\text{CR} > 1000$  have been reported,<sup>21</sup> we assume that the shutter introduced crosstalk is minimal.

Noise also arises due to polarization instabilities of the VCSELs. However, this noise can be reduced to a low level by the proper size and shape of the VCSEL aperture.<sup>22</sup> Thus, it appears reasonable to assume that the calculations of Li et al.<sup>5</sup> will hold for the present system and that a detector input power of  $\sim 10 \mu\text{W}$  will result in a  $\text{BER} \leq 10^{-9}$ .

Based on a detector input of  $10 \mu\text{W}$ ; the required VCSEL optical power can be determined from the system optical loss. The optical losses of the proposed system can be estimated in a straightforward manner, as outlined in Table 1, which indicates that the proposed ATM switch with 1024 input channels, can operate with  $-23$  dB loss, which requires a VCSEL output power of  $\sim 2$  mW. This is well within the capability<sup>23,24</sup> of present polarization controlled VCSELs. Polarization control is required to reduce the unusable light generated by the VCSEL as a consequence of the LC shutters requiring linearly polarized light in intensity modulation schemes. The optical power budget of Table 1 assumes that the polarization ratio of the VCSELs is sufficiently large that a passive polarizing element placed in front of the shutters produces only a small loss.

**Table 1** Summary of optical power losses in the VCSEL based ATM switch.

Optical Loss Mechanism	Best Case	Expected Case	Worst Case
Reflections from the air/glass interfaces, assuming antireflection (AR) coatings	-0.3 dB	-0.4 dB	-0.5 dB
Holographic efficiency of the fan-out optics	-0.6	-1.6	-2.6
Polarizer loss, assuming the VCSELs are 99% polarized	-0.1	-0.1	-0.1
Analyzer loss due to liquid crystal (LC) switching angle ( $\theta$ )	0 ( $\theta=45$ deg)	-3.0 ( $\theta=22.5$ deg)	-15.0 ( $\theta=5$ deg)
LC routing shutter efficiency	-1.0	-1.6	-3.0
Efficiency of the fan-in optics	-0.2	-0.7	-2.2
Fan-out optics for 1024 input channels and 32 sectors	-15.0	-15.0	-15.0
Photodetector quantum efficiency	0	-0.7	-3.0
	-17.2 dB	-23.1 dB	-41.4 dB
Optical power required per VCSEL for 10 $\mu$ W (-20 dBm) on the photodetectors	$\sim 0.5$ mW	$\sim 2.0$ mW	$\sim 100$ mW

### 3.2 Size and Power Dissipation of the VCSEL and CMOS Smart Pixel Chips

The scalability of VCSEL/CMOS smart pixel chip(s) are dependent on three primary factors: the power dissipation of the chips, the size of the chips and the number of electrical input/output pads. This section estimates these values for  $N=1024$ .

Power dissipation for a VCSEL array can be calculated assuming that only half of the VCSELs are on at one time, but that all of the VCSELs are biased to the threshold current, i.e., the VCSELs operate in the nonreturn to zero mode (NRZ). As a result,  $N/2$  VCSELs generate heat equal to  $V_{op}I_{op}$ , which are the voltage and current at the VCSEL operating output power of 2 mW. The other  $N/2$  VCSELs dissipate  $V_{th}I_{th}$ , which is the power dissipated at the lasing threshold condition. Therefore the VCSEL chip power dissipation is approximately:

$$P \sim (NV_{th}/2)(I_{th} + I_{op}), \text{ assuming } V_{th} \sim V_{op}. \quad (2)$$

Using the values reported by Kuksenkov et al.<sup>24</sup> for a  $6 \times 4 \mu\text{m}$  polarization controlled VCSEL with a maximum optical power out of  $\sim 3.2$  mW ( $I_{th}=1.29$  mA,  $I_{on}=6$  mA, and  $V_{th}\sim 1.5$  V), the power dissipated by an array of 1024 VCSELs is therefore  $\sim 5.6$  W; which is below the maximum allowable power dissipation of a properly heat sinked  $2 \text{ cm}^2$  chip. Continued improvements in VCSEL characteristics will lower the power dissipation even further.

For compactness, ease of optical alignment and packaging considerations, it is desirable to place all of the VCSEL control electronics and the VCSELs on a single chip. The

CMOS/VCSEL control chip must be composed of  $N$  pixels each of which contains an odd/even switch, two 424 bit shift registers and two VCSEL drivers (Fig. 3). There must also be  $N$  input channel bonding pads and bonding pads for each of the  $2N$  VCSELs. The necessity of  $3N$  bonding pads is immediately seen as a limitation to the scalability of the system. One solution to this problem is to use multiple chips. However, this will complicate the optics and optical alignment. A more promising solution is the flip chip bonding of the VCSELs directly to the pixels,<sup>25,26</sup> which, as discussed later, will reduce the number of bonding pads to  $\sim N$ .

To estimate the CMOS chip die size,  $0.35 \mu\text{m}$  CMOS design rules are used, although smaller line width will soon be commonplace.<sup>27</sup> A simple dynamic shift register (SR) can be used for the pixels since the ATM cells will be continuously clocked serial in and out, and serve only as a delay line. One bit of the SR will require  $\sim 150 \mu\text{m}^2$ , thus a 424 bit SR will require  $\sim 6.6 \times 10^{-4} \text{ cm}^2$ . Using standard  $90 \times 90 \mu\text{m}$  wire bonding pads requires  $\sim 1.6 \times 10^{-4} \text{ cm}^2$  per pad including the space between the pads. The size of the VCSEL driver depends on the maximum current that must be supplied and the required bit rate. By scaling the driver design of Banwell et al.<sup>20</sup> for both reduced design rules and lower maximum current, the required area of the driver can be estimated to be  $\sim 0.8 \times 10^{-4} \text{ cm}^2$ . The flip chip bonding pads for the VCSELs can be placed on top of the dielectric layers of the chip and therefore do not require any additional chip area. The total required chip is therefore,

$$2N(6.6 + 1.6/2 + 1) \times 10^{-4} \text{ cm}^2 \approx 1.6 \times 10^{-3} N \text{ cm}^2.$$

As a result, a  $1024 \times 1024$  switch will require a CMOS chip of about  $2 \text{ cm}^2$ .

Connecting VCSELs to smart pixels introduces fabrication problems since they cannot be readily grown on standard Si CMOS integrated circuits; thus, a hybrid technique is required. The three standard methods of making hybrid connections are wire bonding, bridge bonding or flip chip bonding the whole array onto CMOS chip.<sup>28</sup> Unfortunately none of these are suitable for large high speed arrays since they introduce large interconnect capacitance and/or use large chip area. We developed a coplanar contact flip chip process that places individual VCSEL directly within the pixel.<sup>25,26</sup> This technique requires further development but has been shown<sup>29</sup> to be scalable to over 4000 self-electro-optic devices (SEEDs) on Si CMOS. A flip chip process for LEDs was also reported<sup>30</sup> that utilizes shrinkable epoxy to reliably attach 2300 LEDs to a substrate with a  $10 \mu\text{m}$  pitch. Other processes have also been reported.<sup>31,32</sup> In addition, an  $8 \times 8$  array of photodetectors has been attached to a Si CMOS circuit using epitaxial lift off.<sup>33</sup> Therefore it appears that a suitable bonding technique for the proposed CMOS/VCSEL ATM switch will be developed in the near future and should not pose a limitation on switch size up to at least 1024.

### 3.3 Characteristics of the LC Routing Shutter Array

The proposed three stage  $1024 \times 1024$  ATM switch with 32 sectors operating at 155 MHz will require 65,536 LC pixels with a  $\text{CR} \geq 2N/m \geq 64$  and a switching time of  $2.7 \mu\text{s}$ . Taken together, these are demanding requirements but not beyond the state of the art since the development of LC on Si CMOS backplane technology has advanced rapidly in recent years,<sup>34</sup> e.g., pixel arrays of  $256 \times 256$  (65,536) and larger have been fabricated,<sup>35</sup> and LC switching times of  $17.2 \mu\text{s}$  have been demonstrated on Si backplanes with typical CMOS voltages and should decrease with continued research. Increasing the operating voltage will yield a faster switching speed, but this is at the expense of pixel density. CRs greater than 64 have been demonstrated.<sup>36</sup>

### 3.4 Optics and Optomechanics

For a  $1024 \times 1024$  cross point switch, the proposed VCSEL implementation reduces the number of resolvable points in the interconnect plane from  $>10^7$  using the previous suggested implementation<sup>7</sup> to  $6.5 \times 10^4$ . This greatly simplifies the optics, however, the overall size of the optics must be scaled to the size of the shutter. Consider an input plane of approximately  $15 \times 15 \text{ mm}$ . When this is replicated by  $m = 32$  times, the resultant images will only fit onto a VLSI based shutter if demagnification is used. This demagnification must be selected so that the reduced VCSEL beams are greater than (or equal to) the diffraction limited spot size at the operating wavelength. Since the emerging beams from a VCSEL are approximately  $6 \mu\text{m}$  in diameter and the diffraction limited spot size is only  $1.2 \mu\text{m}$  in diameter, a demagnification of 4 would be appropriate. The routing shutter will consequently fit on a Si VLSI chip. Using a chip of the order  $15 \times 15 \text{ mm}$  would require the use of lenses of the order 40 mm diameter. If such lenses have  $F$  numbers between 2 and 5, the length of the optical system would be of the order of 0.5 m, which would yield an

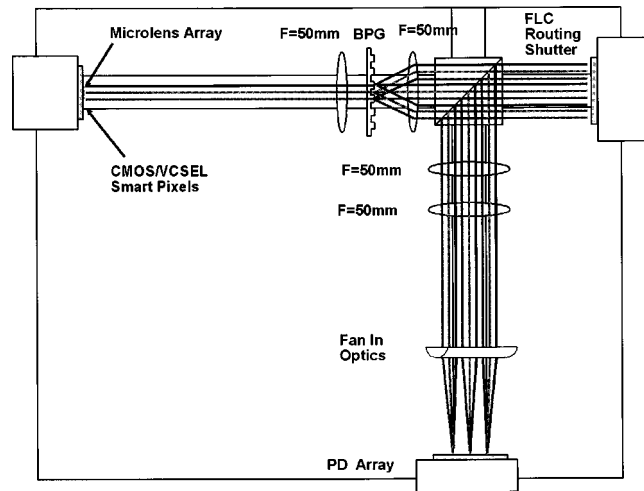


Fig. 4 Optical layout of the ATM demonstrator on a slotted plate.

approximate volume of  $200 \text{ cm}^3$ . While this simple analysis indicates that the switch can be assembled with reasonable optic components, a detailed optical simulation is required. A more practical design may require a tradeoff between the physical optics and the magnitude of the fan out.

## 4 Proof of Principle Demonstration

The optical layout of the demonstrator system was assembled on a  $12 \times 12 \text{ in.}$  slotted plate,<sup>37</sup> as illustrated in the drawing of Fig. 4 and the photo of Fig. 5. The system components consisted of a  $4 \times 4$  array of VCSELs ( $\lambda = 850 \text{ nm}$ ) mounted on a steel slug with the VCSELs electrically connected to driver circuits controlled by a PC. For this demonstrator, the VCSELs were not attached directly to a custom CMOS chip, but this arrangement will be used in subsequent demonstrators. A Display Tech SLM was used as the LC routing shutter and a CCD camera provided images of the output. The optics was composed of a microlens array placed in front of the VCSELs, four 50 mm focal length lenses and a 1 in. polarizing beamsplitter (PBS). A  $1 \times 5$  binary phase grating provided a fan-out for the 16 VCSEL beams, but only four of the five fan-out patterns were required. A  $1 \times 5$  fan-out was used since a low cost, off the shelf grating was available, thus avoiding an expensive custom grating. Two cylindrical lenses ( $F = 6 \text{ mm}$  and

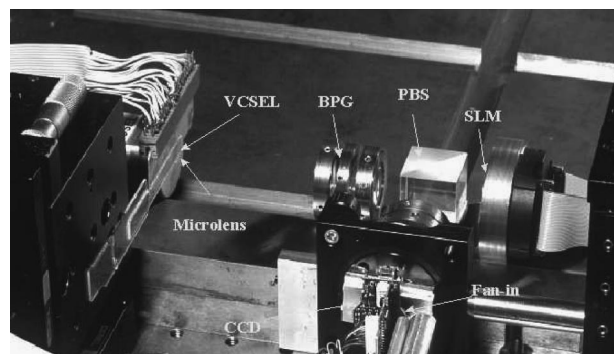
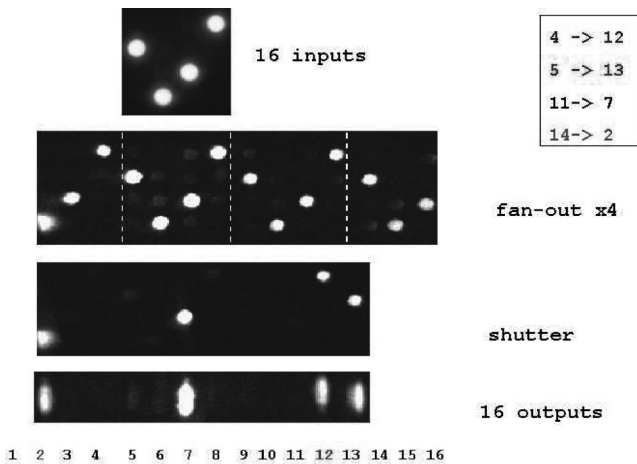


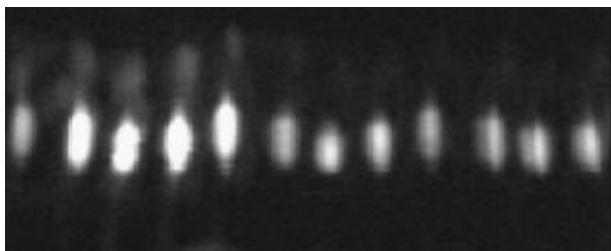
Fig. 5 Photograph of the demonstrator.



**Fig. 6** Patterns of the optical beams at different locations in the demonstrator: (a) 4 of the 16 VCSELs turned on (numbers 4, 5, 11 and 14); (b) after the fan-out by the BPG; (c) reflections from the LC SLM; and (d) after the fan-in optics.

$F=5$  mm) were used to fan-in the beams reflecting off of the SLM. The two lenses provided a better focus of the output beams than was possible with only one lens.

Proper routing through the demonstrator was verified by turning on several of the VCSELs and then routing them to different output locations by changing the LC pattern. Figure 6 illustrates the results of routing input 4 to output 12, 5 to 13, 11 to 7 and 14 to 2. Figure 6(a) shows the VCSEL array with numbers 4, 5, 11 and 14 turned on, Fig. 6(b) shows the  $4\times$  linear fan-out of these VCSEL beams from the BPG (note the CCD camera was not large enough to observe four full patterns), Fig. 6(c) shows the beams reflecting off the LC shutter and Fig. 6(d) shows these beams collected by the cylindrical fan-in lenses. Figure 6(d) shows the 4 outputs at the specified 12, 13, 7, and 2 output locations. Changing the shutter patterns with the same input pattern resulted in corresponding changes in the output beam locations. Figure 7 shows the output with all 16 VCSELs turned on. Turning one of the VCSELs off caused the output spot at corresponding location to turn off. These tests verify the general routing concepts of the proposed architecture. These tests were performed in a quasi static mode due to the limitations of the CCD camera and because the input data were not demultiplexed, however, parts of the system were tested up to 100 megabits/s. Note that the beams maintain their approximate Gaussian symmetry up to the fan-in optics, which cause the beams to elongate.



**Fig. 7** Output pattern with all VCSELs turned on with each routed to a different output channel.

## 5 Summary

Large ATM network switches require massively parallel, reconfigurable interconnections that must operate at high speeds. This is a difficult task for large switches and may be best implemented with a combination of electronic and free space optics, where the optics provides the reconfigurable cross point routing. This paper proposes an optoelectronic switch using VCSEL arrays for interconnects and an LC routing shutter. This implementation reduces the number of optical beams and simplifies the optics as compared to previously reported systems.<sup>4-7</sup> First order analysis of the required optical power, power dissipation and physical size of the arrays were presented that indicate that a switch as large as  $1024\times 1024$ , divided into 32 sectors, should be practical in the near future. Results from a proof of principle demonstrator verified the switching architecture.

This paper addresses only the problems associated with the reconfigurable optoelectronic cross point switch and not the extensive electronics that are required to perform such tasks as reading the header, sectorizing the input and output planes, arbitrating collisions and queuing the output. These functions are important and are similar for all high performance ATM switches, but a discussion of the design of these functions is beyond the scope of this paper.

## Acknowledgments

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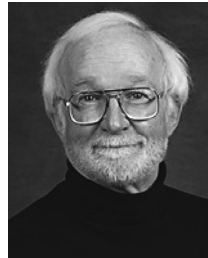
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